Explanation – Level-2 DFT Flow (EDT)

This document explains the flow and each screenshot captured in the project.

1. EDT Dofile (`edt_dofile.png`)

- Contains Tessent commands for setting up the EDT flow.
- Loads the design, standard cell library, and scan-inserted netlist.
- Calls the EDT insertion procedure.

2. EDT Log (`edt_log.png`)

- Tessent run log.
- Confirms:
    - 40 scan cells traced into 4 scan chains.
    - Decompressor and compactor successfully inserted.
- Shows warnings (e.g., X-state handling, scan init overhead). These are normal for EDT flow.

3. Synthesis Log (`syn_log.png`)

- Reports post-EDT area and timing.
- Example values:
    - Area ~1361 units.
    - Slack = 0 → no timing violation.
- Confirms netlist integrity after EDT.

4. Post-EDT Netlist (`case1_edt_top_gate.png`)

- Verilog gate-level netlist after EDT insertion.
- Contains scan-enabled flops and additional logic for decompressor/compactor.
- Example scan flop instance with scan enable, SI, SO.

5. TCD File (`case1_DmaWr_edt_tcd.png`)

- Tessent Constraint Description file.
- Describes how EDT wrapper connects to scan channels.
- Defines decompressor inputs, compactor outputs, scan channels.
- This is used later during ATPG pattern generation.

6. Terminal Log (`terminal_log.png`)

- Captured Tessent shell command execution.
- Shows working directory and flow stages (atpg, edt, edt_pipeline).
- Verifies script execution end-to-end.

Summary

At the end of Level-2 EDT:

- Scan chains were wrapped with EDT decompressor + compactor.
- Generated gate-level netlist + constraint file for compressed ATPG.
- No functional or timing errors introduced.

This sets the foundation for ATPG pattern generation in the next step.