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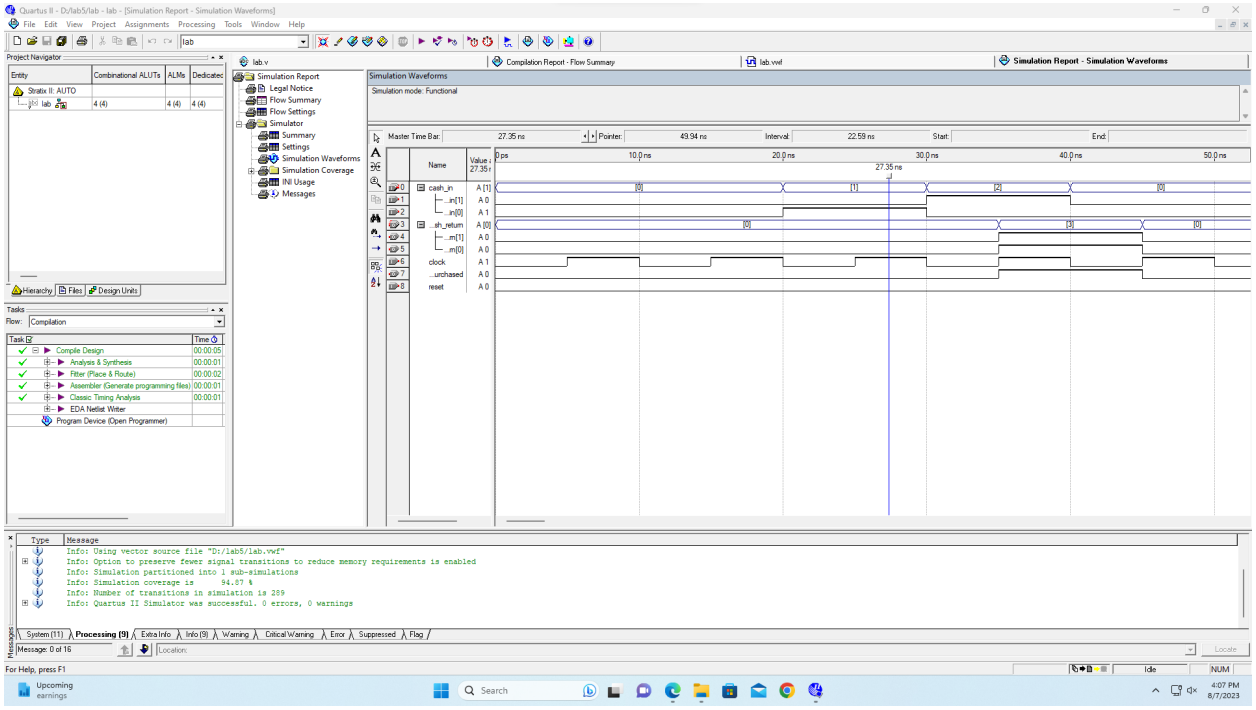
Section-06
Serial number-26
Lab-5

```
#Task-1
module lab(cash_in,clock, reset, cash_return,is_purchased);
input clock,reset;
input [1:0] cash_in;
output reg is_purchased;
output reg [1:0] cash_return;
reg present_state, next_state;
parameter s0=0,
s1=1,
tk_0 = 2'b00,
tk_20 = 2'b01,
tk_50 = 2'b10,
tk_10 = 2'b10,
tk_40 = 2'b11;
always @(posedge clock)
if (reset)
begin

present_state= s0;
next_state=s0;
end
else
begin
present_state=next_state;
case (present_state)
s0: if (cash_in == tk_0)
begin
next_state =s0;
```

```
is_purchased =0;
cash_return= tk_0;
end
else if (cash_in == tk_20)
begin
next_state =s1;
is_purchased =0;
cash_return= tk_0;
end

else if (cash_in == tk_50)
begin
next_state =s0;
is_purchased =1;
cash_return= tk_20;
end
s1: if (cash_in == tk_0)
begin
next_state =s0;
is_purchased =0;
cash_return= tk_20;
end
else if (cash_in == tk_20)
begin
next_state =s0;
is_purchased =1;
cash_return= tk_10;
end
else if (cash_in == tk_50)
begin
next_state =s0;
is_purchased =1;
cash_return= tk_40;
end

endcase
end
```

endmodule


Quartus II - D:/lab5/lab - lab - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Combinational ALUTs
ALMs
Dedicatec
Stratix II: AUTO
lab
4 (4)
4 (4)
4 (4)
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design 00:00:05
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:02
Assembler (Generate programming files) 00:00:01
Classic Timing Analysis 00:00:01
EDA Netlist Writer
Program Device (Open Programmer)
lab.v
Compilation Report - Flow Summary
lab.vwf
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar:
27.35 ns
Pointer:
49.94 ns
Interval:
22.59 ns
Start:
End:
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
27.35 ns
cash_in
clock
reset
Type
Message
Info: Using vector source file "D:/lab5/lab.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 94.87 %
Info: Number of transitions in simulation is 289
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (11)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Idle
NUM
Upcoming earnings
Search
4:07 PM
6/7/2023

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0 tk → 00
20 tk → 01
50 tk → 10
10 tk → 10
40 tk → 11

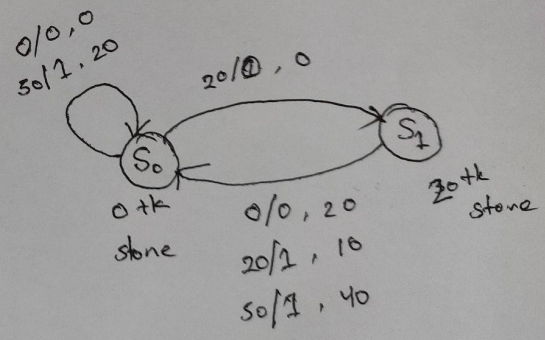
Problem 1:

You have to design a vending machine in Quartus for a 30 Tk product. User's money, returned money by the machine, and product bought condition is represented as cash_in (2-bit input), chg (output), and buy (1-bit output) respectively.

The vending machine can only accept three inputs: Tk 0 (cash_in = 00), Tk 20 (cash_in = 01), and Tk 50 (cash_in = 10). Once an acceptable input is more than or equal to 30 Tk, the machine immediately generates an output (buy=1), goes back to the initial state, and gives back the change (if required).

Requirements:

A. Draw the state diagram.
B. Write the Verilog code.
C. Run the simulation, and verify your answer.
   Hint:
   a) from 20 to 30 ns, provide 20tk and
   b) from 30 to 40 ns, provide 50tk and



Problem 2:

Suppose that we wish to design a **Mealy** type Finite State Machine (**FSM**) that meets the