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Section-06
Serial number-26
Lab-3

Question : 3>1>2>0

```
module lab3(w,y);  
input[3:0]w;  
output reg[1:0]y;  
  
always @(w)  
    casex(w)  
        4'b1xxx: y=3;  
        4'b0x1x: y=1;  
        4'b010x: y=2;  
        4'b0001: y=0;  
    endcase  
  
endmodule
```

Quartus II - D:\lab3\lab3 - lab3 - [lab3.v]

File Edit View Project Assignments Processing Tools Window Help

lab3

lab3.v

Simulation Report - Simulation Vectors

Entity

Entity	Combinational ALUTs	ALUTs	Dedicated
Stratix II: AUTO			
lab3	5 (5)	3 (3)	0 (0)

lab3.v

```
1 module lab3(w,y);
2   input [3:0]w;
3   output reg[1:0]y;
4
5   always @ (w)
6   begin
7     casex(w)
8       4'b1xxx: y=3;
9       4'b0x1x: y=1;
10      4'b010x: y=2;
11      4'b0001: y=0;
12    endcase
13 endmodule
```

Tasks

Row: Compilation

Task ID	Time (s)
Compile Design	00:00:06
Analysis & Synthesis	00:00:01
Filter (Place & Route)	00:00:02
Assembler (Generate programming file)	00:00:02
Classic Timing Analysis	00:00:01
EDA Netlist Writer	
Program Device (Open Programmer)	

Message

Info: Using vector source file "D:\lab3\lab3.vwf"

Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled

Info: Simulation partitioned into 1 sub-simulations

Info: Simulation coverage is 49.47 %

Info: Number of transitions in simulation is 437

Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (20) Processing (1) Extra Info (1) Warning (1) Critical Warning (1) Error (1) Suppressed (1) Flag (1)

Message: 0 of 16

For Help, press F1

Ln 13, Col 10

Idle

NUM

4:18 PM

7/10/2023

