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Section-06
Serial number-26
Lab-4

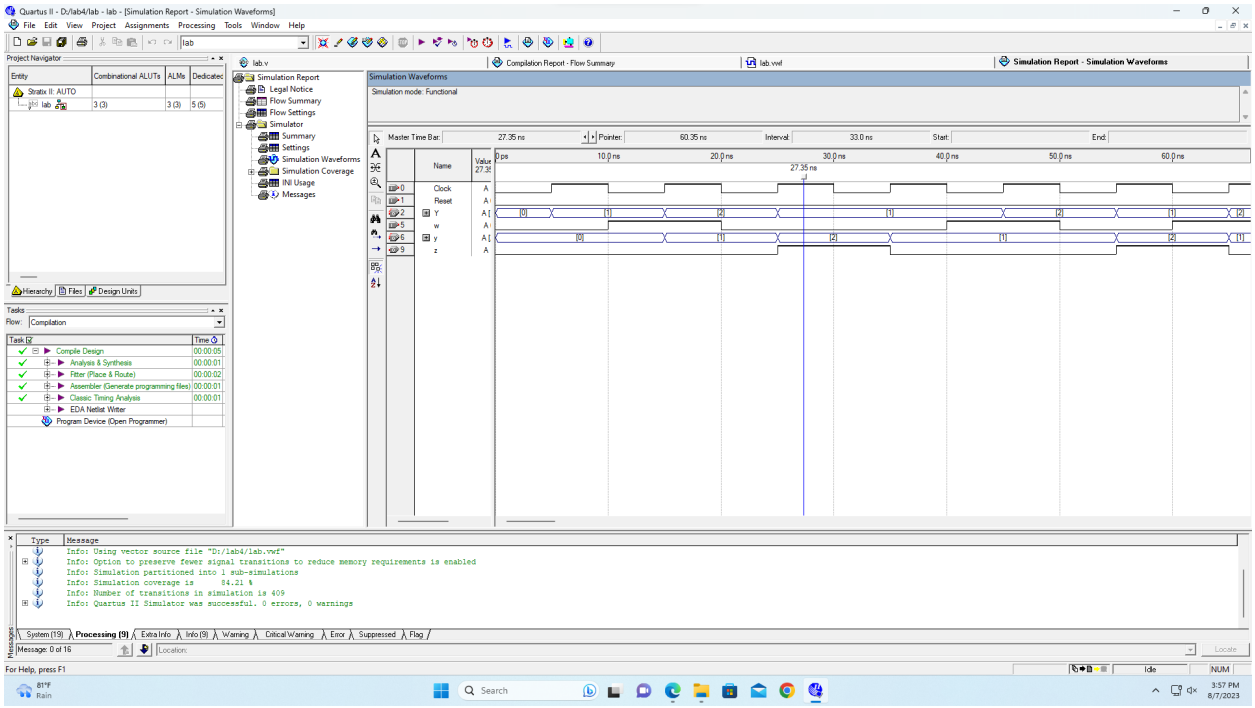
```
#Task-2
module lab(Clock, Reset, w, z,y,Y);
input Clock, Reset, w;
output reg z;
output reg [1:0] y,Y;
parameter [1:0] A = 0, B = 1, C = 2;

always @(posedge Clock, posedge Reset)
begin
if (Reset == 1)
begin
y = 0;
Y=0;
z=0;
end
else
begin
y=Y;
case(y)
A: if (w)
begin
Y= A;
z=0;
end
else
begin
Y= B;
z=0;
```

```
end
B: if (w)
begin
Y= C;
z=0;
end
else
begin
Y= B;
z=0;
end
C: if (w)
begin

Y= A;
z=0;
end
else
begin
Y= B;
z=1;
end
default: Y = 2'bxx;
endcase
end

end
endmodule
```


Quartus II - D:/lab4/lab - lab - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Combinational ALUTs
ALMs
Dedicatec
Stratix II: AUTO
lab
3 (3)
3 (3)
5 (5)
Hierarchy
Files
Design Units
Tasks
Flow:
Compilation
Task
Time
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
Classic Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
lab.v
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Compilation Report - Flow Summary
lab.vwf
Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Functional
Master Time Bar:
27.35 ns
Pointer:
60.35 ns
Interval:
33.0 ns
Start:
End:
Name
Clock
Reset
x
w
y
z
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
27.35 ns
Type
Message
Info: Using vector source file "D:/lab4/lab.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 84.21 %
Info: Number of transitions in simulation is 409
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (19)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
Messages
For Help, press F1
Idle
NUM
81°F
Rain
Search
3:57 PM
8/7/2023

Problem 2:

Suppose that we wish to design a **Mealy** type Finite State Machine (**FSM**) that meets the following specification:

- The FSM has one input w, and one output z.
- All changes in the FSM occur on the positive edge of a clock signal.
- The FSM has reset functionality.
- FSM will generate z = 1 at the instant the input values of w has the pattern:

=> 010

[Overlapping of the input patterns should be detected]