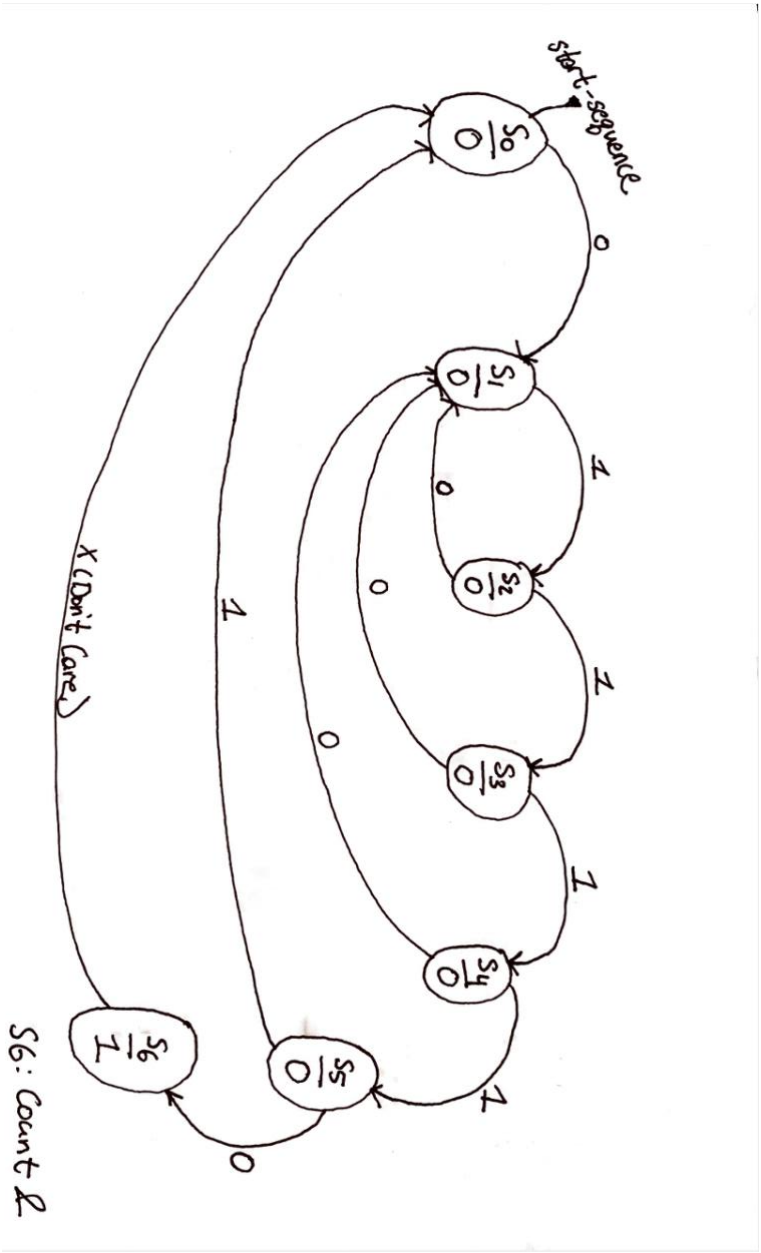
Ashaki Gumbs
Sequence Detector

A. Files for FPGA Implementation can be found here: Quartus_FPGA_Implementation
    a. Files for Xilinx Synthesis can be found here and in this Microsoft Word Document:
B. Finite State Machine



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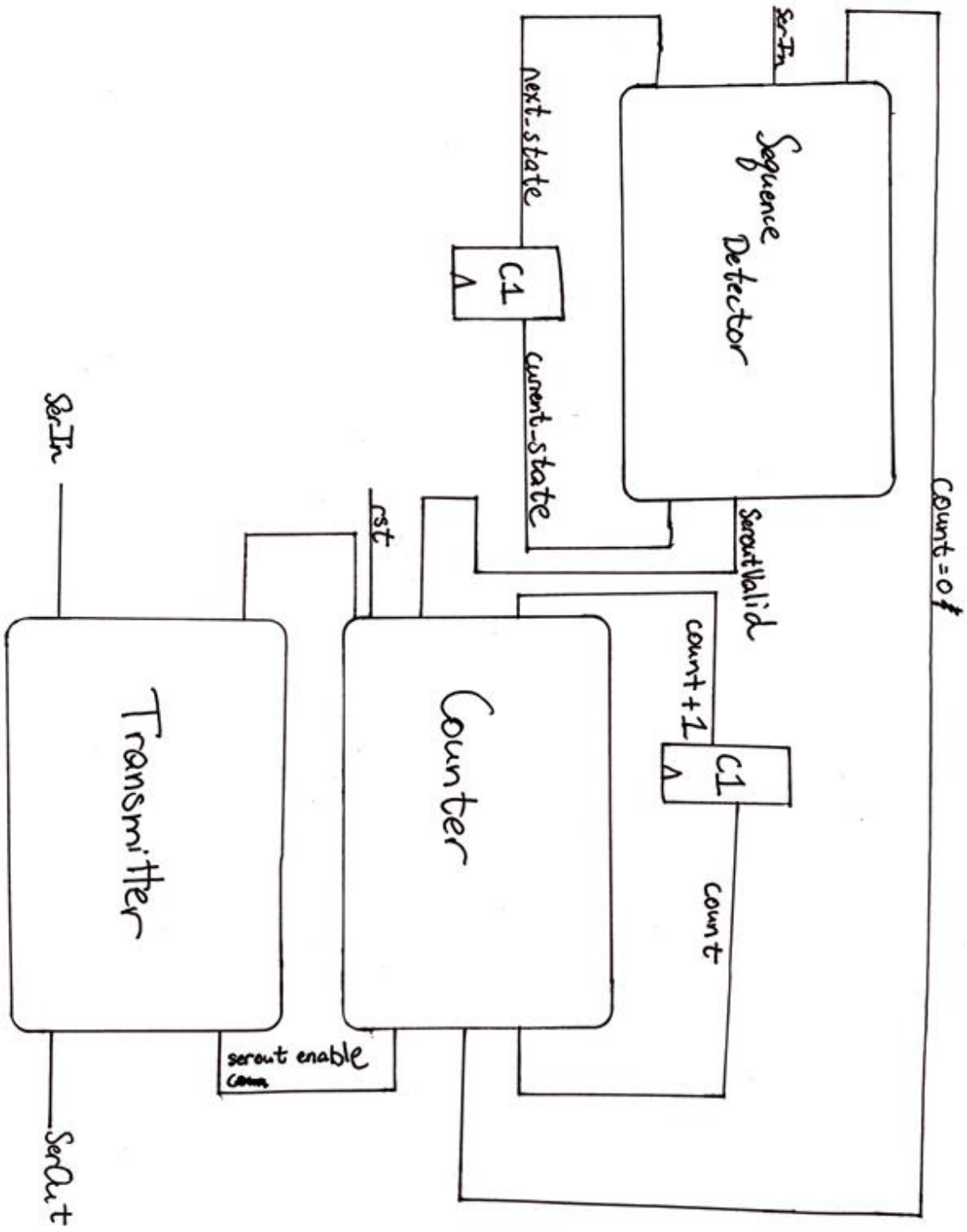
C. Wiring Schematic



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D. Write System Verilog description of transmitter circuit

```
assign serOut = (counter != 0)? serIn: 1'bz;
```

Figure 1: Transmitter

E. Write System Verilog description of sequence detector.

```
always @ (posedge clk or posedge rst)begin
 if (rst) current_state <= S0;
 else
 current_state <= next_state;
 $display("Current state is: %d", current_state);
End

always@(current_state, serIn, serOutValid, counter)begin
  case(current_state)
  S0:if (serIn==0) next_state <= S1;  else next_state <= S0;
  S1:if (serIn==1) next_state <= S2;  else next_state <= S1;
  S2:if (serIn==1) next_state <= S3;  else next_state <= S1;
  S3:if (serIn==1) next_state <= S4; else next_state <= S1;
  S4:if (serIn==1) next_state <= S5; else next_state <= S1;
  S5:if (serIn==0) next_state <= S6; else next_state <= S5;
  S6:if (counter == 1023) next_state <= S0; else next_state <= S6; // sequence detected
  endcase
end

assign serOutValid = (current_state == S6)? 1: 0; //if in S6, start counter
```

F. Write SystemVerilog Description of Counter

```
logic [10:0] counter; //1024 clock cycles
always@(posedge clk or posedge rst) begin
   if(rst) begin
      counter <= 0;
    end else if (serOutValid==1 && clk == 1)begin
      counter <= counter + 1'b1;
     end
end
```

G. Write the SystemVerilog Description of the testbench: ***Continued on next page…***

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```
module Top_Test();
reg In;
reg clk;
reg rst;
wire Out;
int p;
logic[10:0] i;

Top uut(.serIn(In), .clk(clk), .rst(rst), .serOut(Out));

//Detect Sequence//
initial begin
clk = 0;
rst = 0;
In =1'bz;
#10
rst = 1;
#10
rst = 0;
#10
In = 1'b0;
#10
In = 1'b1;
#10
In = 1'b1;
#10
In = 1'b1;
#10
In = 1'b1;
#10
In = 1'b0;
#10
In = 1'b1;


//Sequence Detected
#10
In = 1'b0;
#10
for(i = 0; i <= 1024; i = i +1)begin
   #10
   In = $urandom_range(1,0);

   end
end


always # 5 clk = ~clk;
endmodule
```

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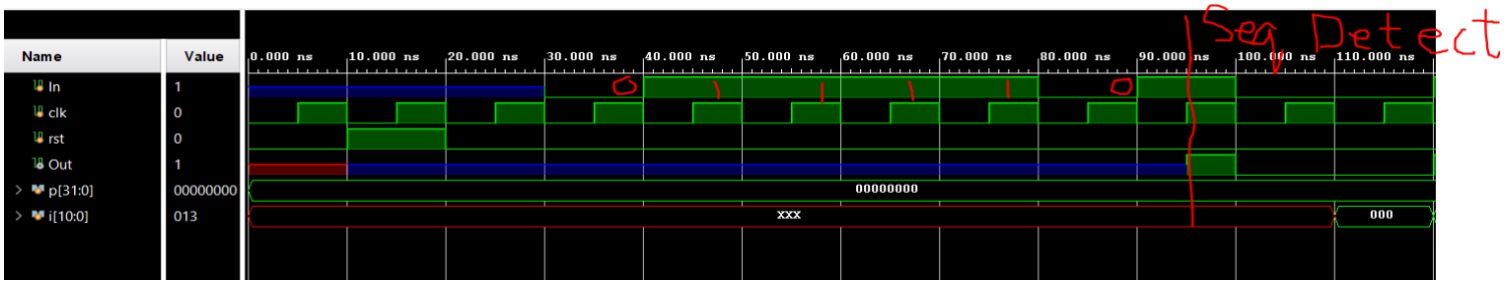
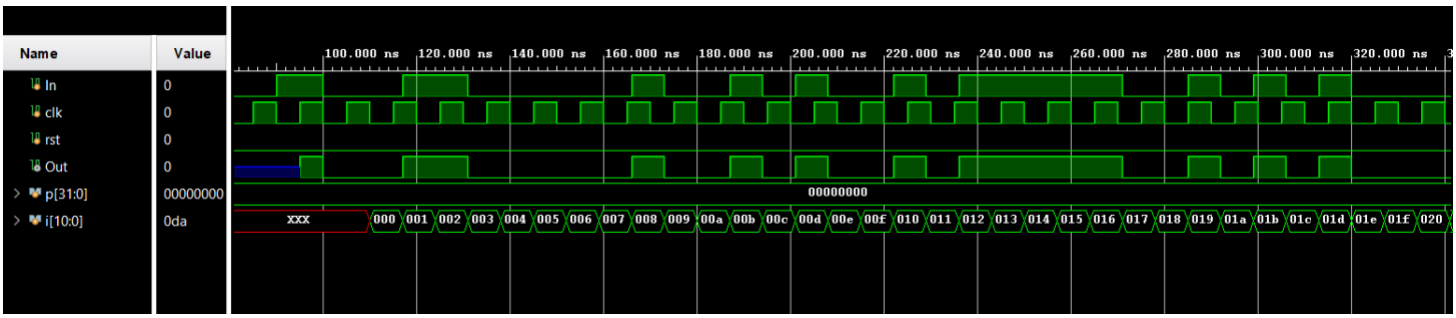
Simulation when sequence detected



Transmit when sequence detected



1024-clock cycles once sequence is detected…