EE312 Group Project

Name: DAMERA ASHAN RAJ
Roll No: 190102022

Group -5

- DAMERA ASHAN RAJ-190102022
- DESABOINA HEMAKRISHNA – 190102023
- DHANAVATH BASKER – 190102024
- DIBYA DARSHNEY - 190102025

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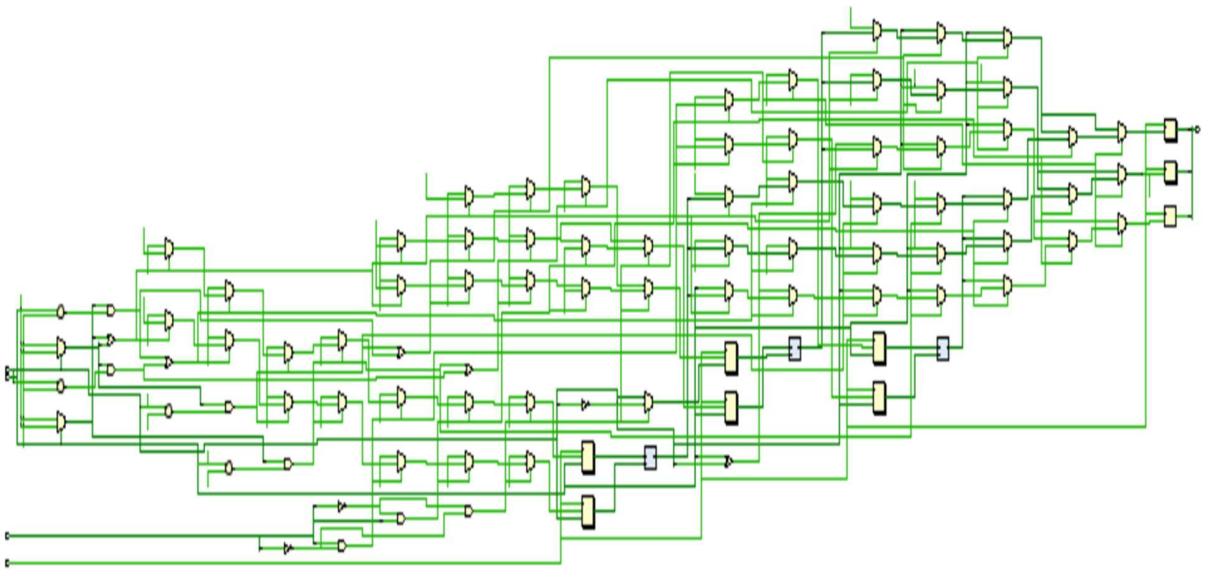
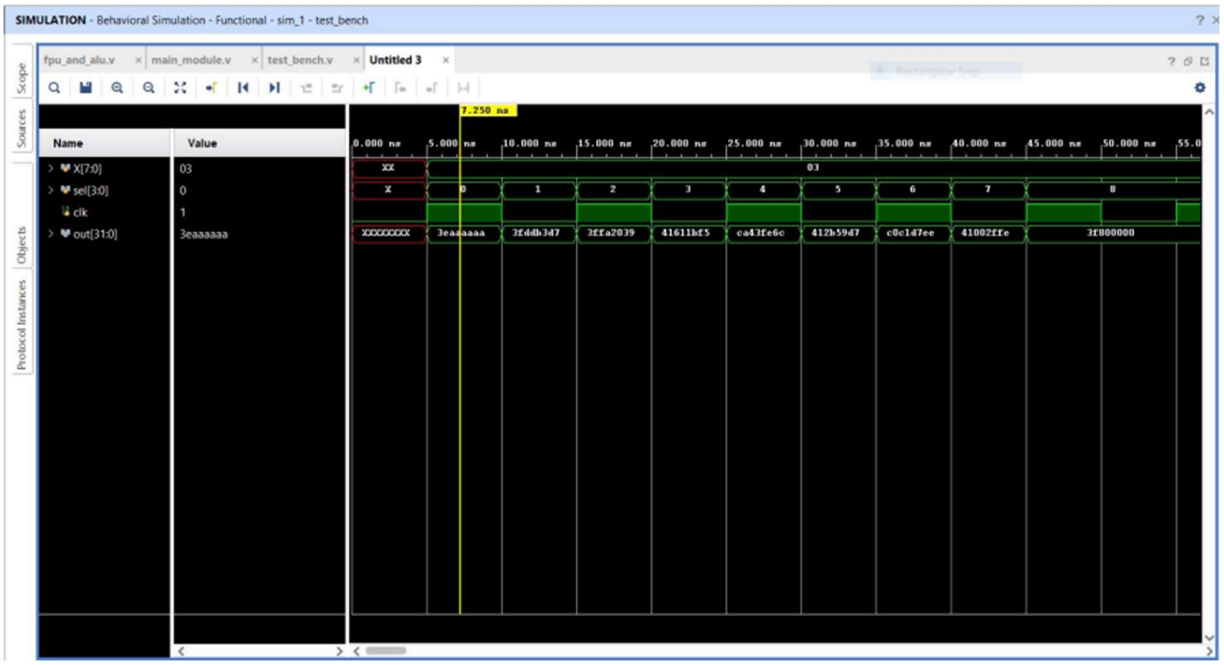
1. **Verilog Code For FPU and ALU and Main file have been submitted through ZIP Folder.**
2. **Schematic:**

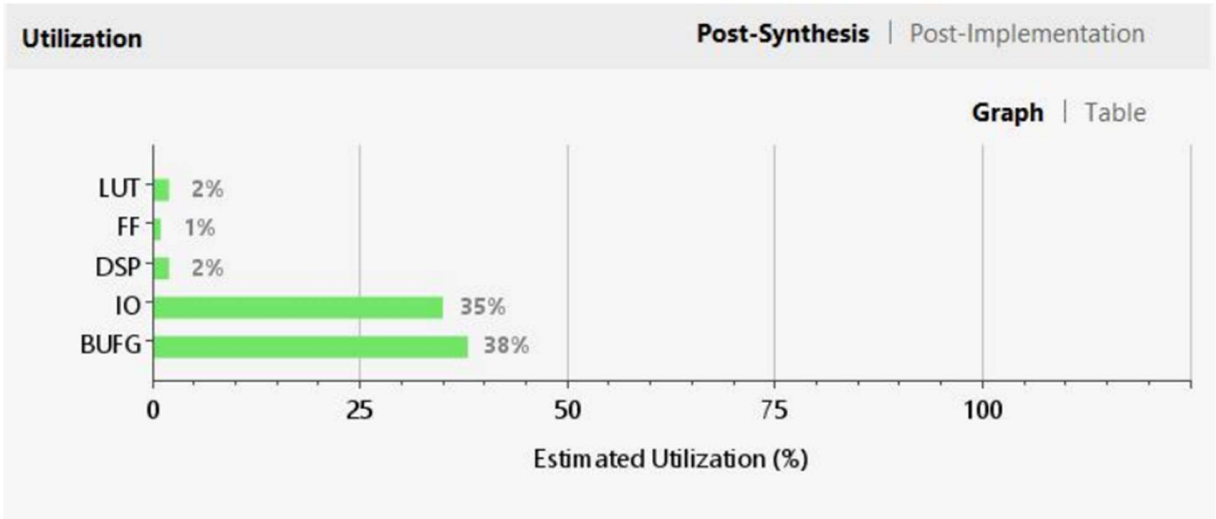


3. Behavioral Simulation Output Form:



4. Synthesis Report:

- **Utilisation Summary:**



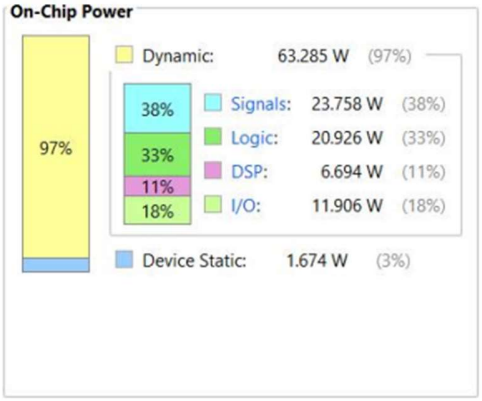
- **Power Summary:**

Summary

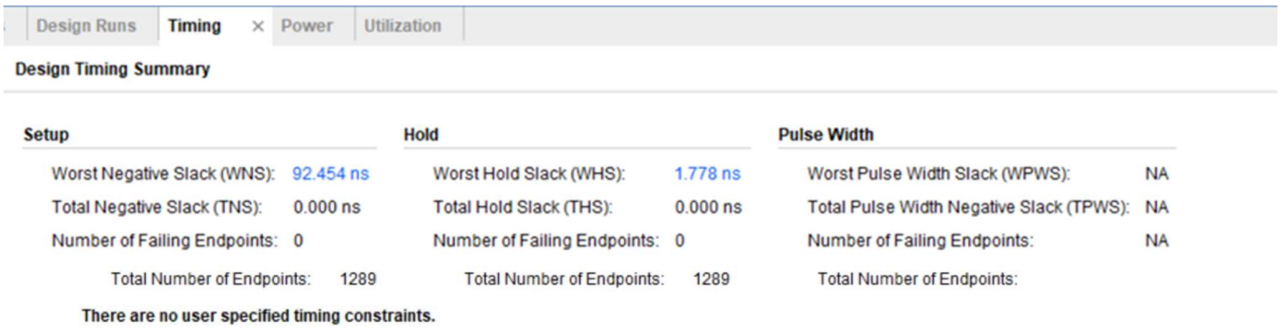
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**64.959 W (Junction temp exceeded!)**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**125.0°C**
Thermal Margin:	-155.3°C (-45.6 W)
Effective θJA:	3.3°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

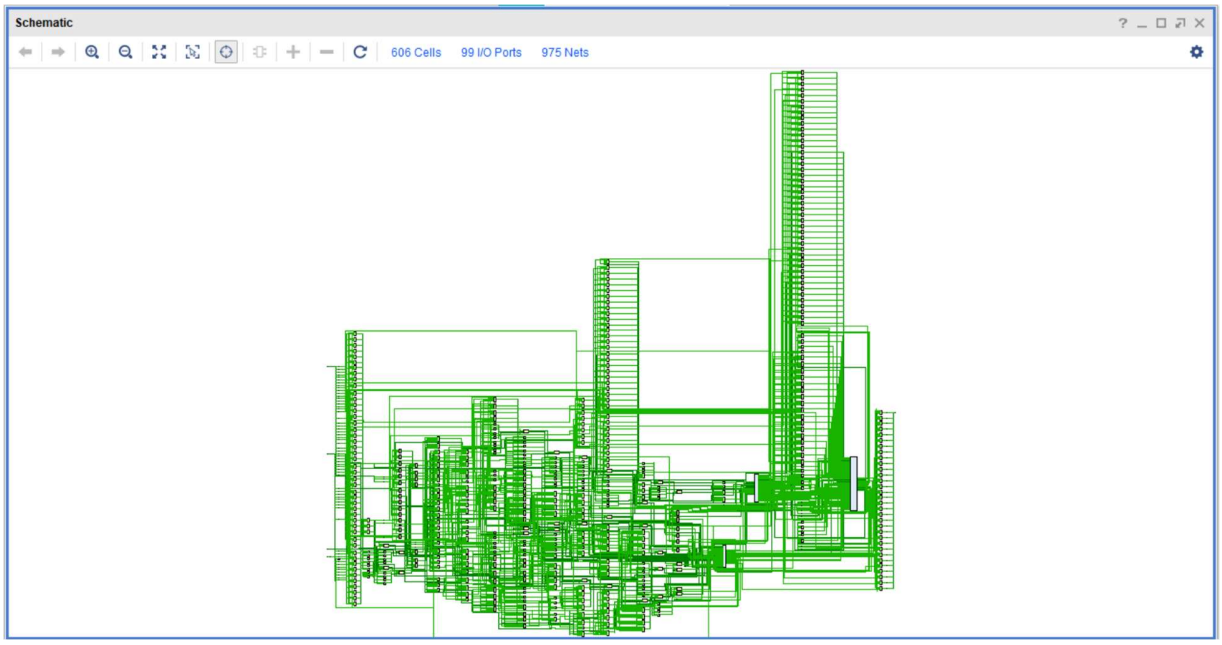
Launch Power Constraint Advisor to find and fix invalid switching activity



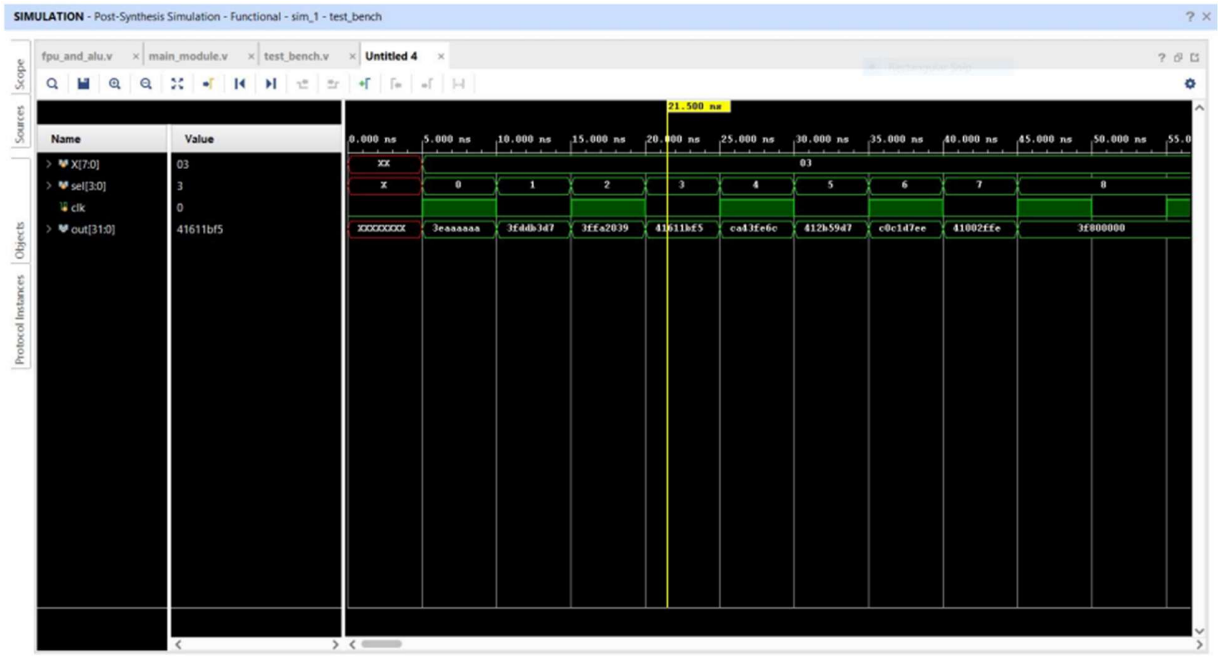
5. Timing Summary



6. Schematic Diagram:

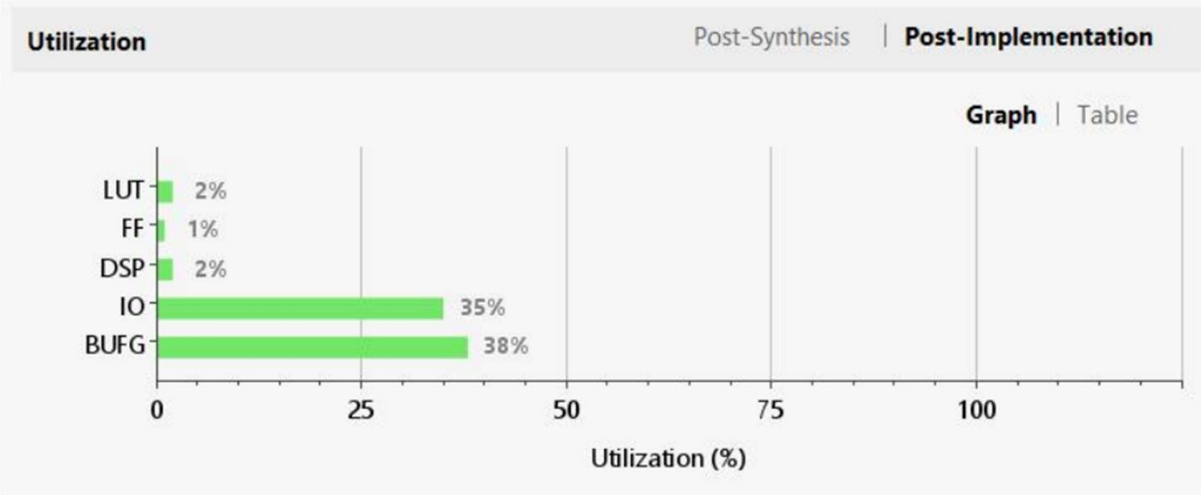


7. Post synthesis functional simulation output waveform

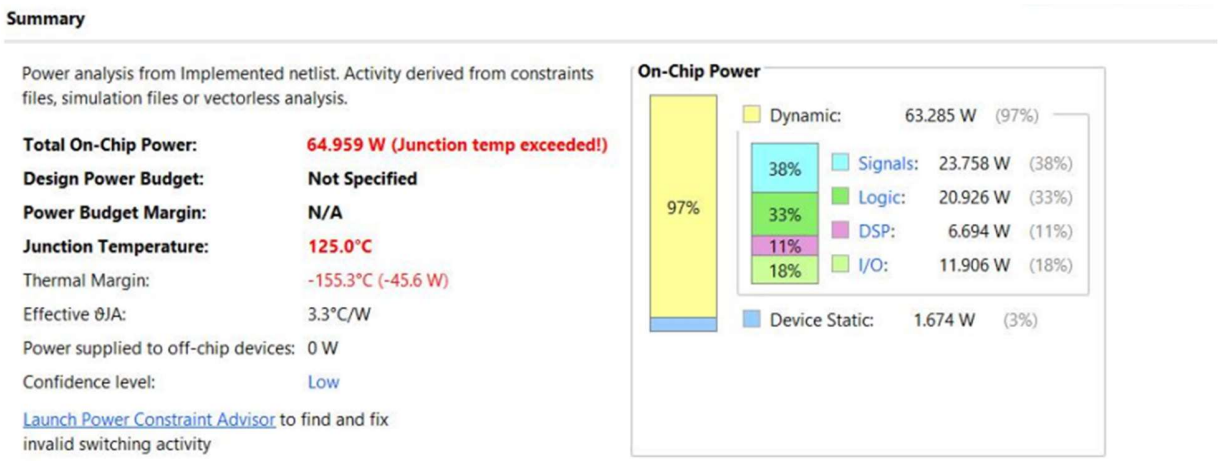


8. Implementation report

- **Utilization summary:**



- **Power summary:**



- **Timing report:**

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	88.480 ns	Worst Hold Slack (WHS):	2.310 ns	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	16	Total Number of Endpoints:	16	Total Number of Endpoints:	NA

All user specified timing constraints are met.

9. Post implementation functional simulation output waveform