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Welcome to HDL Lab 2017

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HDL Lab 2017 - Outline

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1. Introduction, Motivation and Warm Up
2. Task Assignment for 2017
3. Requirements
4. Quick Start
5. Q & A

Motivation

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Why do we set up such a HDL Lab in such a hot summer

- Continuing the CAD4SOC lecture
- HDL design technique is state-of-art in industry and hot
- Every EE engineer should know

What will you learn from the lab?

- Extend your HDL knowledge from exam papers to real practise
- Design Flow and EDA Tools (Modelsim, Synopsys Design Complier)
- Maybe Basic Linux & Unix (be sure you do not hate them)

After the lab, you might

- Thesis at IES?
- Anyway enjoy the second half of August!

Warm Up

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Work in groups of 4 with 2 user accounts, in each group

- One common language among group members
- Divide the work among group members but everyone should know what others are doing
- Change of groups in between is not allowed

What is the time and venue arrangement for the lab?

- From Mon. 31. 07 – Fri. 11.08 (Two weeks, ten working days)
- Daily from 9 am to 6 pm !!!
- In S306 /067

Evaluation and Exam

- On spot check on 11. 08 (Friday) from the morning, in your lab set up
- Report submission deadline on 16. 08 (Wednesday) 23:59:59
- Oral exam (in groups) date will be announced in TUCaN.

Lab Rules

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Absence

- Only health related problems and exams would be taken as exceptions

Team work and room policy

- Do not blame your team mates
- Water is allowed, but NOT cola and any food

Task Assignment 2017

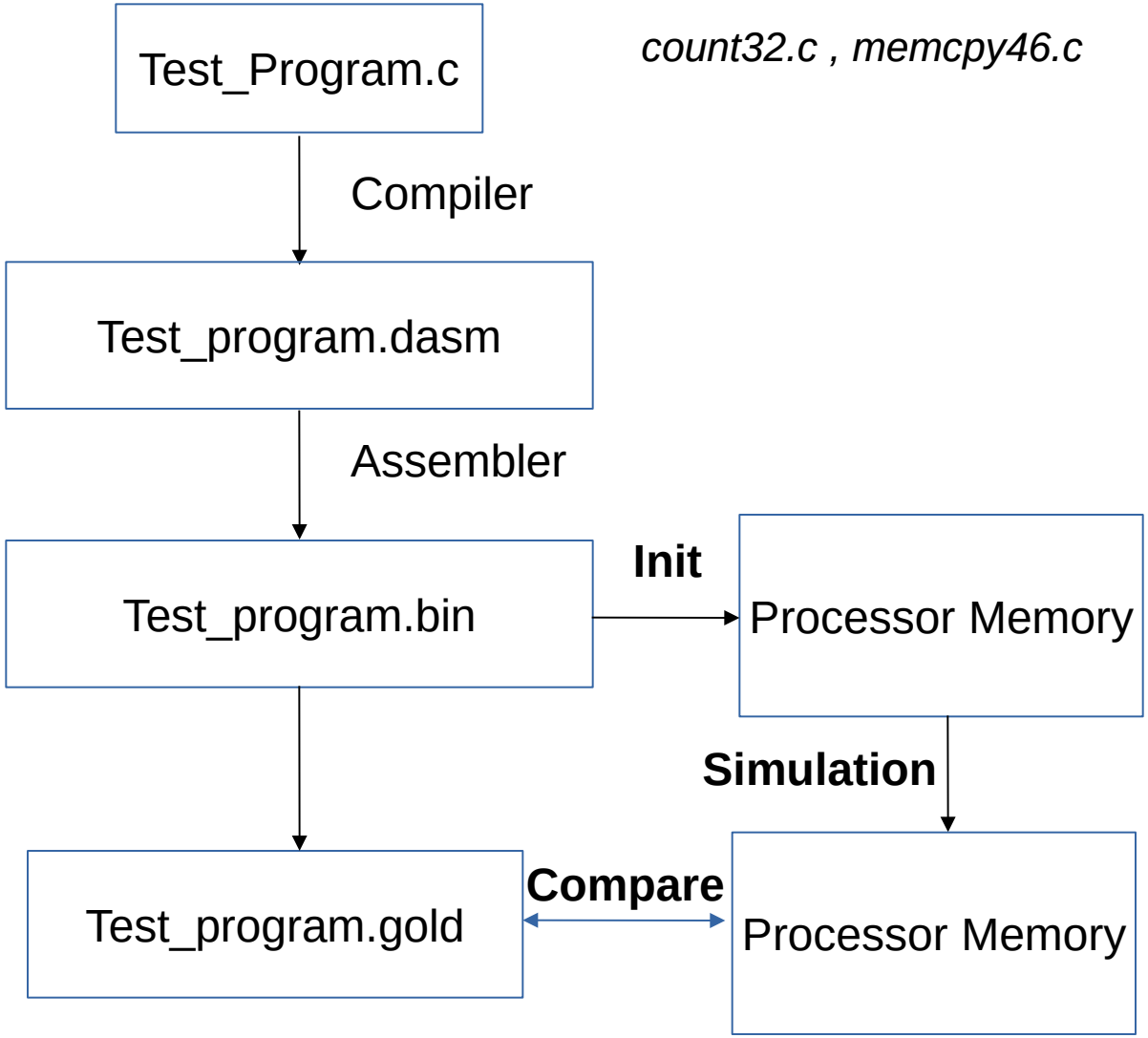
Model a processor that executes the given C-programs – assembled for the ARM THUMB instruction set – in Verilog

Correctly Execute the Given Binary

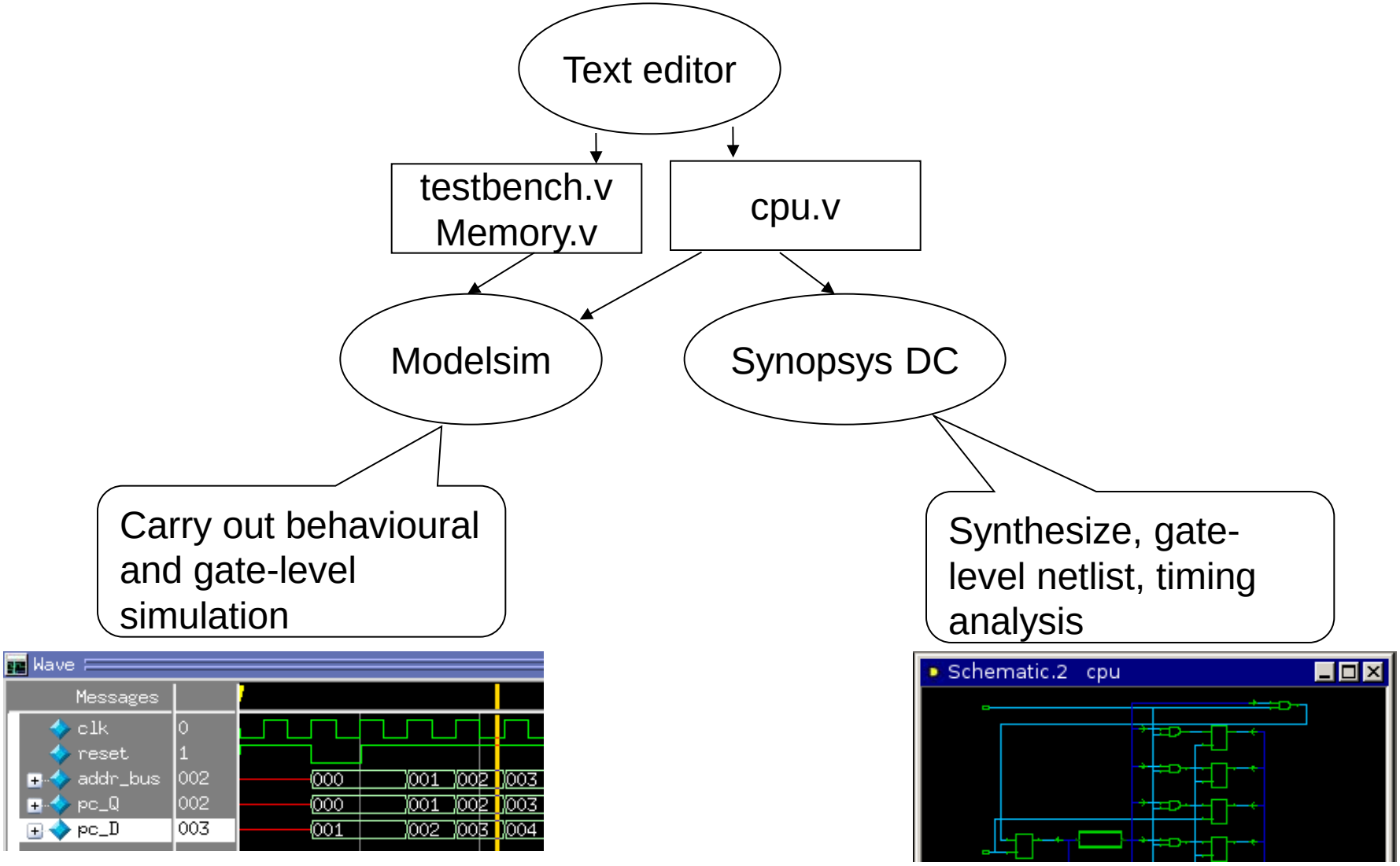
Reasonable Architecture

Synthesizable

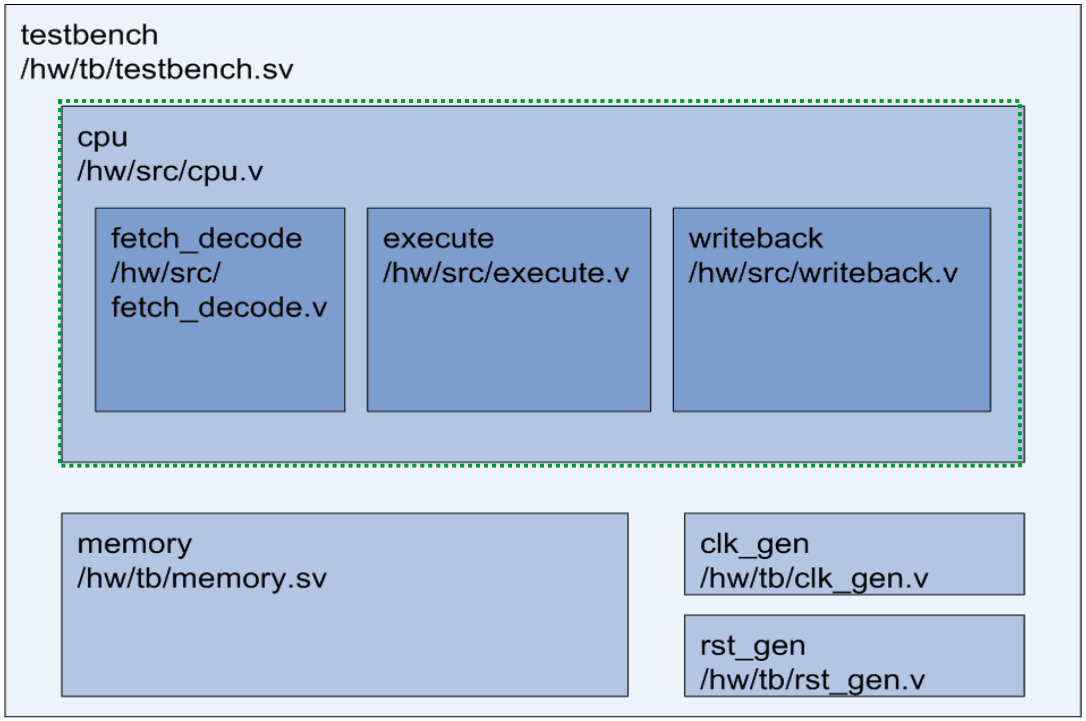
Design Flow - 1



Design Flow – 2



Final Paradigm



Verilog Files provided:
1. testbench
2. memory module

Requirement

Use of pipeline stages (recommended 3 stages)
If you have a strong will, you can do it up to 5

The count32 and memcpy46 should be correctly executed on your CPU
Evaluation through the comparison between the Memory content and .gold file

The CPU should be synthesizable
Max. frequency, Area, Gate level simulation, … should be done

Try your best to shorten the overall execution time for the given applications

Group Effort

Individual Effort

Report Quality (English)

No Plagiarism!! All the codes will be checked with automated tools.

Quick Start – Today

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Log on with the account details provided

Copy HDL_Lab_2017.zip from /home/vhdlpxx/lehrepub/vhdl to another directory

Understand the testbench.v, count32 and memcpy46

Understand the relationship between .dasm, .bin and .gold

Know where to check for the instructions

Run the given testbench.v with memory (without CPU)

Quick Start – Until Tomorrow Evening

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Decide the architecture of your CPU (Pipeline, Blocks, …)

Divide work to all team members

Start to work!

Evaluation

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The best teams will definitely have 1,0

Important points for checking on 11.08

- Functionally correct
- Synthesizable
- Clock frequency
- Area
- Speed
- Power
- Gate level simulation
- Clean codes

Final delivery format is given in the folder, please follow

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Any Questions?