Single-Port SRAM Compiler
UMC 0.13µm (L130E-HS-FSG)
Preliminary Information

Features

- High performance – 523 MHz for a 4Kx16 array
- Synchronous read/write operations
  - Rising-edge triggered
- Same read and write address port
- One Input and One Output data port
- Data retention at low voltage
- Zero standby current
- 3-State output buffers
- Byte-write control for selective data write
- Routable over the core with metal 5 and higher metal layers
- Ability to compile to multiple aspect ratios
- Interface to industry standard BIST controllers

Applications

The Single-Port SRAM Compiler is a high density, high performance memory solution for embedded applications. The UMC supplied bordered bit cells achieve reduced die area while maintaining low mask cost. "What-if" scenarios are easy to explore using the Single-Port SRAM Compiler to perform optimal floorplanning of your design.

System designers can evaluate early architectural tradeoffs between performance, area and power by easily varying the aspect ratios, word depths and word widths of their designs. Once satisfied with the resulting configuration, the compiler will create all the EDA model views necessary to drive today's most popular IC design software.

Functional Description

The Single-Port SRAM Compiler has a single address port for both read and write addresses with separate data ports. Read and write cycles are timed with respect to a single edge of the clock. During both read and write cycles, the write enable and cell enable inputs are sampled by the rising edge of the clock. During a read cycle, if the cell enable is de-asserted, the data output bus values are held. If the cell enable is low, write enable is high and output enable is low, data from the addressed location is propagated to the data output using self-timed circuitry.

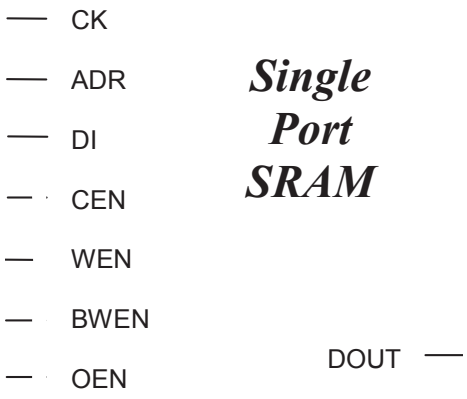
The data output bus has an asynchronous tri-state enable control input. During a write cycle, if CEN is low, the sampled input data is written to the specific address location. The written data is also propagated to the data output. The SRAM has byte write capability. There is one BWEN (byte write enable) pin per byte. To write into the selected byte at the current memory address, WEN and BWEN must both be active.

The SRAM also has BIST (Built in Self-Test) option. When this option is selected, additional pins are generated for ADDR, CEN, OEN, DI and BWEN.

UMC

I/O Pin Description

Name	Type	Description
CK	I	Clock Input
ADR [m:0]	I	Address bits, latched at the rising edge of CK
DI [n:0}	I	Data bits, latched at the rising edge of CK
DOUT[n:0]	O	Data Output bits
CEN	I	Cell Enable, Active Low, latched at the rising edge of CK
WEN	I	Write Enable, Active Low, latched at the rising edge of CK
BWEN [n/8:0]	I	Byte Write Enable, Active Low, latched at the rising edge of CK
OEN	I	Output Enable, Active Low



Key Features

Features	Capability
Maximum Macro Size	256Kbit
Maximum Words	16K
Minimum Words	64
Word Increment	2 * column mux
Maximum Data Width	128 bits
Minimum Data Width	2 bits
Data Width Increment	1 bit
Column Mux	4,8,16,32

Performance and Area

Typical case memory performance should meet the following specs:

Memory	Size	Area(mm 2)	T ACC (ns)	Fmax (MHz)	Power (uW/MHz)
Single Port SRAM	4Kx16	0.21	1.8	523	44.4

Typical corner is typical process model at 25c, VSS = 1.5V with 0.004 pf output loading

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