TECHNISCHE UNIVERSITÄT DARMSTADT

Synopsys Design Compiler Quick Start

M.Sc. Sarath Kundumattathil Mohanan
Room: S3|06/345a
Email: sarath.mohanan@ies.tu-darmstadt.de

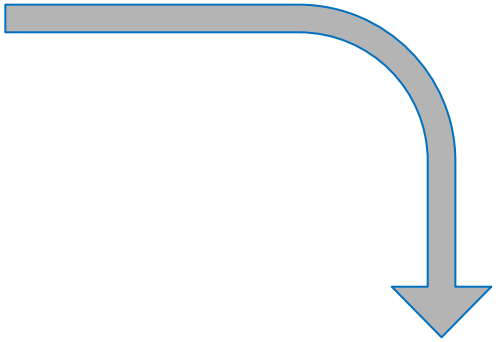
Synthesis Overview

```
module IADD
 (input  wire [31:0] OP_A_I,
  input  wire [31:0] OP_B_I,
  output wire [31:0] RESULT_O);

  assign RESULT_O = OP_A_I + OP_B_I;

endmodule
```

RTL Code



```
XOR2XD1BWP12TLVT U44 ( .A1(n29), .A2(n28), .Z(n32) );
AN2D1BWP12TLVT U45 ( .A1(n18), .A2(RSOP_18_C1_DATA1_8), .Z(n36) );
AN2D1BWP12TLVT U46 ( .A1(n30), .A2(r_plus[8]), .Z(n35) );
AN2D1BWP12TLVT U47 ( .A1(n18), .A2(RSOP_18_C1_DATA1_7), .Z(n40) );
AN2D1BWP12TLVT U48 ( .A1(n30), .A2(r_plus[7]), .Z(n39) );
AN2D1BWP12TLVT U49 ( .A1(n18), .A2(RSOP_18_C1_DATA1_6), .Z(n44) );
AN2D1BWP12TLVT U50 ( .A1(n30), .A2(r_plus[6]), .Z(n43) );
AN2D1BWP12TLVT U51 ( .A1(n18), .A2(RSOP_18_C1_DATA1_5), .Z(n48) );
AN2D1BWP12TLVT U52 ( .A1(n30), .A2(r_plus[5]), .Z(n47) );
AN2D1BWP12TLVT U53 ( .A1(n18), .A2(RSOP_18_C1_DATA1_4), .Z(n52) );
AN2D1BWP12TLVT U54 ( .A1(n30), .A2(r_plus[4]), .Z(n51) );
AN2D1BWP12TLVT U55 ( .A1(n18), .A2(RSOP_18_C1_DATA1_3), .Z(n56) );
```

Gate Level Netlist

Step 1 – Loading the Design

Desing Compiler/Desing Vision should be launched from the syn directory of your project	cd ~/HDL_Lab/syn
Open a terminal and start the compiler	module load syn design_vision
Load the technology libraries	Run script in design vision (File -> Execute Script) ***setup.tcl***
Create the project setup	***project_setup.tcl***
Load the RTL codes and elaboarte into library WORK	***load_design.tcl***

Step 2 – Applying Constraints

Maximum clock frequency constraint is applied now	***constraints.tcl***
Check Timing and Connectivity issues	***check.tcl***

Look at the log output pane in GUI. Check_timing should return a ‘1’ to indicate that timing constraints have not created any problems.
Similary check_design should return ‘1’ for connectivity checks.

Step 3 – Run Synthesis

Compile the design and write the gate level netlist	***compile.tcl***

The design is synthesised into gate level netlist at this step generating a single verilog netlist for the whole design.
The associated timing information is also saved as a .sdc file.

Step 4 – Save Data

All the reports are generated	***report.tcl***

The various paramters of the design like power consumption, area occupied , timing information etc. are saved into different report files.

Q & A

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If you do not have any questions, let's move to the labs!