Modelsim Quickstart

- Log in to Asterix

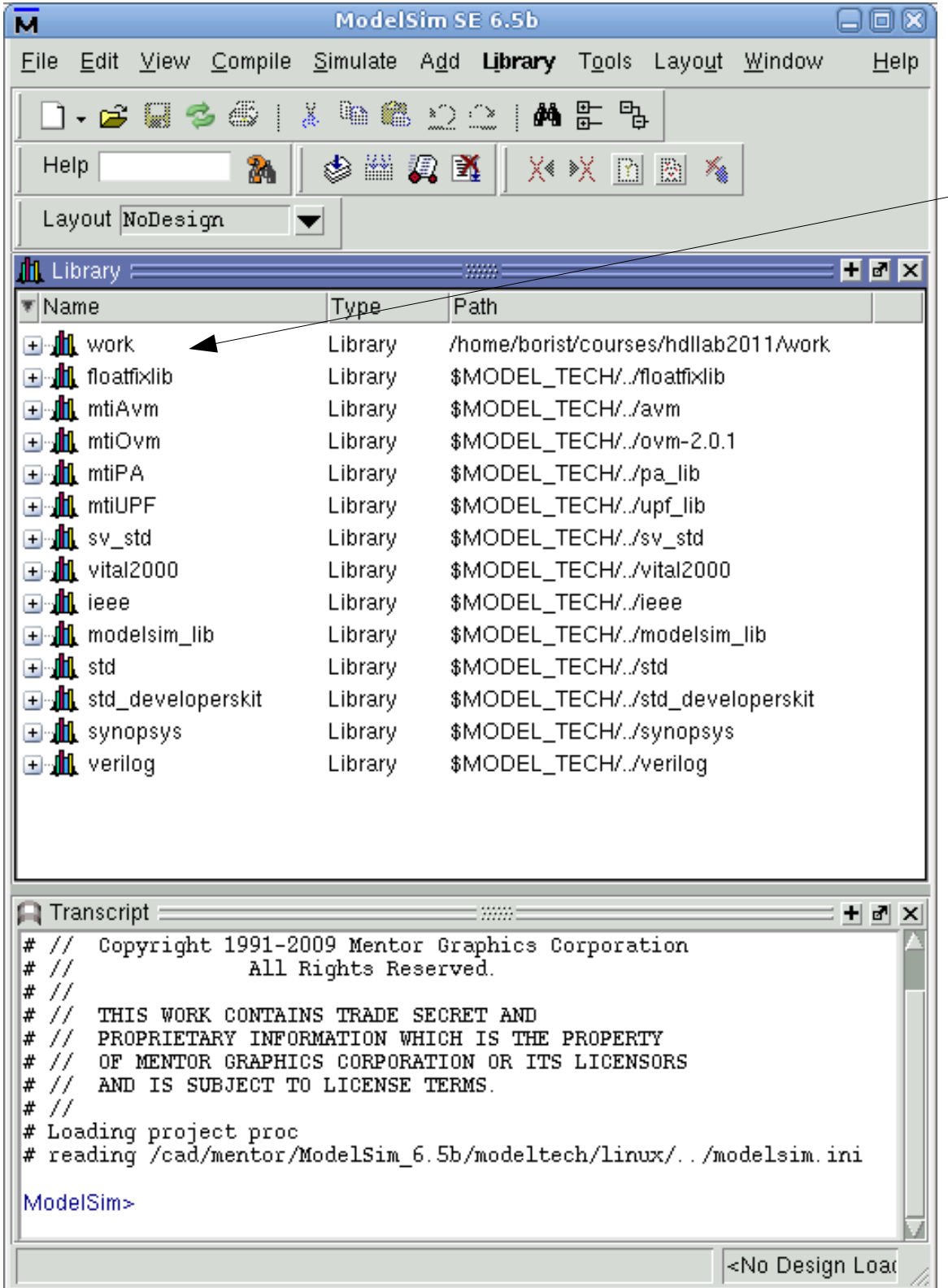
  >ssh -X Asterix
- Load Modelsim

  >module load modelsim
- Create new folder

  >mkdir hdllab

  >cd hdllab
- Start Modelsim

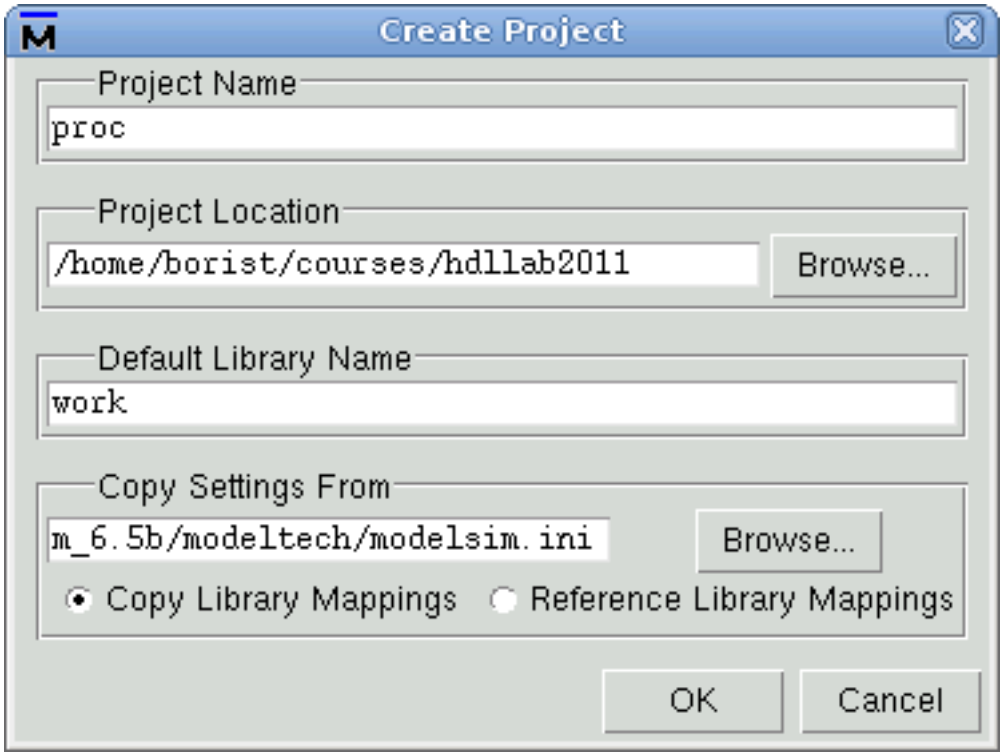
  >vsim &

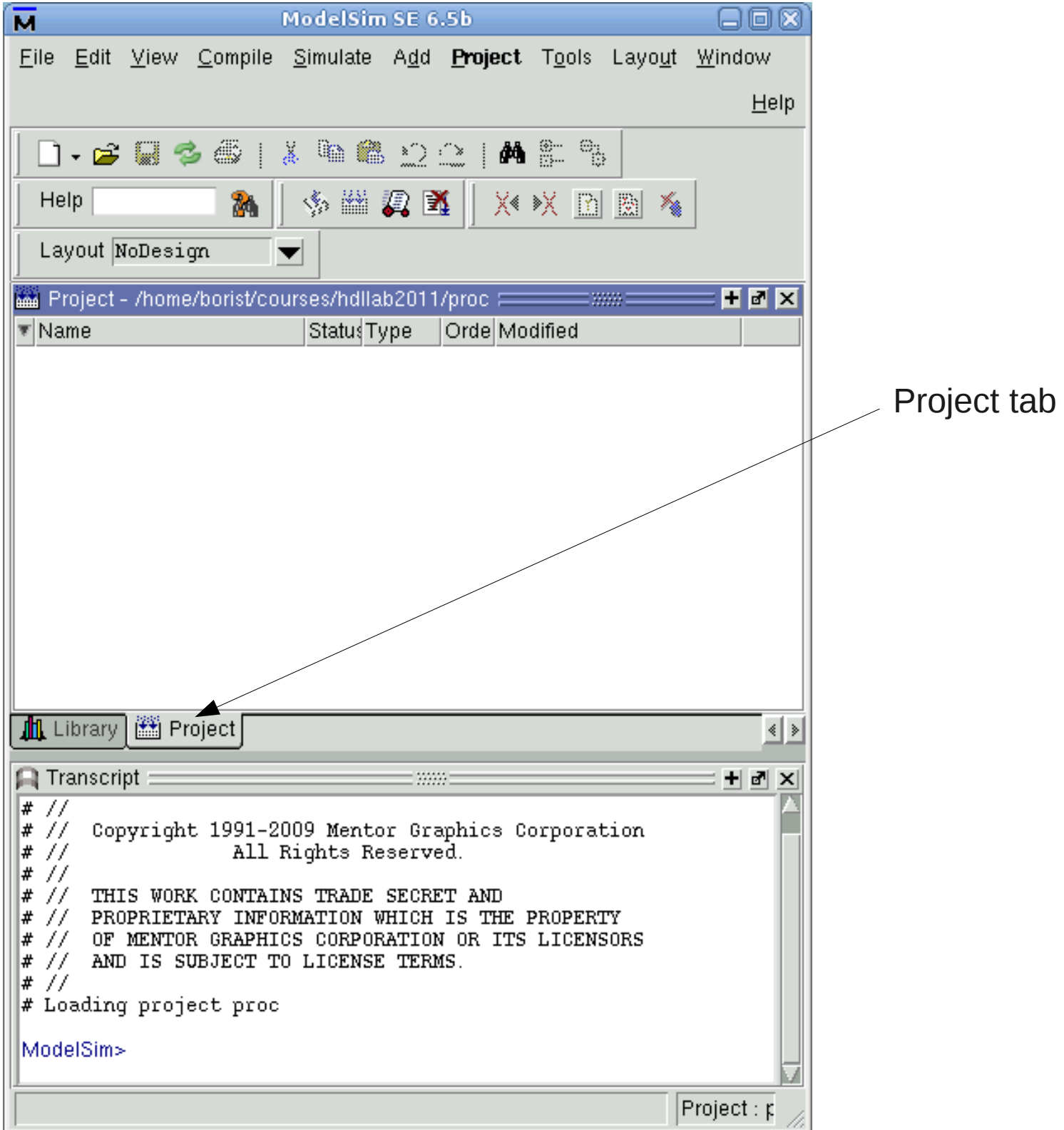


your working library

Create a Project

- Click on “File->New->Project” in the menu bar. A popup window will open.
- Enter a project name of your choice, e.g. “proc”.
- Click “OK”




ModelSim SE 6.5b
File Edit View Compile Simulate Add Project Tools Layout Window
Help
Help
Layout NoDesign
Project - /home/borist/courses/hdllab2011/proc
Name Status Type Orde Modified
Library
Project
Transcript
//
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//
Loading project proc
ModelSim>
Project : p
Project tab

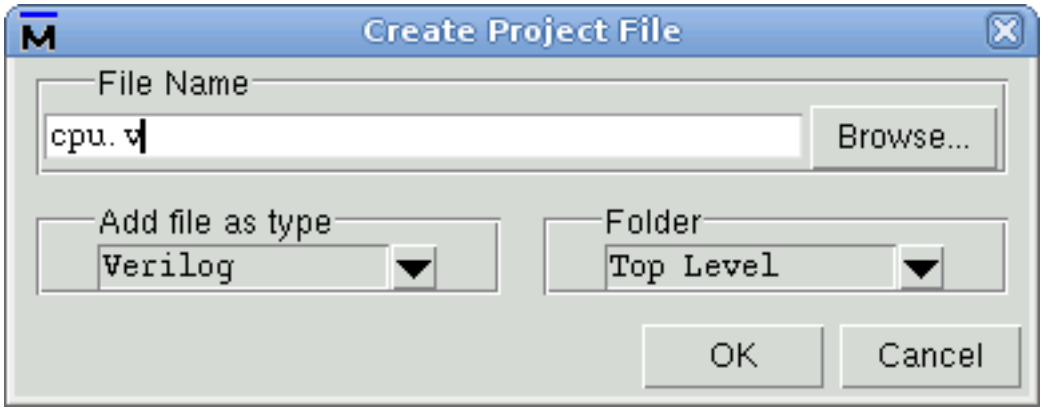
Add files to your project

- To add verilog files to the project:

  - right-click in your project tab

  - click “Add to project” → “new File”

- Chose the type “Verilog”
- Type your new file name, e.g. “cpu.v”
- → click OK



How to start coding

- Start simple:
  - cpu.v (dummy with
    - clock input
    - 1 input, 1 output
    - Make a short-circuit between input and output
- Make a testbench
  - testbench.v
  - instantiate the cpu module
  - Drive its ports

How to compile

1. Rule: compile often! (to check your syntax)

* Go to your “project” tab.
* Right-click on your verilog file (testbench.v).
* Click on either of the “compile” commands.
* Try “compile order”. It will try to compile everything at once.

Compilation Messages

- # Compile of cpu.v failed with 1 errors.
- Right-click on the message and a pop-up will tell you what's wrong.

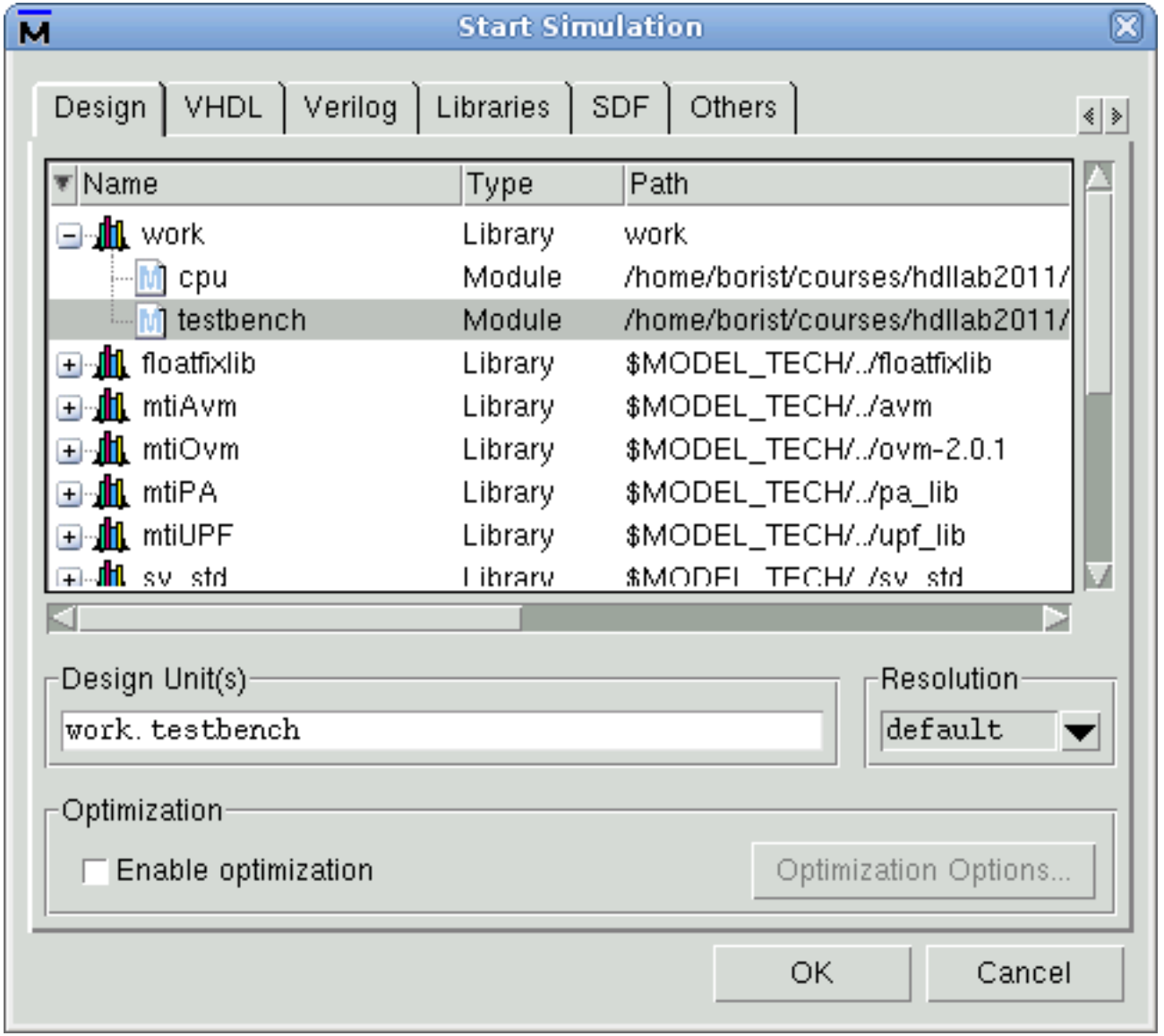
- # Compile of cpu.v was successful.

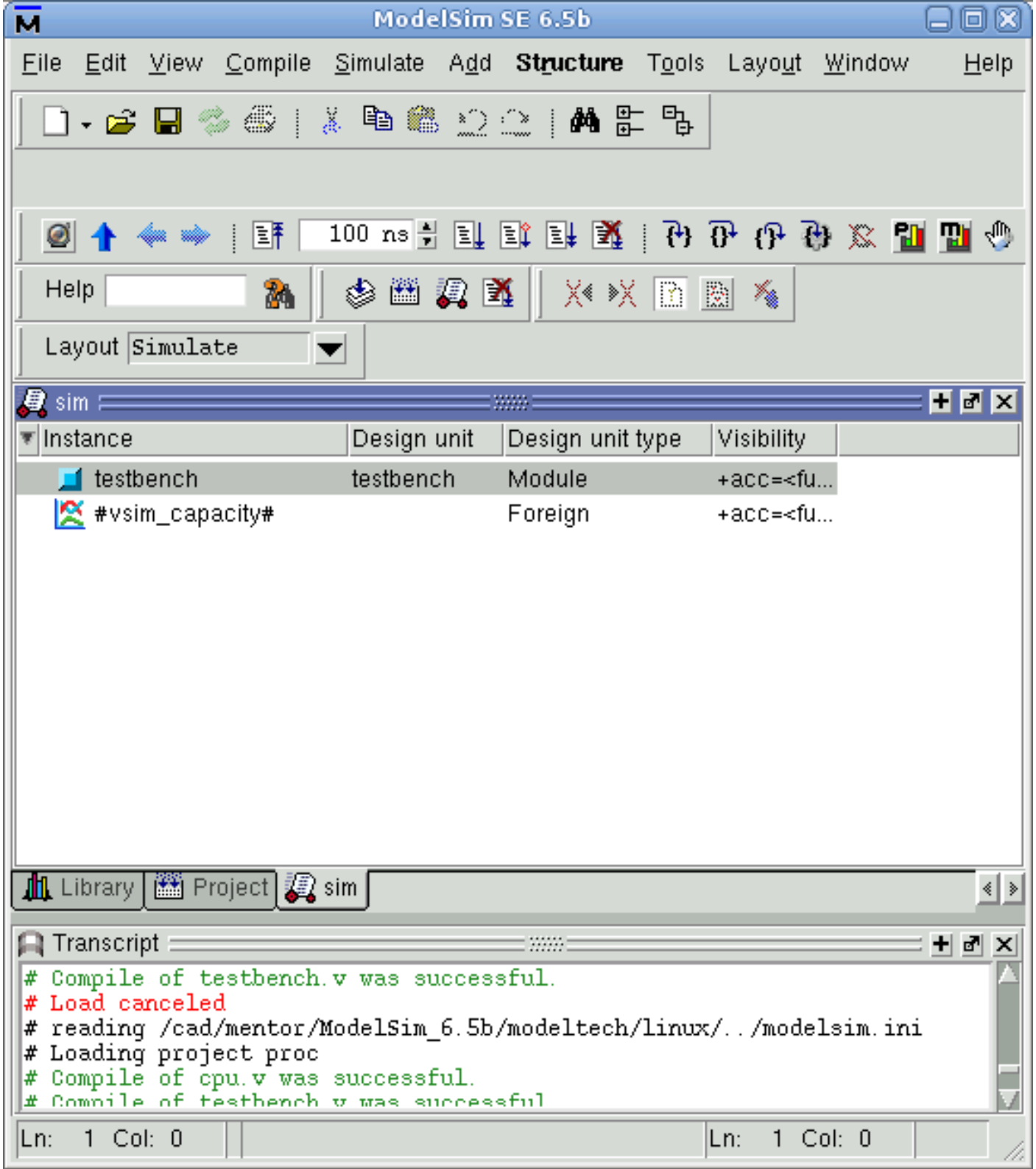
  :-)

How to Simulate

* Click on “Simulate” in the menu bar.

- Chose your testbench
- Disable optimizations!




ModelSim SE 6.5b
File Edit View Compile Simulate Add Structure Tools Layout Window Help
100 ns
Help
Layout Simulate
sim
Instance Design unit Design unit type Visibility
testbench testbench Module +acc=<fu...
#vsim_capacity# Foreign +acc=<fu...
Library Project sim
Transcript
Compile of testbench.v was successful.
Load canceled
reading /cad/mentor/ModelSim_6.5b/modeltech/linux/../modelsim.ini
Loading project proc
Compile of cpu.v was successful.
Ln: 1 Col: 0
Ln: 1 Col: 0

How to Simulate (2)

- In the new “sim” tab (next to the project tab):
- Right-click on the testbench → “add to wave” → “all items in region”.
- Then click on run!
- Use “stop simulation” to return to your code and fix errors.

How to simulate (3)

- Take a deep breath and repeat!

- Hints:
  - Take a close look at the GUI and its buttons!
  - Save often!
  - Backup before lunch and before leaving!
  - Communicate with your team members!