Design Rules Verification Report

Filename : C:\Users\gharris\projects\keyboard\pokey\brain\3u.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=8mil) (InPolygon),(All)	0
Clearance Constraint (Gap=6mil) (InPolygon and (ontop or OnBottom)),(All)	0
Clearance Constraint (Gap=15mil) (IsElectrical),(IsBoardOutline)	0
Clearance Constraint (Gap=0mil) (InComponent('M7.1') or InComponent('M1.1') or	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=5mil) (Max=150mil) (Preferred=5mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air	0
Hole Size Constraint (Min=1mil) (Max=250mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (OnLayer('Top Overlay') or OnLayer('Bottom Overlay'))	0
Permitted Layers - (Top Layer, Bottom Layer) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0