Getting Started With SHARC® Processors

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ANALOG DEVICES

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PREFACE

Thank you for your interest in the SHARC® family of processors from Analog Devices.

Purpose of This Manual

Getting Started With SHARC Processors provides you with information about the evaluation process, Analog Devices tools, training, documentation, and other informational resources to assist you in the evaluation of SHARC processors. This manual describes the resources available to help you evaluate and design the SHARC processors into your final system.

For engineers already using SHARC processors in their designs, this guide provides resources and pointers to help transition your system to take advantage of the newest generation of processors. For detailed descriptions of processor internal architectures, refer to the applicable hardware reference manual. For detailed descriptions of processor software, refer to applicable instruction set reference or programming manuals. A complete list of documents that support your product can be found in the Preface of each hardware or software manual.

Intended Audience

The primary audiences for this guide are system designers, programmers, and hardware engineers who want to learn whether a specific SHARC processor matches design requirements for new applications.

Manual Contents

This manual consists of:

- Chapter 1, "Introduction to SHARC Processors"
  This chapter briefly describes the processor architecture, available models, and processor features.
- Chapter 2, "The Evaluation Process"
  This chapter focuses on available software and hardware tools.
- Chapter 3, "Support Options"
  This chapter describes support (documentation, training, and more) available during the evaluation and development processes.
- Appendix A, "Benchmarking Processors"
  This appendix provides SHARC benchmarking data compiled by Berkeley Design Technology Incorporated (BDTI), a company that specializes in impartial evaluations of processor performance.

Supported SHARC Processors

The following Analog Devices SHARC processors are supported in VisualDSP++® 4.5.

The name "SHARC" refers to a family of high-performance, 32-bit, floating-point processors that can be used in speech, sound, graphics, and imaging applications. VisualDSP++ currently supports the following SHARC processors:

ADSP-21020	ADSP-21060	ADSP-21061	ADSP-21062
ADSP-21065L	ADSP-21160	ADSP-21161	ADSP-21261
ADSP-21262	ADSP-21266	ADSP-21362	ADSP-21363

ADSP-21364	ADSP-21365	ADSP-21366	ADSP-21367
ADSP-21368	ADSP-21369	ADSP-21371	ADSP-21375

The list of supported SHARC processors is subject to change. For a complete and up-to-date listing of SHARC processors refer to:

http://www.analog.com/processors/sharc/

Product Information

You can obtain product information from the Analog Devices Web site, from the product CD-ROM, or from printed publications (manuals).

Analog Devices is online at http://www.analog.com. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and embedded processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Be sure to enable the weekly automatic notification feature. These mailings are especially important as they notify you of processor anomalies and errata.

Registration

Visit http://www.myanalog.com to sign up. Click **Register** to use http://www.MyAnalog.com. Registration takes about five minutes and serves as a means to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at http://www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)
- Fax questions or requests for information to
  1-781-461-3010 (North America)
  +49-89-76903-157 (Europe)
- Access the FTP Web site at
  ftp://ftp.analog.com
- Access processor technical support, including a comprehensive , searchable knowledgebase at
  http://www.analog.com/processors/technicalSupport/index.html

Related Documents

For information on product related development software, see these publications:

- *VisualDSP++ 4.5 Getting Started Guide*
- *VisualDSP++ 4.5 User's Guide*
- *VisualDSP++ 4.5 Run-Time Library Manual for SHARC Processors*
- *VisualDSP++ 4.5 C/C++ Compiler Manual for SHARC Processors*
- *VisualDSP++ 4.5 Assembler and Preprocessor Manual*
- *VisualDSP++ 4.5 Product Release Bulletin*
- *VisualDSP++ Kernel (VDK) User's Guide*
- *Quick Installation Reference Card*

For hardware information, refer to your processor's hardware reference, programming reference, and data sheet. All documentation is available online. Most documentation is available in printed form.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

`http://www.analog.com/processors/manuals`.

Online Technical Documentation

Online documentation includes the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the

entire VisualDSP++ documentation set for any topic of interest using the **Search** function of the VisualDSP++ Help system. For easy printing, supplementary `.PDF` files of most manuals are also provided.

Each documentation file type is described as follows.

File	Description
`.chm`	Help system files and manuals in Help format
`.htm` or `.html`	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the `.HTML` files requires a browser, such as Internet Explorer 6.0 (or higher).
`.pdf`	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the `.pdf` files requires a PDF reader, such as Adobe Acrobat Reader (5.0 or higher).

Access the online documentation from the VisualDSP++ environment, Windows® Explorer, or the Analog Devices Web site.

Accessing Documentation From VisualDSP++

From the VisualDSP++ environment:

- Access VisualDSP++ online Help from the Help menu's **Contents**, **Search**, and **Index** commands.
- Open online Help from context-sensitive user interface items (toolbar buttons, menu commands, and windows).

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (.chm) are located in the Help folder of the VisualDSP++ environment. The .pdf files are located in the Docs folder of your VisualDSP++ installation CD-ROM. The Docs folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Using Windows Explorer

- Double-click the vdsp-help.chm file, which is the master Help system, to access all the other .chm files.
- Open your VisualDSP++ installation CD-ROM and double-click any file that is part of the VisualDSP++ documentation set.

Using the Windows Start Button

- Access VisualDSP++ online Help by clicking the **Start** button and choosing **Programs**, **Analog Devices**, **VisualDSP++**, and **VisualDSP++ Documentation**.
- Access the .pdf files by clicking the **Start** button and choosing **Programs**, **Analog Devices**, **VisualDSP++4.5**, **Documentation for Printing** and the name of the book.

Accessing Documentation From the Web

Download manuals in PDF format at the following Web site:

http://www.analog.com/processors/manuals.

Select a processor family and book title. Download archive (.zip) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call **1-603-883-2430**. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto:

http://www.analog.com/salesdir/.

Hardware Tools Manuals

To purchase EZ-KIT Lite® and In-Circuit Emulator (ICE) manuals, call **1-603-883-2430**. The manuals may be ordered by title or by product number located on the back cover of each manual.

Processor Manuals

Hardware reference and programming reference manuals may be ordered through the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**), or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.

Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD** (**1-800-262-5643**); they also can be downloaded from the Web site.

To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

1 INTRODUCTION TO SHARC PROCESSORS

This chapter briefly describes the SHARC processor's architecture and key features and compares available models.

Topics include:

What are SHARC Processors?

SHARC is the name of a family of high-performance 32-bit floating-point processors based on a Super Harvard Architecture. SHARC processors dominate the floating-point digital signal processing market, delivering exceptional core and memory performance complemented by outstanding I/O throughput. The industry standard SHARC family makes floating-point processing economical for applications where performance and dynamic range are key considerations such as home, professional, and automotive audio, medical, and industrial and instrumentation products.

The SHARC processor portfolio currently consists of three generations of products providing code-compatible solutions, ranging from entry-level products priced at less than $10 to the highest performance products offering fixed- and floating-point computational power to 400 MHz/2400 MFLOPs. Regardless of the specific product choice, all SHARC processors provide a common set of features and functionality usable across many signal processing markets and applications. This baseline functionality

enables the SHARC user to leverage legacy code and design experience, while transitioning to higher-performance, more highly integrated SHARC products.

By integrating on-chip, single-instruction, multiple-data (SIMD) processing elements, SDRAM, and I/O peripherals, SHARC processors deliver breakthrough signal processing performance.

SHARC Applications

The combination of a high performance core surrounded by appropriate peripherals, a large software library, and award-winning development tools makes SHARC processors the ideal choice for audio and broad market processor applications. Here are some applications:

- **Home theater/digital home applications.** The ADSP-21266, ADSP-21365/6, and ADSP-21367 processors permit highly efficient software implementations of audio decode and postprocessing algorithms, such as Dolby Digital, Dolby Digital EX, DTS-ES Discrete 6.1, DTS-ESMatrix 6.1, DTS 96/24™ 5.1, MPEG-2 AAC LC, MPEG-2 BC 2ch, Dolby Pro Logic II, Dolby Pro Logic 2x, DTS Neo:6, and WMA Pro. Libraries of all standard–and many proprietary–audio algorithms reside in on-chip ROM, eliminating the need for external ROM.
- **Professional audio applications.** A number of the third-generation SHARC processors are well-suited for professional audio applications requiring high processing power and advanced on-chip peripherals such as sample rate conversion, S/PDIF transmitter/receiver, and BGA and LQFP package options.

- **Automotive audio applications.** The ADSP-2136x, with integration of sample-rate conversion, DTCP cipher, precision clock generators, and serial ports, is an ideal choice for new multichannel automotive audio designs.
- **Broad market use.** SHARC processors are available in commercial, industrial, and automotive temperature grade packages. They are used in a wide variety of signal processing applications, providing up to 400 MHz performance in a single instruction, multiple data architecture (SIMD). Applications include imaging, medical devices, communications, military, test equipment, 3-D graphics, speech recognition, and motor control.

Architecture Overview

This section describes architectural features of the SHARC processor.

Super Harvard Architecture

The 32-bit floating-point SHARC processors from Analog Devices are based on a Super Harvard architecture that balances exceptional core and memory performance with outstanding I/O throughput capabilities. This architecture extends the original concepts of separate program and data memory busses by adding an I/O processor with its associated dedicated busses.

In addition to satisfying the demands of the most computationally intensive, real-time signal processing applications, SHARC processors integrate large memory arrays and application-specific peripherals designed to simplify product development and reduce time to market.

Common Architectural Features

SHARC processors share the following architectural features.

- 32/40-bit IEEE floating-point math
- 32-bit fixed-point multipliers with 64-bit product and 80-bit accumulation
- No arithmetic pipeline. All computations are single-cycle.
- Circular buffer addressing supported in hardware
- Sixteen address pointers support 16 circular buffers.
- Six nested levels of zero-overhead looping in hardware
- Rich algebraic assembly language syntax
- Conditional arithmetic, bit manipulation, divide and square root, bit field deposit and extract supported by instruction set
- Zero-overhead background transfers at full clock rate without processor intervention

In the core, every instruction can execute in a single cycle. The buses and instruction cache provide rapid unimpeded data flow to the core to maintain the execution rate.

Figure 1-1 on page 1-6 shows a detailed block diagram of a single core SHARC 32-bit processor and the I/O processor (IOP). It illustrates the following architectural features:

- Two processing elements (PEx and PEy), each containing 32-bit IEEE floating-point computation units–multiplier, arithmetic logic unit (ALU), shifter, and data register file
- Program sequencer with related instruction cache, interval timer, and data address generators (DAG1 and DAG2)

- An SDRAM controller that provides an interface to as many as four separate banks of industry-standard SDRAM devices
- Up to a maximum of 4 Mbits of on-chip SRAM and 6 Mbits of on-chip, mask-programmable ROM
- Input/output processor (IOP) with integrated direct memory access (DMA) controller, serial peripheral interface (SPI) compatible port, and serial ports (SPORTs) for point-to-point multiprocessor communications
- A variety of audio-centric peripheral modules including a Sony/Philips digital interface (S/PDIF), sample rate converter (SRC), and pulse width modulation (PWM). Table 1-1 on page 1-6 provides details on these and other features for the current members of the ADSP-2136x processor generation.
- JTAG test access port for emulation

Figure 1-1 also shows the three on-chip buses of the ADSP-21367/8/9 processors: the PM bus, DM bus, and I/O bus. The PM bus provides access to instructions or data. During a single cycle, these buses let the processor access two data operands from memory, access an instruction (from cache), and perform a DMA transfer. In addition, Figure 1-1 shows the asychronous memory interface available on the ADSP-21368 processor.

Three Generations of SHARC Processors

The SHARC architecture has a long history in the floating-point processor market. While architectural enhancements have been made with each successive processor generation, the common traits of exceptional floating-point performance, matched to high-bandwidth memory and I/O transfers, remains. All three generations of SHARC processors are still in production, offering a variety of code-compatible options to meet a wide array of price, performance, and footprint requirements.

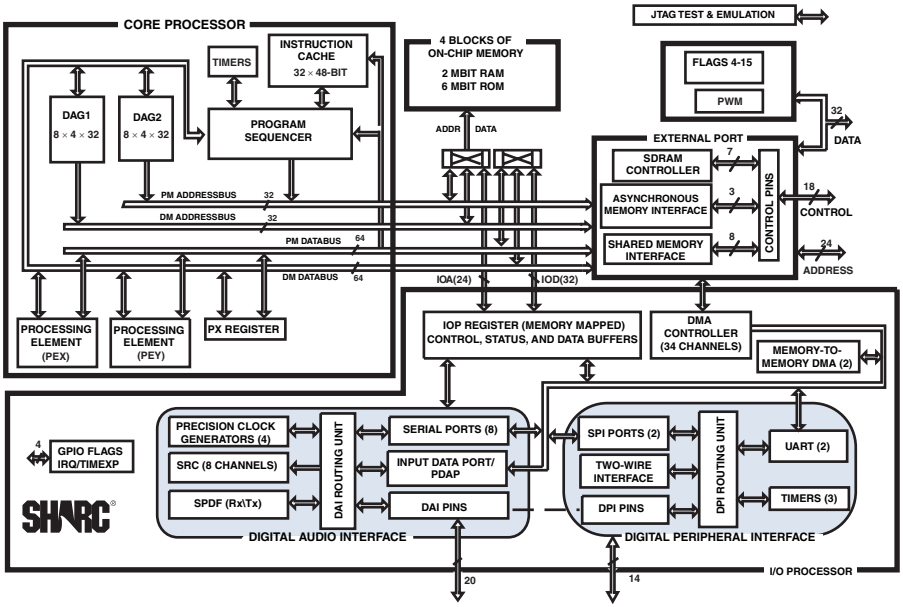

Figure 1-1. ADSP-21368 Block Diagram

First-generation SHARC products offer performance of up to 66MHz/198 MFLOPS and form the cornerstone of the SHARC processor family. Their easy-to-use instruction set architecture that supports both 32-bit fixed-point and 32/40-bit floating-point data formats, combined with large memory arrays and sophisticated communications ports, make them suitable for a wide array of parallel processing applications including consumer audio, medical imaging, military, industrial, and instrumentation.

Second-generation products contain dual multipliers, ALUs, shifters, and data register files, significantly increasing overall system performance in a variety of applications. This capability is especially relevant in consumer, automotive, and professional audio where the algorithms related to stereo channel processing can effectively utilize the SIMD architecture.

Third-generation SHARC products employ an enhanced SIMD architecture that extends CPU performance to 400 MHz/2400 MFLOPS. These products also integrate a variety of ROM configurations and audio-centric peripherals designed to decrease time to market and reduce the overall bill of materials costs. This increased level of performance and peripheral integration allow third-generation SHARC processors to be considered as single chip solutions for a variety of audio markets.

Each SHARC processor provides unique capabilities, while being pin-compatible with other SHARC devices. Table 1-1 on page 1-8 lists key third generation SHARC processor specifications. For more information, view the SHARC processor selection table online at the Analog Devices Web site at:

`http://www.analog.com/sharc`

Processor Peripherals and Performance

SHARC processors represent a class of devices that combine an extremely capable single-instruction, multiple-data (SIMD) processor engine with features like core timers, general purpose timers, UARTs, and SPI ports.

In addition to advanced peripherals, SHARC processors use a software programmable, on-chip phase lock loop (PLL) that allows software control during runtime of core and peripheral clock of the SHARC processors.

Performance

Real-time signal processing tasks are I/O and computationally intensive. In addition to high-speed math units and single-cycle instruction execution (including single-cycle multiply accumulates [MACs]), SHARC processors are designed for maximum I/O and memory access bandwidth. This balance of core speed, memory integration, and I/O bandwidth achieves the sustained performance critical to real-time applications.

Table 1-1. Third Generation SHARC Processor Specifications

	ADSP-21261	ADSP-21262	ADSP-21266	ADSP-21362	ADSP-21363	ADSP-21364	ADSP-21365	ADSP-21366	ADSP-21367	ADSP-21368	ADSP-21369	ADSP-21371	ADSP-21375
Frequency (MHz)	150	200	200	333	333	333	333	333	266 333 400	333 400	266 333 400	266	266
On-Chip RAM	1Mbit	2Mbit	2Mbit	3Mbit	3Mbit	3Mbit	3Mbit	3Mbit	2Mbit	2Mbit	2Mbit	1Mbit	0.5Mbit
On-Chip ROM	3Mbit	4Mbit	4Mbit	4Mbit	4Mbit	4Mbit	4Mbit	4Mbit	6Mbit	6Mbit	6Mbit	4Mbit	2Mbit
SRC	0	0	0	-128dB	0	-140dB	-128dB	**-128dB**	-128dB	-140dB	-128dB	0	0
PWM	0	0	0	1	1	1	1	1	1	1	1	1	1
UART	0	0	0	1	1	1	1	1	2	2	2	1	1
SPI	1	1	1	2	2	2	1	1	2	2	2	2	2
SPDIF	0	0	0	1	1	1	1	1	1	1	1	1	0
TWI	0	0	0	0	0	0	0	0	1	1	1	1	1
Timer	3	3	3	3	3	3	3	3	3	3	3	2	2
SPORT	4	6	6	6	6	6	6	6	8	8	8	8	4
SRU	1	1	1	1	1	1	1	1	1	1	1	1	1
DTCP	0	0	0	1	0	0	1	1	0	0	0	0	0
PCG	2	2	2	2	2	2	2	2	4	4	4	4	4
Temp. Grade	-40-85°	-40-85°	-40-105°C	-40-85°	-40-105°C	-40-105°C	-40-85°	-40-85°	-40-85°	-40-85°	-40-85°	0-70°C	0-70°C
Execution from Ext. Memory?	No	No	No	No	No	No	No	No	No	No	No	Yes	Yes

2 THE EVALUATION PROCESS

This chapter describes the available software and hardware tools needed to evaluate SHARC processors and develop application programs.

This chapter introduces the software and hardware evaluation tools that are currently available, including:

Evaluation Tools

This section examines the process through which SHARC processor applications are developed. Various tools are used at each stage. Typical application development occurs over multiple stages.

Most users acquire a set of *software development tools* first. The software development tools run on a PC and provide code generation and debug utilities such as a compiler, assembler, linker, simulator, debugger, and libraries. For information on selecting appropriate software, see "Selecting Software Development Tools" on page 2-2.

Optionally, users acquire a *hardware tool* to begin testing the application on a SHARC processor. Development boards typically provide expansion headers, allowing you to prototype basic hardware without customized user hardware.

"Selecting Software Development Tools" provides a summary of the available software development tools for SHARC processors. Most development tools available for SHARC processors provide a cycle accurate simulator which can develop initial algorithms and applications without the actual hardware.

Selecting Software Development Tools

Because SHARC processors are programmable, software development tools are required to author software applications. Typical software development tools include a C/C++ compiler, run-time libraries, assembler, and linker. Emulation, simulation, debugging, and project management capabilities vary, based on the tools vendor. The process of selecting tools is shown in Figure 2-1 on page 2-3.

Currently, one set of software development tools is available for the SHARC processor architecture: VisualDSP++ 4.5 from Analog Devices.

This document focuses on the Analog Devices VisualDSP++ tool chain, which is the most popular set of tools and provides the best starting point for new users.

Other software development tools are available in languages such as Japanese and Chinese. Contact your local Analog Devices sales office or distributor for more information.

VisualDSP++ From Analog Devices

VisualDSP++ is an easy-to-install and easy-to-use integrated software development and debugging environment (IDDE) that enables efficient management of projects from start to finish from within a single interface.

Because project development and debugging is integrated, you can move quickly and easily between editing, building, and debugging activities. Key features include the native C/C++ compiler, advanced graphical plotting tools, statistical profiling, and the VisualDSP++ Kernel (VDK),

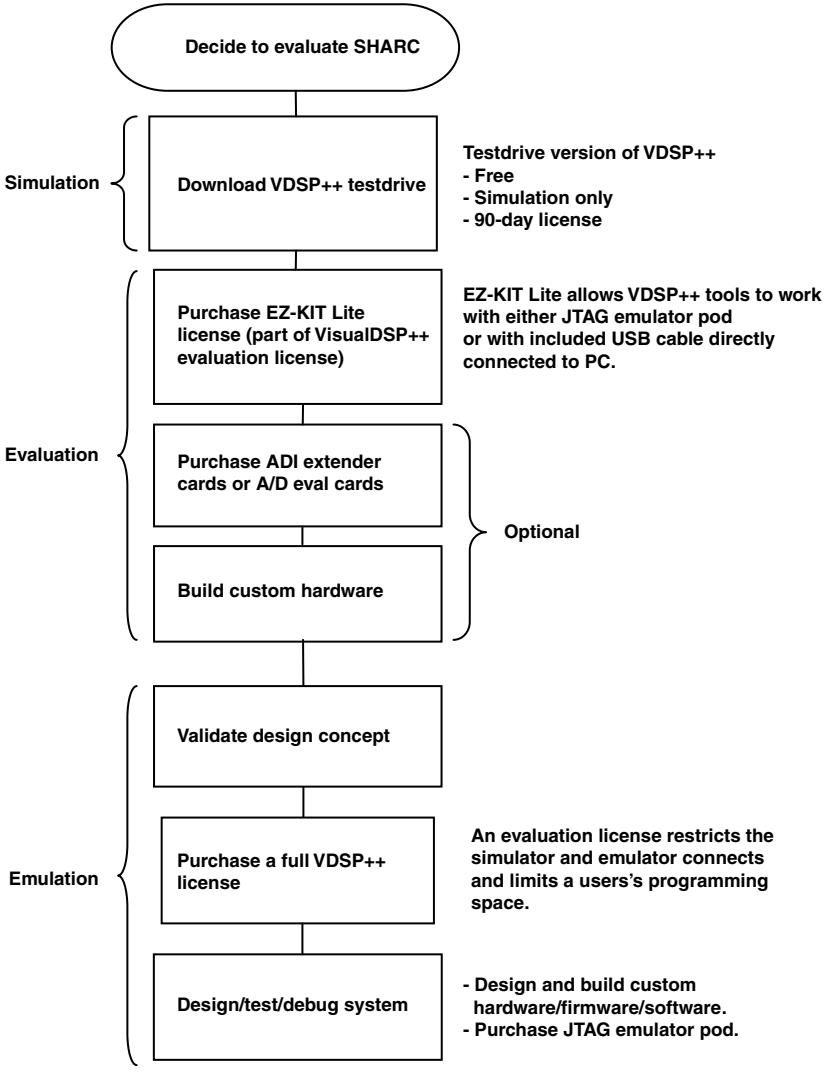

Figure 2-1. Tool Selection Workflow

which allows a user's code to be implemented in a more structured and easier to scale manner. Other features include assembler, linker, libraries, loader, splitter, cycle-accurate and functional-accurate compiled simulators, emulator support, and more. VisualDSP++ offers programmers a powerful yet easy-to-use programming tool with flexibility that significantly reduces the time to market.

Platform and Processor Support

VisualDSP++ supports SHARC processors on Windows® 2000 and Windows® XP. Windows® Vista, Windows® XP and Windows 2000 hosts are also supported.

Develop High-Performance Applications Quickly

At the heart of VisualDSP++ is a robust and powerful C/C++ compiler. The compiler consistently delivers industry-leading performance on standard benchmarks, ensuring that all but the most performance-demanding applications can be written entirely in the C language, accelerating development time while maintaining a portable code base. The compiler is backed by a rich library of signal processing routines, allowing easy access to hand-coded, optimized implementations of FFTs, FIRs, and so forth.

The ANSI-C compiler is also augmented with popular language extensions and enhancements to make it more amiable to existing code bases. Examples include GNU GCC extensions and multiple heap support.

A compiler's mission is to produce correct code, so there are occasions when the compiler must take a conservative approach to a code sequence when a more aggressive approach could have been taken if certain constraints could be guaranteed by the programmer. The VisualDSP++ compiler supports a broad range of pragmas that allow the programmer to better exploit the compiler while maintaining C language neutrality. Just as important, the compiler has the ability to feed back advisory information to the programmer, offering further improvements to a code sequence, should the programmer be able to make certain guarantees

about it. This information is displayed seamlessly in the VisualDSP++ main editor window. This removes the black box label that compilers sometimes have.

Backing the compiler is a powerful assembler and linker technology. Processors from Analog Devices are noted for their intuitive algebraic assembly language syntax, and the VisualDSP++ assembler extends that ease of use with the ability to import C header files, allowing for symbolic references into arbitrarily complex C data structures. Binary data can be included directly into assembly source files, creating an easy way to add blocks of static data (such as audio samples and bitmaps) to an application. The VisualDSP++ linker is fully multicore and multiprocessor (MP) aware, allowing for the creation of cross-linked, multiexecutable applications in a single pass. Other powerful capabilities of the linker include dead code and data elimination, code and data overlays, and section spilling (for example, automatic overflow from internal to external memory).

Leverage-Proven Application Infrastructure

VisualDSP++ goes beyond robust code generation tools, providing considerable application infrastructure and middleware out of the box to speed application development.

The VisualDSP++ kernel (VDK) is a robust, royalty-free, real-time operating system (RTOS) kernel. This pre-emptive multitasking kernel incorporates state-of-the-art scheduling and resource allocation techniques tailored specifically for the memory and timing constraints of DSP programming. The kernel facilitates development of performance-structured applications using frameworks of template files. It provides essential kernel features in a minimal footprint. Features include a fully pre-emptive scheduler (time slicing and cooperative scheduling are also supported), thread creation, semaphores, interrupt management, inter-thread messaging, events, and memory management (memory pools and multiple heaps). In MP environments, MP messaging is also provided. Configuration of these elements is done graphically, with code wizards to speed the

creation of new threads and interrupt handlers. VDK has been available for multiple releases of VisualDSP++ and is now a key component of products shipping from a number of high-volume vendors.

As embedded applications become increasingly part of the connected world, the ability to rapidly add reliable USB connectivity to an application can often make or break a development schedule. For SHARC processors, USB 2.0 device connectivity is provided via an EZ-Extender card for the EZ-KIT Lite. (See "SHARC USB EZ-Extender" on page 2-27.) USB data is sent using the SHARC external port. Bulk and asynchronous transfer modes are supported out of the box, with USB-IF logo-certified embedded and host applications provided with full source code.

VisualDSP++ uses incremental builds, multiple build configurations ("Debug" and "Release," for example), a syntax-coloring editor, and many other code editing features. Makefiles can be imported and exported freely.

Debug and Tune Your Application with Ease

The ability to develop a high-performance application is often gated by the visibility into your running system that your debugger provides. VisualDSP++ excels in this regard, with best-in-class debugging and inspection support. Robust fundamental C language source debugging (source-level stepping and breakpoints, stack unwinds, local variable and C expression support, memory and register windows) serves as a foundation upon which multiple innovative and unique tools rest.

VisualDSP++ supports a variety of debugging targets. Most common is a JTAG connection to an EZ-KIT Lite board or to a custom target board by means of Analog Devices emulator products. However, there will be occasions where closer inspection in a simulated environment may be required. VisualDSP++ provides core cycle-accurate simulators, allowing inspection of every nuance of activity within the processor, including visualization of the processor's pipeline and cache.

As many of the most performance-demanding applications process a signal of some sort, comprehensive memory plotting is a corner stone of VisualDSP++ debugger support. VisualDSP++ provides multiple views, from basic (line plots) to sophisticated (eye diagrams and waterfalls) to pinpoint anomalous data sequences in your application. Image viewing in a number of data formats is also available.

VDK users get unparalleled visibility into the internals of the kernel. Status on a per-thread basis is available, as is a comprehensive pictorial history of kernel events and CPU loading. Thread changes, posted and pended semaphores, and other kernel events are captured in this display.

Inspection, or even application stimulation, from the debugger at run-time is possible through the use of the processor's background telemetry channels (BTCs). BTC allows for an arbitrary number of communication channels to be established between the host debugger and the application. Channels may go in either direction, so BTC can be used to read and write data as the processor runs. Scalar values or entire arrays may be serviced by a channel. Arrays read from the target can even be plotted in real time.

Multiprocessor users get the same compelling set of debugging features across all processors, unified into a single debugging interface. Individual windows can be made to "float" their focus to whichever processor currently is the debugger's focus, or they can be "pinned" to a specific processor so their contents do not follow the debugger's focus. To further aid MP debug, synchronous run, step, halt, and reset are also provided.

The patented statistical profiler from Analog Devices offers unprecedented and unique visibility into a running application. Operating completely non-intrusively to the application, the application is polled thousands of times per second and a statistical view of where an application is spending the majority of its time is quickly assembled. This tool can be used to easily inspect an application for unexpected hotspots (for example, suggesting the need to move a key routine from external to internal memory). Simulator targets provide a completely linear profiling view.

Going even further, the VisualDSP++ compiler is able to act upon profiling information. Profile-guided optimization (PGO) is a technique that allows the compiler to instrument an application, run the application, and then make a second pass compilation, exploiting the information that was gathered during the previous run of the application. This gives the compiler unique insight on a block-by-block basis, allowing it to optimize with a level of granularity that is not possible with a tool that operates only on a file-by-file basis.

Integrate Into Your Existing Environment

A development tool suite is always a part of an organization's larger software engineering environment. VisualDSP++ has been designed to operate in a larger environment.

Since an embedded engineer is often developing on a new platform while maintaining existing products that were likely developed with an earlier version of the tools, VisualDSP++ can be installed discretely an arbitrary number of times at a variety of release levels, allowing engineering to easily switch between current and legacy versions of VisualDSP++.

To better integrate to source code control (SCC) systems, VisualDSP++ is able to connect to any SCC provider that supports the Microsoft® common source code control (MCSCC) interface. This interface is supported by all leading SCC vendors. VisualDSP++ goes one step further by supporting the control of VisualDSP++ itself within a source code control system.

The ability to robustly test an embedded application is enabled through a comprehensive automation application programming interface (API). Using Microsoft's language-neutral automation technology, nearly every feature of the graphical environment is available to script authors. Applications can be rebuilt, downloaded, and run from a simple script executed from the command-line or from within a custom test harness framework. The automation API is supported by C++ and VBScript examples for all API calls, though any automation-aware language can be used.

For prototype runs and/or small volume deployment, an Analog Devices emulator can be used to program the flash memory in your custom system. Accessible through the automation API, the flash programmer can be scripted, making it possible to develop a turnkey user interface for use by a production floor technician or other individual not familiar with VisualDSP++. Device drivers are provided for all flash devices found on EZ-KIT Lite products, and these drivers can be easily adjusted to support an arbitrary flash device.

Getting Help and Staying Up to Date

VisualDSP++ includes a comprehensive, indexed, searchable online Help system. In addition to information concerning VisualDSP++, manuals for Analog Devices processors, application notes, and more are included in the Help system. Versions of these documents (in `.pdf` format) are also available on the installation CD or online at:

`http://www.analog.com/processors`

Licensed users of VisualDSP++ are entitled to free technical support. The support staff is dedicated to VisualDSP++ and has specific expertise regarding it. There is never a per-incident or maintenance fee; support remains free regardless of how long you have owned your software.

Major and minor upgrades and updates to VisualDSP++ are also free and are released through the Analog Devices Web site.

The Collaborative

The VisualDSP++ environment enables independent third-party companies to add value using the published set of application programming interfaces (APIs) from Analog Devices. The Collaborative™ is an independent network of third-party developers. The Collaborative product offerings (real-time operating systems, emulators, high-level language

compilers, and multiprocessor hardware) can interface seamlessly with VisualDSP++, thereby simplifying development across all platforms and targets.

Take a VisualDSP++ Test Drive!

Take a free 90-day test drive of VisualDSP++. To take a test drive, you can download a test drive or request a CD from the Analog Devices DSP Tools Web site at: http://www.analog.com/processors/tools/testdrive or contact your local Analog Devices sales representative/distributor.

Analog Devices Tools Product Line

CrossCore®, the development tools product line from Analog Devices, provides easier and more robust methods for engineers to develop and optimize systems by shortening product development cycles for faster time to market. The CrossCore components include the VisualDSP++ software development environment, EZ-KIT Lite evaluation systems, EZ-Extender daughter boards, and emulators for rapid on-chip debugging. For more information on development tools, visit the Analog Devices Web site:

http://www.analog.com/processors/tools

Table 2-1 provides information about SHARC processor evaluation kits. For additional information, visit the following Analog Web site:

http://www.analog.com/processors/sharc

Embedded Processors and DSPs

Analog Devices is a leading supplier of embedded and digital signal processing solutions, and its low-cost SHARC processors and integrated mixed-signal processors are ideal for an ever-increasing spectrum of applications. Advances in design by Analog Devices provide faster processing, more memory, lower power consumption, and simplified system

Table 2-1. SHARC Processor Evaluation Kits

Processor	Evaluation Kit/Reference Board	Daughter Board
ADSP-21261 ADSP-21262 ADSP-21266	21262 EZ-KIT Lite Desktop Evaluation Board	- EZ-Extender Daughter Board - USB EZ-Extender Daughter Board
ADSP-21363 ADSP-21364 ADSP-21365 ADSP-21366	21364 EZ-KIT Lite Desktop Evaluation Board	- EZ-Extender Daughter Board - USB EZ-Extender Daughter Board
ADSP-21367 ADSP-21368 ADSP-21369	21369 EZ-KIT Lite Desktop Evaluation Board	- USB EZ-Extender Daughter Board
ADSP-21371 ADSP-21375	21375 EZ-KIT Lite Desktop Evaluation Board	- USB EZ-Extender Daughter Board

integration. Analog Devices products and technology provide a competitive edge complete with expert technical support, comprehensive development tools, and The Collaborative.

Software Modules

Analog Devices has a wide range of tested and optimized software modules available, including decoders, encoders, codecs and other algorithms that provide multimedia functions for the Blackfin family. The software modules allow engineers to quickly and easily incorporate these functions, providing a faster development path to the end product. In addition, the highly-optimized software modules feature a consistent API and framework to ensure rapid development of multiple functions.

Selecting Hardware Development Tools

Hardware development tools include development and evaluation boards (such as EZ-KIT Lite), expansion boards, and JTAG emulators.

EZ-KIT Lite Evaluation Systems

Typically, development and evaluation boards are standalone printed circuit boards (PCBs) that contain a SHARC processor with other devices.

Analog Devices offers an evaluation system, called an EZ-KIT Lite, for each subfamily of SHARC processors. Each EZ-KIT Lite includes a board, cable, power supply, documentation, software, and a license key.

The EZ-KIT Lite board is a low-cost hardware platform that includes a SHARC processor surrounded by several other devices such as audio codecs, video encoders, video decoders, flash, SDRAM, and so on.

Each EZ-KIT Lite board also includes an on-board JTAG emulator with a USB 2.0 connector and a standard 14-pin, 100-mil, JTAG header for use with high-performance JTAG emulators available from Analog Devices. Using the processor's JTAG port and the VisualDSP++ software, you can set breakpoints, single-step through code, view memory, fill/dump memory, perform real-time data manipulation, profile execution and memory access, plot data, and use standard I/O.

EZ-KIT Lite evaluation systems include a serial number, that when registered, yields full VisualDSP++ license status for 90 days from the date of installation. After 90 days, the license changes to restricted status, which limits the size of the application that can be built and supports debug agent connectivity only. Refer to "Software Development on SHARC Processors" on page 2-39 to see where the EZ-KIT Lite fits into the phases of program development.

Most EZ-KIT Lite boards include three expansion connectors configured in the shape of a U. Several third-party expansion boards connect to the EZ-KIT Lite board via these connectors. See the "EZ-KIT Lite Expansion Boards" on page 2-24 for details.

The following sections briefly describe EZ-KIT Lite development systems that are currently available for SHARC processors.

ADSP-21262 EZ-KIT Lite From Analog Devices

Part Number: ADDS-21262-EZLITE

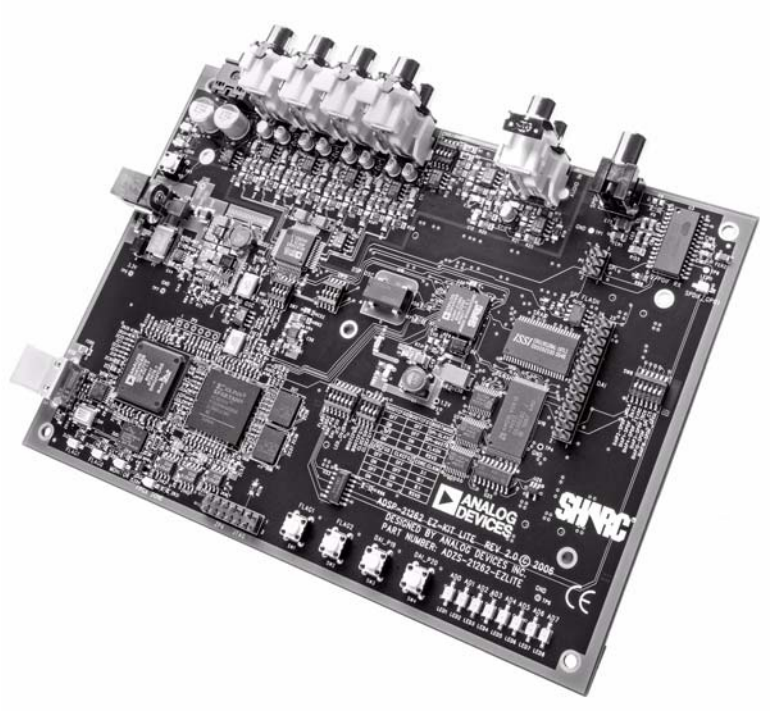

Figure 2-2. ADSP-21262 EZ-KIT Lite Evaluation System

The ADSP-21262 EZ-KIT Lite evaluation system, as shown in Figure 2-2, provides developers with a cost-effective method for initial evaluation of the ADSP-21261/21262/21266 SHARC processors for a wide range of applications.

The ADSP-21262 EZ-KIT Lite evaluation system includes an ADSP-21262 SHARC processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a

USB-based PC-hosted tool set. With this EZ-KIT Lite, you can learn more about Analog Devices ADSP-21262 SHARC processor hardware and software development and prototype applications. The EZ-KIT Lite provides an evaluation suite of the VisualDSP++ integrated development and debug environment (IDDE) with the C/C++ compiler, advanced plotting tools, statistical profiling, and the VisualDSP++ kernel (VDK). Other features include: assembler, linker, libraries, loader, and splitter. VisualDSP++ offers programmers a powerful programming tool with flexibility that shortens time to market.

Features

- ADSP-21262 SHARC processor
- 1M x 8-bit flash memory
- 512K x 8-bit SRAM
- 2 Mbit SPI® flash memory
- AD1835 stereo, 96-kHz, 24-bit codec
- 4 x 2 RCA jack for four channels of stereo audio output
- 1 x 2 RCA jack for one channel of stereo audio input
- Headphone jack (connected to one of the stereo outputs)
- SPDIF receiver with RCA jack
- USB interface
- JTAG ICE 14-pin header
- Evaluation suite of VisualDSP++ development tools
- 0-ohm resistor for current measurement
- Flash programmer utility for downloading boot code to on-board flash memory

- Type A expansion interface with three connectors supporting parallel port, FLAG, SPI, and DAI interfaces
- Twelve LEDs: one power (green), one board reset (red), S/PDIF (amber), one USB monitor (amber), and eight general-purpose (amber)
- Five push buttons: one reset, two general-purpose input (connected to DAI), and two IRQs (connected to flag pins)
- USB cable
- CE certified

The ADSP-21261/2/6 SHARC processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the ADSP-21262 SHARC processor. Thus, this EZ-KIT Lite evaluation system may be used for any of these devices.

ADSP-21364 EZ-KIT Lite From Analog Devices

Part Number: ADDS-21364-EZLITE

Figure 2-3. ADSP-21364 EZ-KIT Lite Board

The ADSP-21364 EZ-KIT Lite evaluation system, as shown in Figure 2-3, provides developers with a cost-effective method for initial evaluation of ADSP-21364/3/5/6 SHARC processors.

The EZ-KIT Lite includes an ADSP-21364 SHARC processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based PC-hosted tool set. With this EZ-KIT Lite, users can learn more about ADSP-21363/21364/21365/21366

SHARC processor hardware and software development and prototype applications. The ADSP-21364 EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, loader, and linker. All software tools are limited to use with the EZ-KIT Lite.

Features

- ADSP-21364 SHARC processor
- 1M x 8-bit flash memory
- 512K x 8-bit SRAM
- 2 Mbit SPI® flash memory
- AD1835 stereo, 96-kHz, 24-bit codec
- 4 x 2 RCA jack for four channels of stereo audio output
- 1 x 2 RCA jack for one channel of stereo audio input
- Headphone jack (connected to one of the stereo outputs)
- SPDIF In RCA jack
- SPDIF Out RCA jack
- USB interface
- JTAG ICE 14-pin header
- Evaluation suite of VisualDSP++ development tools
- Flash programmer utility for downloading boot code to on-board flash memory
- Type A expansion interface with three connectors supporting parallel port, FLAG, SPI, and DAI interfaces

- Four programmable flags
- 11 LEDs: 1 power (green), 1 board reset (red), 1 USB monitor (amber), and 8 general purpose (amber)
- 5 push buttons: 1 reset, 2 connected to DAI, 2 connected to the FLAG pins of the processor
- USB cable
- CE certified

The ADSP-21363/21364/21365/21366 SHARC processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the ADSP-21264 SHARC processor. Thus, this EZ-KIT Lite evaluation system may be used for any of these devices.

ADSP-21369 EZ-KIT Lite From Analog Devices

Part Number: ADDS-21369-EZLITE

Figure 2-4. ADSP-21369 EZ-KIT Lite Evaluation System

The ADSP-21369 EZ-KIT Lite, as shown in as shown in Figure 2-4, provides a cost-effective method for initial evaluation of the ADSP-21367/21368/21369 SHARC processors via a USB-based PC-hosted tool set.

The ADSP-21367/21368/21369 SHARC processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the 21369 processor. Thus the EZ-KIT Lite evaluation system may be used for any of these devices.

The EZ-KIT Lite includes an ADSP-21369 SHARC processor desktop evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, loader, and linker. It also includes sample processor application programs, a CE-approved power supply, and a USB cable.

Features

- ADSP-21369 SHARC processor
- 1M x 8-bit flash memory
- 1M 32-bit 4 banks SDRAM
- 512K x 8-bit SRAM
- 2M SPI flash memory
- AD1835 stereo, 96-kHz, 24-bit codec
- 4 x 2 RCA jack for four channels of stereo audio output
- 1 x 2 RCA jack for one channel of stereo audio input
- Headphone jack (connected to one of the stereo outputs)
- SPDIF In RCA jack

- SPDIF Out RCA jack
- ADM3202 RS-232 driver/receiver
- USB interface
- JTAG ICE 14-pin header
- Evaluation suite of VisualDSP++ development tools
- Flash programmer utility for downloading boot code to on-board flash memory
- Type A expansion interface with three connectors supporting external port, FLAG, SPI, and DAI interfaces
- 20-pin DPI header
- 26-pin DAI header
- 12 LEDs: 1 power (green), 1 board reset (red), 1 USB reset (red), 1 USB monitor (amber), and 8 general purpose (amber)
- 5 push buttons: 1 reset, 2 connected to DAI, 2 connected to the FLAG pins of the processor)
- ELVIS interface
- USB cable
- 3.5-mm stereo headphones
- 6-foot RCA audio cable
- 6-foot 3.5-mm/RCA x 2 Y-cable
- CE certified

ADSP-21375 EZ-KIT Lite From Analog Devices

Part Number: ADDS-21375-EZLITE

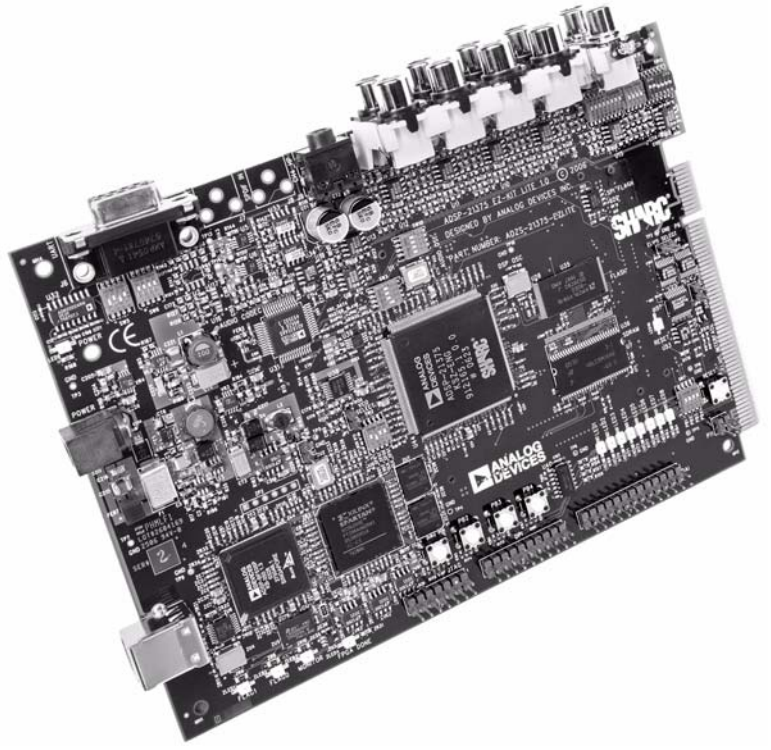

Figure 2-5. ADSP-21375 EZ-KIT Lite Evaluation System

The ADSP-21375 EZ-KIT Lite evaluation system, as shown in Figure 2-5, provides developers with a cost-effective method for initial evaluation of the ADSP-21371/21375 SHARC processors.

The ADSP-21371/21375 SHARC processors, which are pin-compatible, have similar memory maps. Software development for any of these devices can be performed on the 21375 processor. Thus the EZ-KIT Lite evaluation system may be used for any of these devices.

The EZ-KIT Lite includes an ADSP-21375 SHARC processor desktop evaluation board and fundamental debugging software to facilitate architecture evaluations via a USB-based PC-hosted tool set. With this EZ-KIT Lite, users can learn more about Analog Devices ADSP-21375 SHARC processor hardware and software development and prototype applications. The ADSP-21375 EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C/C++ compiler, assembler, loader, and linker. All software tools are limited to use with the EZ-KIT Lite.

Features

- ADSP-21375 SHARC processor
- 2M x 16-bit x 4 banks
- 1M x 8-bit flash memory
- 2M bit SPI® flash
- AD1835 codec
- ADM3202 RS-232 line driver/receiver
- Parallel port, SDRAM control, flags, DAI, DPI
- ELVIS interface
- Stereo in/stereo out RCA jack

- USB interface
- JTAG ICE 14-pin header
- Evaluation suite of VisualDSP++ development tools
- Flash programmer utility for downloading boot code to on-board flash memory
- Type A expansion interface with three connectors supporting external port, FLAG, SPI, and DAI interfaces
- 20-pin DPI header
- 26-pin DAI header
- 11 LEDs: 1 power (green), 1 board reset (red), 1 USB monitor (amber), and 8 general purpose (amber)
- 5 push buttons: 1 reset, 2 connected to DAI, 2 connected to the FLAG pins of the processor
- CE certified

EZ-KIT Lite Expansion Boards

EZ-KIT Lite expansion boards enhance and extend EZ-KIT Lite features and functions. This section describes the SHARC EZ-Extender daughter board and the SHARC USB daughter board.

SHARC EZ-Extender

Part Number: ADDS-21262-1-EZEXT

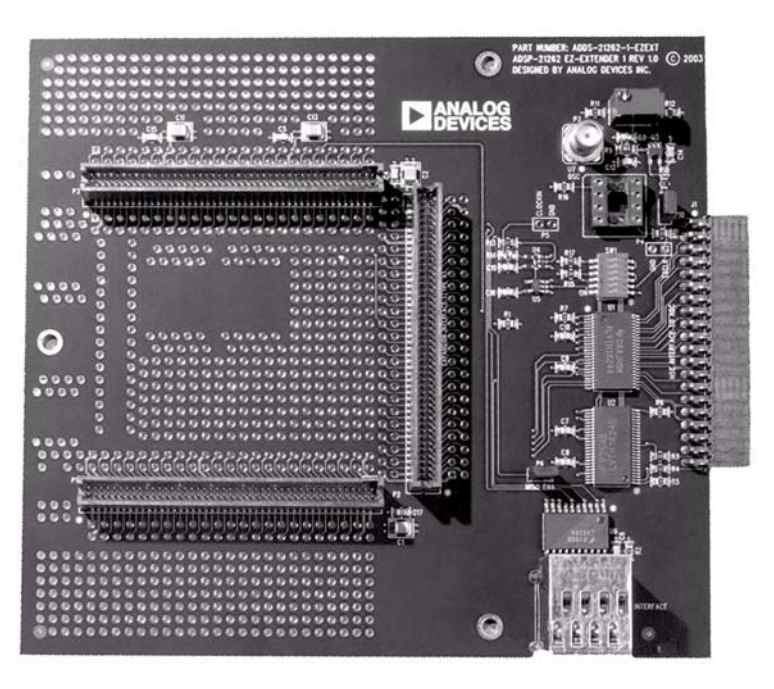

Figure 2-6. SHARC EZ-Extender

The SHARC EZ-Extender daughter board, as shown in Figure 2-6, is a separately sold assembly that plugs into a SHARC EZ-KIT Lite evaluation system's expansion interface. The extender aids the design and prototyping phases of SHARC processor-targeted applications.

The SHARC EZ-Extender allows developers to connect a number of Analog Devices analog-to-digital (ADC) high-speed converter (HSC) evaluation boards to the ADSP-21262 EZ-KIT Lite and the ADSP-21364

EZ-KIT Lite. The SHARC EZ-Extender also provides developers a bread-board area and the ability to access all of the pins on the ADSP-21262 and ADSP-21364 EZ-KIT Lite's expansion interface.

The SHARC EZ-Extender features:

- Expansion interface for connecting to the ADSP-21262 and ADSP-21364 EZ-KIT Lites
- Analog Devices high-speed converter (HSC) interface for connecting analog-to-digital (ADC) HSC evaluation boards such as the AD9244-40PCB and the AD9244-65PCB
- 40-pin, 0.1-in. spacing, right angle, female socket connector
- RJ45 connector for providing SPI signals for configuring converter registers
- SMA connector for connecting to an external clock source
- Unpopulated socket for inserting of an optional oscillator
- SMT footprint area; 1206 and 805 footprints
- SOIC24 and SOIC20 footprints
- Dimensions: 5 in. x 5 in.

SHARC USB EZ-Extender

Part Number: ADDS-SHRCUSB-EZEXT

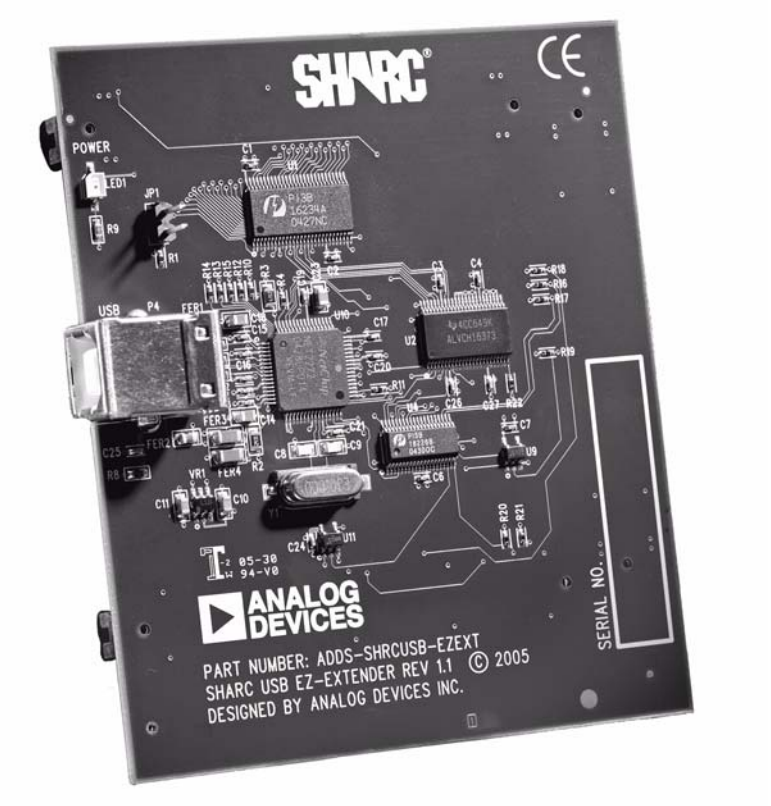

Figure 2-7. SHARC USB EZ-Extender

The SHARC USB EZ-Extender daughter board, as shown in Figure 2-7, provides a solution for users to evaluate different peripherals on SHARC processors.

The SHARC USB EZ-Extender daughter board allows developers to connect to the parallel port on the ADSP-21262 and ADSP-21364 EZ-KIT Lite and to the asynchronous memory bus on the ADSP-21369 EZ-KIT Lite and the ADSP-21375 EZ-KIT Lite. The EZ-Extender has peripherals that support USB 2.0.

The SHARC USB EZ-Extender daughter board features:

- USB 2.0 interface. No power supply required, derives power from EZ-KIT Lite.
- CE certified
- Dimensions: 3.13 in (H) x 3.6 in (W)

JTAG Emulators

JTAG (Joint Test Action Group) is defined by the IEEE 1149.1 standard for a test access port for testing electronic devices. This standard defines a method for serially scanning the I/O status of each pin on the device as well as controlling internal operation of the device.

Boundary-scan testing was developed in the mid 1980s as the JTAG interface to solve physical access problems on PCBs caused by increasingly crowded assemblies due to novel packaging technologies. Boundary-scan embeds test circuitry at chip level to form a complete board-level test protocol. With boundary-scan—industry standard IEEE 1149.1 since 1990—you can access the most complex assemblies for testing, debugging, in-system device programming, and diagnosing hardware problems.

SHARC processors are equipped with a JTAG port and thus support the IEEE 1149.1 standard for system test.

Through the JTAG port, you can run and halt the processor remotely. The internal and external processor memory can be read or written, and breakpoints can be set.

Most development boards include some built-in JTAG emulation circuitry. Your own hardware, most likely, does not contain this circuitry.

High-Performance USB 2.0 JTAG Emulator

Part Number: ADDS-HPUSB

Figure 2-8. High-Performance USB 2.0 JTAG Emulator

The Analog Devices high-speed, high-performance, universal serial bus-based emulator (HP-USB), as shown in Figure 2-8, provides a portable, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

These easy-to-use USB-based emulators perform a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the HP-USB emulator enables you to communicate with all of the Analog Devices JTAG processors using a full-speed USB 1.0 or high-speed USB 2.0 port on the host PC.

Applications and data can be tested and transferred easily (and rapidly, when the HP-USB emulator is connected to a high-speed USB 2.0 port on your host PC) between the emulators and the separately available VisualDSP++ development and debugging environment.

The plug-and-play architecture of USB allows the emulators to be automatically detected and configured by the host operating system. It can also be connected to (and disconnected from) the host without opening the PC or turning off the power to the PC. A 3-meter (9-foot) cable is included to connect the emulators to the host PC, thus providing abundant accessibility.

As a bonus, customers in an environment that does not allow them to open their PCs without IS support will find that both emulators eliminate the need to obtain that help and thus can be easily moved from the lab to the local desktop to the laptop.

Features

- High-speed USB 2.0 (backward compatible with full-speed USB 1.1) interface and connector
- JTAG clock operation from 10 MHz to 50 MHz
- Support for all ADI JTAG processors
- Multiple processor I/O voltage support with automatic detection
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant

- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support
- 14-pin JTAG connector
- 3-meter USB cable for-difficult-to-reach targets

USB 1.1 JTAG Emulator

Part Number: ADDS-USB-ICE
Availability: Now

Figure 2-9. USB 1.1 JTAG Emulator

The cost-effective universal serial bus (USB)-based emulator, as shown in Figure 2-9, from Analog Devices provides a portable, non-intrusive, target-based debugging solution for Analog Devices JTAG processors.

This USB-based emulator performs a wide range of emulation functions, including single-step and full-speed execution with predefined breakpoints, and viewing and/or altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the USB emulator enables users to communicate with all of the Analog Devices JTAG processors using a full-speed USB 1.1 or high-speed USB 2.0 port on the host PC. Applications and data can easily be tested and transferred between the emulator and the separately available VisualDSP++ development and debugging environment.

The plug-and-play architecture of USB allows the emulators to be detected automatically and configured by the host operating system. The USB can also be connected to (and disconnected from) the host without opening the PC or turning off the power to the PC. A 3-meter (9-foot) cable is included to connect the emulators to the host PC, thus providing abundant accessibility.

As a bonus, customers in an environment that does not allow them to open their PCs without IS support will find that the USB emulator eliminates the need to obtain that help and thus can be easily moved from the lab to the local desktop to the laptop.

Features

- Full-speed USB 1.1 compliant (forward compatible with high-speed USB 2.0 interface and connector)
- Support for all ADI JTAG processors
- Multiple processor I/O voltage support with automatic detection
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant
- 5 V tolerant and 3.3 V compliant for 5 V processors
- Multiprocessor support

- 14-pin JTAG connector
- 3-meter USB cable for difficult to reach targets

High-Performance PCI JTAG Emulator

Part Number: ADDS-HPPCI-ICE

Figure 2-10. High-Performance PCI JTAG Emulator

This high-performance (HP) PCI (peripheral component interconnect) emulator, as shown in Figure 2-10, offers code download speeds of up to 2.2 MB/sec with the JTAG clocked five times faster than its predecessor. It can also seamlessly exchange real-time data from the host to target application. The PCI-based emulator provides a high-speed emulation solution for Analog Devices state-of-the-art JTAG processors.

This high-performance PCI-based emulator consists of a small shielded POD and cable, allowing for a non-intrusive debug interface to all of the ADI JTAG processors. The emulator auto-detects voltages for 1.8 V,

2.5 V, 3.3 V, and 5.0 V targets as indicated by the display LEDs. The cable extends 6-feet from the host PC to the emulator POD, and extends 1-foot from the POD to the processor target. This new cable assembly greatly extends the reach of the emulator, helping to reduce clutter in the hardware lab.

Features

- Plug-and-play, PCI Revision 2.2 compliant
- Multiple emulator support
- Multiple processor I/O voltage support
- 1.8 V, 2.5 V, and 3.3 V compliant and tolerant
- 5 V tolerant and 3.3 V compliant for 5 V processors and DSPs
- Multiprocessor support
- JTAG clock operation up to 50 MHz
- 3-meter USB cable for difficult to reach targets

Selecting the Right Combination of Tools

Knowing which tools to use is critical to ensuring a quick development cycle. There are many options for software and hardware development tools. Two of the most common scenarios described in this section contain circumstances encountered by other developers along with recommended solutions. Your needs may be similar to one of the following scenarios.

Scenario 1

Question. *We are a small design house with one software engineer and one hardware engineer for this project. We cannot afford a substantial initial investment in tools. What do you recommend?*

Answer. Purchase a SHARC EZ-KIT Lite evaluation system (for example, p/n: ADDS-21364-EZLITE).

This hardware platform allows you to begin software development. By interfacing components to the board's expansion headers, the platform can serve as the basis for a hardware prototype. The EZ-KIT Lite evaluation system includes VisualDSP++, but the software license restricts various capabilities (debug agent connectivity only and reduced program size allowance).

Obtain a TestDrive serial number on the Analog Devices Web site at:

`http://analog.com/processors/tools/testdrive`

When the TestDrive license expires, consider purchasing a full seat of VisualDSP++ (p/n: VDSP-SHARC-PC-FULL).

After you have finished constructing your hardware, purchase a low-cost USB emulator (p/n: ADDS-USB-ICE) from Analog Devices.

Scenario 2

Question. *We have a team of seven software engineers who are developing code for the SHARC processor, but no more than five are likely to be using the tools at any given time. How do we handle licensing? Does each engineer need a license?*

Answer. A floating license may be right for you. VisualDSP++ may be installed on many machines. A developer checks out a floating license from a license server onto any machine. With five floating licenses, up to five people can use VisualDSP++ at the same time.

Order a floating license (p/n: VDSP-SHARC-PCFLOAT).

Software Development on SHARC Processors

Once the development tools are installed, begin working with application software development. Figure 2-1 on page 2-3 shows a typical development flow.

Some users modify a development board in parallel with software application development. The modified board serves as a prototype until their own hardware is built and ready.

Eventually, your custom hardware becomes available and you then move development to that platform. This custom hardware will include a 14-pin header called a JTAG port that connects to the SHARC processor. To debug this custom board, Analog Devices recommends that you purchase a JTAG emulator. Emulators enable you to perform the debug operations that you may have performed previously on a development board on your own custom hardware.

3 SUPPORT OPTIONS

This chapter addresses the support options available for users both during the evaluation process and development phases of SHARC processor processor design.

Available Support

Analog Devices provides a wide variety of processor support options. Material is available in printed form along with online information. Live training is also available. This information is available to evaluators of software and hardware solutions at the beginning of the evaluation process, to design engineers while they are developing a system, and to support engineers as they resolve compatibility and usability issues after product release.

Since information about its processor products is updated continuously and new material is added constantly, Analog Devices encourages you to keep up to date with new developments through our online resources.

Analog Devices Web Site

Your first point of reference for the most recent information is always the Analog Devices Web site. The following kinds of information are available:

- Processor and development tools selection guides
- Additional getting started information

- Applications notes, EE-notes, and other articles
- Communities-related information
- Platform-related information

Visit the SHARC processor home page at: http://www.analog.com/sharc. The Analog Devices Embedded Processing and DSP page, which offers access to other processor families, is located at

http://www.analog.com/processors

To visit the knowledgebase, use your browser to access this site: http://www.analog.com/processors/knowledgebase. This information is available to all classes of users, Analog Devices customers, and interested parties.

Processor and Development Tools Selection Information

For processor-specific information start at the Web site's SHARC processor page (http://www.analog.com/sharc), and then check SHARC processor offerings with regards to package, speed, or temperature specifications. Links provide access to additional processor selection information (such as peripherals and memory), development tools selection information, and other materials.

Getting Started Information

Under the heading "Help Me Explore," the SHARC processor page (http://www.analog.com/sharc) provides links that introduce the SHARC processor architecture and targeted applications. To find out about the processor's core and peripherals, refer to this Web site topic at the Analog Devices Web site. You may also want to check the benchmark data available from independent testers. A link to training and events provides an up-to-date list of local training seminars and upcoming events where you can learn more about all SHARC processor products.

Applications Notes, EE-Notes, and Other Articles

The most useful documents available to users are the Application or EE-(Engineer-to-Engineer) Notes, since they offer detailed technical information about using the SHARC processor. These materials may be downloaded from the Web site.

These documents supplement the standard documentation for processors and tools. EE-Notes focus on a very narrow or specific topic. Note that you can also use VisualDSP++ Help to search, locate, and view this collection of articles, as well as the entire list of all EE-Notes.

Additional links are provided to recently published articles, many of which have been featured in trade magazines. Please point your browser to:

```
://www.analog.com/ee-notes
```

Communities-Related Information

For information about application-specific development types, refer to the "Communities" topic at the SHARC processor Web site. Here you can find information about a particular application theme, such as audio, automotive telematics, or video and imaging.

Platform-Related Information

"Platform-related information" refers to the SHARC processor and its use with other hardware or software solutions.

Workshops and Seminars

The most efficient way to learn about the SHARC processor architecture is by attending a 3½-day (or 1-day) SHARC seminar. These seminars provide a mixture of lectures and demonstrations. The 3½-day workshop provides hands-on exercises and serves as an excellent starting point for both hardware and software development.

A variety of training options are available, both online and in a classroom setting. For users who prefer live training sessions, a variety of venues is available.

SHARC Processor Workshops

SHARC processor workshops are designed to develop a strong working knowledge of Analog Devices processors through lecture and hands-on exercises in a classroom setting.

These practical courses teach how to use the latest software development tools. First, the core elements of the processor, which includes the computational units, the data address generators, and the program sequencer, are examined along with the relevant assembly code instructions. A number of simulator labs help in understanding operation of the individual elements. Memory configuration (both internal and external) is discussed next. Advanced instructions are presented with a follow on lab session about code optimization. The I/O peripherals, which include the SPORTS, link ports, and external port, are discussed in detail along with DMA operation between these peripherals and internal memory.

Workshops are offered through Kaztek Engineering throughout the world. Visit the Kaztek Web site for the schedule of upcoming workshops and pricing information at:

http://www.kaztek.com/services.htm

SHARC Processor Seminars

The SHARC processor seminar is a subset of the SHARC Processor Workshop slide set and does not include hands-on exercises. A SHARC seminar is often accompanied by tools and software demonstrations running on hardware (sometimes by key Analog Devices third party partners).

Contact your local Analog Devices sales office or distribution partner for information on SHARC seminars or refer to:

`http://www.analog.com/processors/learning/index.html`

Processor Documentation

Three documents accompany each SHARC processor: a data sheet, a hardware reference, and a programming reference. These documents enable you to design software and hardware.

SHARC Processor Manuals

Two kinds of manuals provide detailed information about the SHARC processor: the hardware reference manual and the programming reference.

Hardware Reference Manuals

Each processor's hardware reference manual provides architectural information about that particular SHARC processor. The descriptions cover functional blocks, buses, and ports, including all features and processes that they support.

Before a processor is released to production, its hardware reference manual is available only in electronic form as a `.pdf` file. After it is released, the manual is available in both electronic form and as a printed manual. The VisualDSP++ Help system also includes a copy of each hardware reference manual and provides powerful search facilities to help you locate information.

You can find SHARC processor hardware reference manuals at:

http://www.analog.com/processors/manuals

Programming Reference

The programming reference contains information about the processor architecture and assembly language for SHARC processors. The manual provides information on how assembly instructions execute on the SHARC processor's architecture, along with reference information about processor operations.

Before a processor is released to production, its programming reference is available only in electronic form as a .pdf file. After it is released, the manual is available in both electronic form and as a printed manual.
The VisualDSP++ Help system also includes a searchable version of the programming reference so you can locate information quickly.

The processor core and instruction set, which is common to all SHARC processors, is documented in the programming reference manual.

You can find the SHARC processor programming reference at:

http://www.analog.com/processors/manuals

Printed Manuals

Printed copies of processor manuals, such as hardware reference, and programming reference manuals, may be ordered from the Analog Devices Literature Center at 800-ANALOGD (800-262-5643). When ordering hard copy documentation, specify the manual's title or product number (located on the manual's back cover).

Downloadable Manuals

While users may want printed versions of manuals, `.pdf` versions of these manuals are also readily available. These may be downloaded from the Analog Devices Web site. Open your browser and access:

`http://www.analog.com/processors/manuals`

Data Sheets

Data sheets are created for each SHARC processor and for each revision of a single product. Each SHARC processor data sheet provides:

- A high-level overview of the processor
- A description of processor pins
- Electrical, power, and timing characteristics/requirements
- Device package dimensions
- Environmental (temperature) information

To obtain data sheets for SHARC processors, open your browser and access:

`http://www.analog.com/processors/sharc`

Anomalies Lists for Processors and Tools

Analog Devices maintains an anomalies list for each subfamily of SHARC processors and also maintains an anomalies list for tools. These documents are updated as new information becomes available.

Processor anomalies represent the currently-known differences between revisions of SHARC devices and the functionality specified in the SHARC processor data sheets and hardware manuals. A revision number with the form "-x.x" is branded on all parts to identify them according to silicon revisions.

For processor anomalies, refer to:

http://www.analog.com/processors/technical_library

For tools anomalies, refer to:

http://www.analog.com/processors/tools/anomalies

BSDL Files

Boundary scan description language (BSDL) files are necessary for the application of boundary scan for board and system-level testing and in-system programming. BSDL files are the electronic data sheets that describe the IEEE 1149.1 or JTAG design within an IC, and are provided by the IC vendors as part of their device specifications. Use BSDL files to describe the test logic and generate a test for a loaded board.

IBIS Models

I/O buffer information specification (IBIS) models are used with various IBIS-based simulators for transmission line simulation of digital systems. These models accurately simulate I/O buffers, termination, and circuit board traces. The simulation time is much faster than SPICE simulations, because it is a behavioral model that relies on tabulated current versus voltage characteristics. For more information about IBIS models, see the main ANSI/EIA IBIS home page at:

http://www.eigroup.org/IBIS

CrossCore Tools Documentation

Documentation in both electronic form and printed form describe the various components of the CrossCore software and hardware tools. Analog Devices offers a software tools environment (VisualDSP++) and an assortment of hardware development tools.

For software tools, each release of VisualDSP++ includes a complete set of manuals, describing the entire software development tool chain. Printed copies of VisualDSP++ software tools manuals (compiler, assembler, and so on) ship with the software. You can purchase additional sets through Analog Devices Customer Service (781-329-4700). For additional information, call 603-883-2430. If you do not have an account with Analog Devices, you will be referred to an Analog Devices distributor.

Printed copies of software tools manuals are not provided with "TestDrive" licences.

"Hardware Tools Documentation" on page 3-12 describes EZ-KIT Lite evaluation systems, emulators, and extender boards. Printed copies of hardware tools manuals are packaged with the hardware.

To access the VisualDSP++ Tools Anomalies search page, point your browser at:

`http://www.analog.com/processors/tools/anomalies`

VisualDSP++ Documentation

This section briefly describes the VisualDSP++ manual set. The purchase of a full license of VisualDSP++ includes a printed copy of each manual. Electronic versions of documents are available from the VisualDSP++ installation CD-ROM or via download from the following Web page:

`http://www.analog.com/processors/technical_library`

VisualDSP++ Help incorporates a searchable version of the VisualDSP++ manual set plus processor documentation and other tools manuals. See "VisualDSP++ Help" on page 3-13 for details.

VisualDSP++ Getting Started Guide

This manual provides step-by-step, 15-minute tutorials that highlight VisualDSP++ features. By completing the tutorials, users can become familiar with the VisualDSP++ environment quickly, and see how easy it is to use several tools in your own digital signal processing (DSP) development projects.

This manual and accompanying software provide an excellent starting point to gain a high level of understanding of the VisualDSP++ suite of project management and application development tools.

VisualDSP++ User's Guide

This manual describes the features, components, and functions of the VisualDSP++ integrated development and debugging environment (IDDE). It covers license management, project management, code development, debugging tools, VDK, and much more.

Use this high-level reference to delve further into the powerful features of VisualDSP++.

VisualDSP++ C/C++ Compiler Library Manual for SHARC Processors

This manual contains information about the C/C++ compiler and its features designed for use with SHARC processors. It includes syntax for command lines, switches, and language extensions. It leads you through the process of using library routines and writing mixed C/C++/assembly code.

VisualDSP++ Runtime Library Manual for SHARC Processors

This manual contains information about the C/C++ and DSP run-time libraries for SHARC processors. It leads you through the process of using library routines and provides information about the ANSI standard header files and different libraries that are included with this release of the `cc21k` compiler.

VisualDSP++ Assembler and Preprocessor Manual

The manual provides how-to information for writing assembly programs for SHARC processors and reference information about related development software. It also provides information on new and legacy syntax for assembler and preprocessor directives and comments, as well as command-line switches.

VisualDSP++ Linker and Utilities Manual

This manual provides information on the linking process and describes the syntax for the linker's command language—a scripting language that the linker reads from the linker description file (`.ldf`). The manual leads you through using the linker and archiver to produce processor programs. It also provides reference information on file formats and utility software.

The manual also describes how overlays and advanced `.ldf` commands are used for memory management. In addition, it describes the expert linker, an interactive graphical tool to set up and map processor memory.

VisualDSP++ Kernel (VDK) User's Guide

This manual contains information about the VisualDSP++ kernel, a real-time operating system kernel integrated with the VisualDSP++ development tools. The VDK incorporates state-of-the-art scheduling and resource allocation techniques tailored specifically for the memory and timing constraints of DSP programming. Using frameworks of template

files, the kernel facilitates development of performance-structured applications. The kernel is designed for effective operations on Analog Devices processors.

The majority of the information in this manual is generic to all Analog Devices families. Information applicable to a particular target processor, or to a particular processor family, is provided in Appendix A, "Processor-Specific Notes." This manual explains the kernel internal structure and operation.

VisualDSP++ Loader and Utilities Manual

This manual contains information on how to use the loader/splitter to convert executable files into boot-loadable (or non-bootable) files. These files are then programmed/burned into an external memory device within your target system.

The manual begins by examining where loading/splitting fits in the typical program development activities. It discusses boot modes, boot streams, and second stage kernels. This manual contains the details you need to know about booting each particular subfamily of SHARC processors.

Hardware Tools Documentation

Each hardware tool available from Analog Devices includes electronic and printed documentation. Typically this documentation includes schematics, a short description of switch and jumper settings, and a bill of materials. Printed documentation accompanies the purchase of hardware. The hardware tools available are:

- EZ-KIT Lite evaluation system
- Emulator
- EZ-Extender card
- USB EZ-Extender card

Download electronic versions of the documentation (`.pdf` format) from the following Web page:

`http://www.analog.com/processors/technical_Library`

SHARC EZ-KIT Lite Evaluation System Manual

This manual provides instructions for using the hardware and installing the software on your PC. This manual also provides guidelines for running your own code on the SHARC EZ-KIT Lite. In addition, the manual describes the operation and configuration of the evaluation board's components. Finally, a full design database (schematics, layout, and a bill of materials) is provided as a reference for future SHARC processor board designs.

This manual provides information on the EZ-KIT Lite from a programmer's perspective and provides a memory map of the board.

SHARC EZ-Extender Manual

This manual provides example programs to demonstrate the capabilities of the SHARC EZ-Extender board and the SHARC USB EZ-Extender board.

VisualDSP++ Help

VisualDSP++ online Help is a powerful search tool. It combines the following documents and much more in one place:

- VisualDSP++ manual set
- Processor hardware manuals and hardware tools manuals
- Over 200 technical articles (EE-Notes)

The Help system is integrated into VisualDSP++'s graphical user interface and also provides context information (for debugging windows, tools, and dialog boxes). Each task is described in clear, step-by-step detail.

Best of all, VisualDSP++ Help provides a single access point to just about every processor hardware and tools document produced by Analog Devices.

The search engine in Help enables you to find information quickly from a two-foot deep stack of printed manuals, spanning over 10,000 pages.

VisualDSP++ Help, built around the familiar Microsoft HTML Help standard, enables you to:

- Copy code examples from Help into your source documents
- Bookmark and print topics
- Perform a full text search, or refine a search with wildcards, nested expressions, or Boolean operators

The Collaborative

The Collaborative is a network of processor/DSP third-party developers for Analog Devices. The Collaborative consists of companies all over the world that provide hardware products, software products, algorithms, and design services for a wide variety of applications and markets. Our partners offer consulting services as well as commercial off-the-shelf products specifically for parts from Analog Devices. To learn more, go to:

http://www.analog.com/processors/3rdparty

Technical or Customer Support

Access Analog Devices Customer Support in the following ways:

- Visit the Embedded Processing and DSP Products Web site at
  http://www.analog.com/processors
- E-mail tools questions to
  processor.tools.support@analog.com
- E-mail processor questions to
  processor.support@analog.com (Worldwide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, local sales office or authorized distributor
- Send questions by mail to:
  Analog Devices
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Registration

Visit http://www.myanalog.com to sign up. Click **Register** to use this site. Registration takes about five minutes and serves as a means to select the information you want to receive.

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