ENEE 244 6

1. Design a modulo-6 counter, which counts 0,1,2,3,4,5,0,1,..... The counter counts the clock pulses if its enable input,w, is equal to 1. Use D flip flops in your circuit. If the circuit ever finds itself in an unused state (6 or 7), it should transition to state 0 with the next clock trigger to avoid being stuck in an unused state. Use a formal design procedure. No credit for doing an intuitive design!

Drawing the state table for the given modulo 6 counter.

Present state			Input	Next state		
Q2	Q1	Q0	W	Q2+	Q1+	Q0+
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	1	0	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	0	0	0
1	1	1	1	0	0	0

For D flip-flops, the input into the flip flops is the same as the next state that are shown in the table. (D2=Q2+, D1 = Q1+, D0 = Q0+).

Now drawing 4-variable K maps for D flip flop inputs D2, D1 and D0 we get the following result (K-maps not shown):

D2 = Q2Q1'Q0' + Q2Q1'W' + Q2'Q1Q0W

D1 = Q2'Q1Q0' + Q2'Q1W' + Q2'Q1'Q0W

D0 = Q2'Q0'W + Q1'Q0'W + Q2'Q0W' + Q1'Q0W'.

The above equations completely define the required circuit.

2. Design a counter with T flip flops that goes through the following binary repeated sequence 0,1,3,7,6,4. Show that when the states 010 and 101 are considered as don't care conditions the counter may not operate properly.

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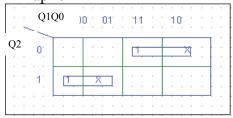
There are ceiling(log 2 6) = 3 flip-flops required.

Drawing the state table:

Present state			Next state			Excitation		
Q2	Q1	$\mathbf{Q0}$	Q2+	Q1+	Q 0+	T2	T1	T0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

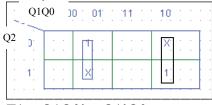
Drawing the K maps for T2, T1 and T0:

K map for T2



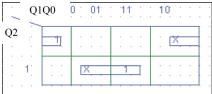
 $\overline{T2 = Q2Q1' + Q2'Q1}$





$$T1 = Q1Q0' + Q1'Q0$$

K map for T0



$$T0 = Q2Q0 + Q2'Q0'$$

In the K-maps, all the don't cares were assigned to 1 in our choice, so the flip-flops will all toggle in states 010 and 101. Thus if the counter finds itself in state 010, it will transition to 101, and vice versa. This constitutes an infinite cycle of unused states. Hence the counter is **not** self-correcting -- if the counter ever finds itself in an unused state, it will remain in unused states forever.

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