CSE 202: DIGTAL LOGIC DESIGN

Credit Hours: 3
Contact Hours: 3
Grading: As per UET Statues

1. COURSE OUTLINE

Digital vs Analog, Binary digits, Logic levels and digital waveforms, Logic operation and functions, Switches and relays, Fundamental logic gates, Boolean Algebra and logic simplification, Fundamental theorems of Boolean Algebra, Truth tables, Karnaugh Map, SOP and POS minimization, Combinational circuits, Number systems, operations and codes, Design of various logic functions, e.g. Adders, Comparators, Encoders/Decoders, Mux/DeMux, BCD-to-7-Segment Decoder, Implementation of combinational circuits using discrete chips and programmable logic devices, i.e. ROMs/PLAs, Speed and delays in logic circuits, Sequential circuits, Latches, Flip-Flops and their applications, 555 Timer, Sequential circuit applications, Asynchronous and synchronous counters, UP/DN counters, Shift registers, Semiconductor memories, RAM, ROM, PROM and EEPROM, Flash memories, Design of a simple processor.

2. WEEKLY PLAN

Week	Contents
Week 1	1. Digital vs. Analog 2. Binary Logic, Digital Logic Gates, and Digital Waveforms 3. Number Systems 4. Binary Codes
Week 2	1. Boolean Algebra 2. Fundamental Theorems of Boolean Algebra
Week 3	1. Digital Design Procedure i. Problem Statement ii. Input-Output Relationship 2. Boolean Functions i. Truth Tables ii. Boolean Expression iii. Canonical Form iv. Standard Form
Week 4	1. Simplification Techniques i. Iterative Method ii. Karnaugh Map
Week 5	1. Common Logic Circuits Design Examples-I i. Code Converters (BCD-to-Excess-3, BCD-to-7-segment) ii. Odd-Prime Detector iii. Magnitude Comparator iv. Parity Generator and Checker

Week 6	1. Common Logic Circuits Design Examples-II i. Adders ii. Subtractors 2. Encoders 3. Decoders 4. Implementation of Logic Circuits using Decoders
Week 7	1. Multiplexers 2. Demultiplexers 3. Implementation of Logic Circuits using Multiplexers
Week 8	1. Concept of Memory i. Read Only Memories (ROMs) ii. Programmable Logic Arrays (PLAs) 2. Implementation of combinational circuits using discrete chips and programmable logic devices, i.e. ROMs/PLAs
	Midterm Examination
Week 9	1. Sequential circuits 2. Latches
Week 10	1. Flip-Flops and their applications i. SR Flip-Flop ii. D Flip-Flop iii. JK Flip-Flop iv. T Flip-Flop
Week 11	1. Edge Triggered vs. Level Sensitive i. JK Flip-Flop ii. Master Slave Flip-Flop 2. Sequential circuit applications i. 1-bit Random Access Memory
Week 12	1. Registers i. Buffer Registers ii. Shift Registers iii. Parallel to Serial Converters iv. Serial to Parallel Converters
Week 13	1. Design Procedure of Asynchronous/Ripple Counters i. Up Counters i. Down Counters ii. Up-Down Counters iii. Controlled Counters iv. Modulus Counters v. Presettable Counters
Week 14	1. Design Procedure of Synchronous Counters 2. Ring Counters
Week 15	1. Hardware design of a simple Computer involving the following units i. Program Counter ii. Memory Address Register iii. Random Access Memory

	iv. Instruction Register v. Arithmetic Logic Unit vi. Temporary Registers vii. Controller Sequencer viii. Introduction to Assembly Language Programming using the Instruction Set of a Simple Microprocessor leading to 8085 ix. Timing States & Instruction/Program Execution Time
Week 16	Course Revision
	Finalterm Examination

3. CLOs AND ITS MAPPING WITH PLOs

CLO #	CLO	Level of Learning	PLOs
CLO-1	Understand different number systems, binary addition and subtraction, 1's and 2's complement representation, addition and subtraction with these representations, Boolean algebra theorems and their applications to combinational logic circuits	Cog-3 (Application)	PLO-1 (Engineering Knowledge)
CLO-2	Translate descriptions of logical problems to digital logic circuits and define the Karnaugh map to perform an algorithmic reduction of logic circuits	Cog-4 (Analysis)	PLO-2 (Problem Analysis)
CLO-3	Design and understand the following combinational and sequential circuits: adders, subtractors, encoders, decoders, multiplexers, (de)multiplexers, parity generators, comparators, ROMs, PLAs, latches, flip-flops, counters, and shift registers; and to perform simple projects with them	Cog-5 (Synthesis)	PLO-3 (Design/Development of Solutions)
CLO-4	Integrate simple combinational and sequential circuits into a fairly large-scale system to meet specified requirements	Cog-5 (Synthesis)	PLO-3 (Design/Development of Solutions)

4. CLOs ASSESSMENT MECHANISIM

Course Assessment Tools	CLOs			
	CLO-1	CLO-2	CLO-3	CLO-4
Assignments	✓	✓	✓	✓
Quizzes	✓	✓	✓	✓
Class participation	✓	✓	✓	✓
Midterm examination	✓	✓	✓	
Finalterm examination		✓	✓	✓

5. RESOURCES

- TEXT BOOKS
  - Digital Logic Design by Morris Mano
  - Digital Computer Electronics by Malvino & Brown

- REFERENCE BOOKS
  - Digital Fundamentals by Thomas L. Floyd