# University of Engineering & Technology, Peshawar

**Programme: BSc Computer Systems Engineering**

**Semester: 3rd Semester**

**Paper: Digital Logic Design** **Date: 10th March, 2021**

**Exam Type: Final Term**

| | |
|---|---|
| **Allowed Time: 180 Minutes** | **Max Marks: 50** |
| **Student's Name:** | |
| **Student's Registration:** | |

## Instructions:

1- This exam is OPEN books/notes/Internet.
2- Sharing of books, notes and other materials during this exam is not permitted.
3- Answer ALL questions on the question sheet.
4- There are 3 problems (and 9 questions) in total. Some questions are harder than others. Answer the easy ones first to maximize your score.
5- Questions will not be interpreted during the exam.

Problem 1: Decoders and Encoders ..... (20 pts.)

1(a) ..... (6 pts.)

The truth table shown below is for a 3-line to 8-line binary Decoder circuit:

| Inputs | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

For each of the eight output lines, there is a Boolean expression describing its function. Write the Boolean expressions for output lines $D_2$, $D_6$, and $D_7$.

Solution:

$D_2$ = _____

$D_6$ = _____

$D_7$ = _____

1(b) …… (6 pts.)

Design a combinational circuit using a Decoder and OR gates. The circuit accepts a 2-bit number and generates an output binary number equal to the square of the input number.

Solution:

Truth Table:

Design:

1(c) …… (5 pts.)

Construct a 4x16 Decoder using 2x4 Decoders.

Solution:

1(d) …… (3 pts.)

What is a priority Encoder, and how does it differ from a regular Encoder?

Solution:

Problem 2: Multiplexers and De-Multiplexers …… (15 pts.)

2(a) …… (5 pts.)

Construct an 8x1 Multiplexer using two 4x1 Multiplexers and a 2x1 Multiplexer.

Solution:

2(b) …… (5 pts.)

Implement the following function using a Multiplexer.

$$F(A, B, C) = \sum_m (1, 4, 6, 7)$$

Solution:

2(c) …… (5 pts.)

Design a 1x4 De-Multiplexer using gates. Draw its truth table and logic circuit.

Solution:

Truth Table:

Logic Circuit:

Problem 3: Latches and Flip-Flops ……. (15 pts.)

3(a) …… (5 pts.)

What is the difference between a Latch and a Flip-Flop?

Solution:

3(b) …… (10 pts.)

The waveforms in Fig 1 are applied to the J, K and CLK inputs of the positive edge-triggered JK flip-flop shown in Fig 2. Determine the Q output, starting in RESET state.

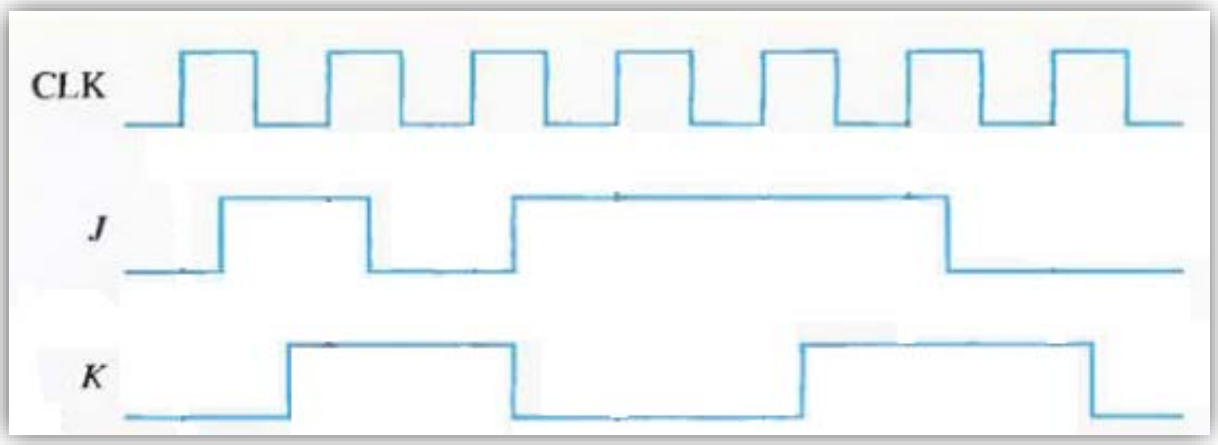


Fig 1. Input waveforms

| INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|
| J | K | CLK | Q | $\overline{Q}$ | COMMENTS |
| 0 | 0 | ↑ | $Q_0$ | $\overline{Q}_0$ | No change |
| 0 | 1 | ↑ | 0 | 1 | RESET |
| 1 | 0 | ↑ | 1 | 0 | SET |
| 1 | 1 | ↑ | $\overline{Q}_0$ | $Q_0$ | Toggle |

↑ = clock transition LOW to HIGH

$Q_0$ = output level prior to clock transition

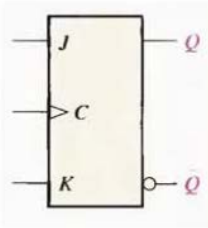


Fig 2. Truth table (left) and logic symbol (right) for a positive edge-triggered JK flip-flop

Solution: