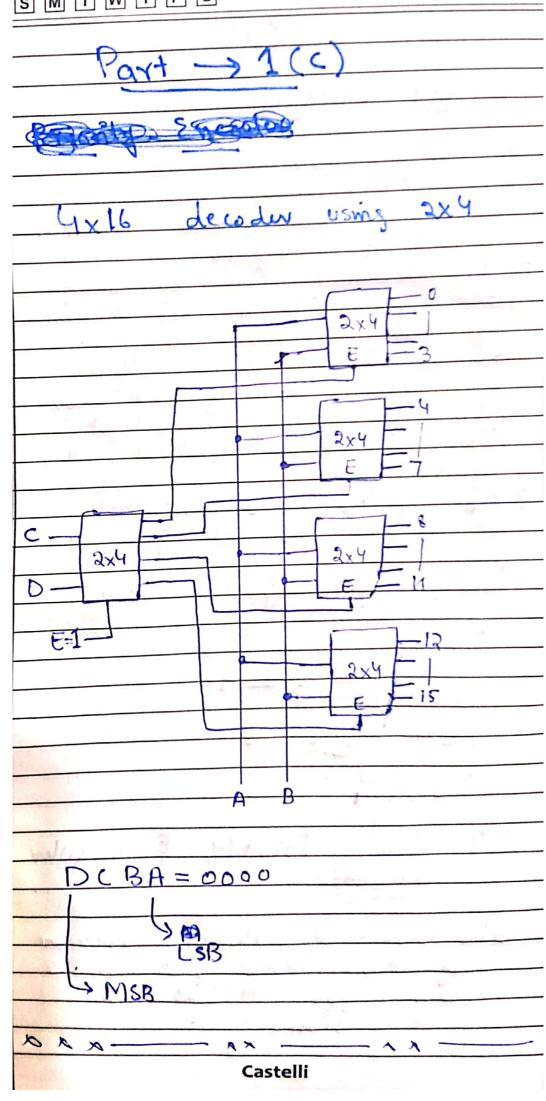
S M T W T F S	Date:
	)
A Land	F. T. W. T. V
The second secon	
O VOO	Daney
tinal-terr	n Daper
the state of the s	
Digital logic &	Computer
-0	
1 Design	- NA 21 - 11
Design	
*	
Dans I Dall	FAC ALLDONA
Name: Ash	FAQ AHMAD
Reg No: 19P1	ucse1795
Section:	3
and the state of the state of	Idasek Commen
and the second of the second of	the state of the state of
Date: 10-	03-2021
	D3-4041
	4
XXX	X XV
and and add to be a	
of outsides.	Higgs
A S. H.	Section 1
The state of the s	The same of the sa
A. J. Carl	1 minutes and the second
	A STATE OF THE STA
Castelli	

Name: ASHFACO AHMAD Reg Nio: 19PWCSE1795 page 2

SMTWTFS	Date:
Problem No -	(1)
(Decoder & En	wden)
X × X	× y
Part -> 1(a)	
Da = ABC	
DG= ABC	
· · · · · · · · · · · · · · · · · · ·	
D7= ABC	χ λ
	14.19-12.1
Part -> 1(b)	
Touth table	
Imputs outputs	decimal
BAWMYZ	of .
0 0 0 0 0 0 0	0
0 0 0 0 0	4
11001	9
Circuit!	
A	
324	
	1980
h X Y	V
W X O	2
Castelli	
II	"



Name: ASHEAD AHMAP		
Name: ASHFAO HOUSE 1795 page		
100,100		
S M T W T F S Date:		
Part -> 1(d)		
Proriety Encoder:		
-)11 a compraise multiple		
that Compressess months		
main of outputs		
-> la normal Encoder only		
one trust active at a mine		
if there is my		
active of a time Encoder		
21 DIE me me mout		
-) (V) Proposition of Soldscript will		
***************************************		
AG: 12 As & Az both active		
at a time A3 will goes orport.		
4x2 proviety Encoder		
4x 2 promety contoaco		
Do		
To Day B		
D <sub>1</sub>		
Da III		
D <sub>3</sub>		
D/E blw Proviety & regular		
D/f blu Proviety & regular Encoder:		
CVI CORKY		
In case of Pronety Encoder		
more than one mous		
coin los active at		
a time		
PTPO		
Castelli		

Name: ASHFACI AHMAD Ros No: 19pwise 1795 page 5

SMTWTFS	Date:
> While Incase 5	ruzuler
Encoder only	one Impot
und be beti	we out
a time.	
-XX	× × -
	~ ~ .
2 / 9	The state of the s
Problem: (2	
/M 6 1	200111
(Mux & de.	-11102
xx xx	Y- 28
Part -> 2(a)	
8XI MUX Usir	a 2(UVI)
and one axi n	
	1 1
17-11-11	The side of the si
To Mux	
5	
SI	
So	3x1 Y
I3- 4x1	MUX
Iz- mux	
I.	Sa
Io -	3
x4 - x4 - +x -	- xx
	And the second s
Castelli	

Reg. No: 19PWCSE 1795 Page (6)
Reg. No: 19PWCSE 1795 Page (6)
S M T W T F S Date:
Part -> a(b)
The state of the s
Given.
F(A,B,C) = [m(1,4,6,7)
Sul
T. Table
ABCF
AND
1 0 0 1
1 0 1 0
1 10 1
As no of Impacts = 3
So
Selection lines = n-1
= 3-1
Selection lines = 2
So we will use ax mux
>B and c will be Selection
lines and A will to
Consider as injusts.
(1/2013)
Now we will made
Implementation tests.
P P T P D
Castelli

Name: ASHEAG AHMAD Reg No: 19pwest 1795 SMTWTFS I3 -> loputs MUX A (7) (P) 4 A -A these ove new 1mpuls of WIUX. Circuit Diagram! 4x1 入入 Using De-Mux Imputs = 1 Selection lines = out put D3 50 Do Di 0 0 0 0 0 0 0 1 0 0 0 0 0 Castelli . T D

Name: ASHFARD: AHMAD:
Reg No: 19PWCST 1795 page: (E

SMTWTFS	Date:
> Expressions	1 7 2 1 1 1
$D_0 = T \in S_1$	Do= LSB:
D1 = 13, 50	D3=MSB
Da = Isi Sa	
D3 = I S1 S0	I= Input
I So SI EN	
	13 644
	Do
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Die
	)
	- Da
	D3
	un be
if EN=0 Circuit	deservice the second se
Dizabi	e will be
it ENZI circuit Enai	ole :
	xx
<u> </u>	
PPT	3
	and a second
	A P THE S
Castelli	

Moinne i Reg No! ASHFACO AHMAD 19pwcse 1795 page 9

S	M T W T F S Date:	
1		
-	Problem (3)	
	1 48 DICM ( )	
	S Clip-Flops	
	Catches 6	
	Catches & Flip-Flops	
1		
$-\parallel$	Part -> 3(a)	No. of the last
-		118
	Disserved later & F/F:	
	Difference blu latch & F/F:	
	Same on the basis of	
	-> Both one differ the	
	each other or we	
	basis of triggening 601	
	Same on the boxes T	<u></u>
	functionality.	
	-) Catch is level sensetive	
	while Flip-Fing is Edge	
	Junctimality.  Tatch is level sensetive  While Flip-Flip is Edge  Sensetive.	
	-) latches are used us	
	Sensetive.  ) latches are Used in  Asynchronous circuits, while  tlip-Flops one Used ino  Synchronous circuit.  ) Output it latch is change;  at any trine while  while output it Flip/Flop  change on close-pulses	
	Flip-Flops one Used in	
	Synchronors circuit.	
1. 2	-) output it latch is change	
37.6	at any time while	
	while output of Flip/1=lop	,
	change on clock-pulses  > latch donot need clock	
	1	
	While Flip-Flop need	
	a cloud	
	-> latch require less gates	
	colule Flip Flop regions	
	mere gate;	A
	- later regime less power	
	while Flip - Flop veguine	
	muse power.	
	→ latch donot need closes  While Flip-Flop need  a close  - latch require less gates  unule Flip-Flop require  more gates  → latch require less power  while Flip-Flop veguire  more power.  - xx - P p r +0 - xv - x.	
	Castelli	
-		
1		
7	THE RESERVE TO SERVE THE PARTY OF THE PARTY	201
		25

Nome: ASHFACE AHMAD Reg No: 19PWCSE1795 page (o) SMTWTFS Date:....

Castelli