S M T W T F S Date:.....

Final-term Paper

Digital logic & Computer Design

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Section: B

Date: 10-03-2021

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Problem No - (1)

(Decoder & Encoder)

Part → 1(a)

$D_2 = \bar{A}B\bar{C}$

$D_6 = \bar{A}BC$

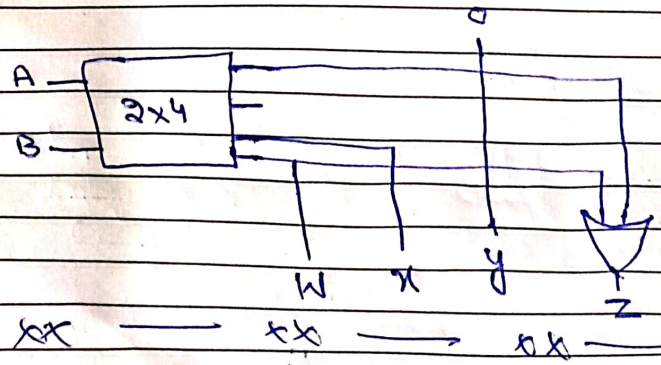
$D_7 = ABC$

Part → 1(b)

Truth table

Inputs		outputs				decimal
B	A	W	X	Y	Z	
0	0	0	0	0	0	0
0	1	0	0	0	1	1
1	0	0	1	0	0	4
1	1	1	0	0	1	9

Circuit:

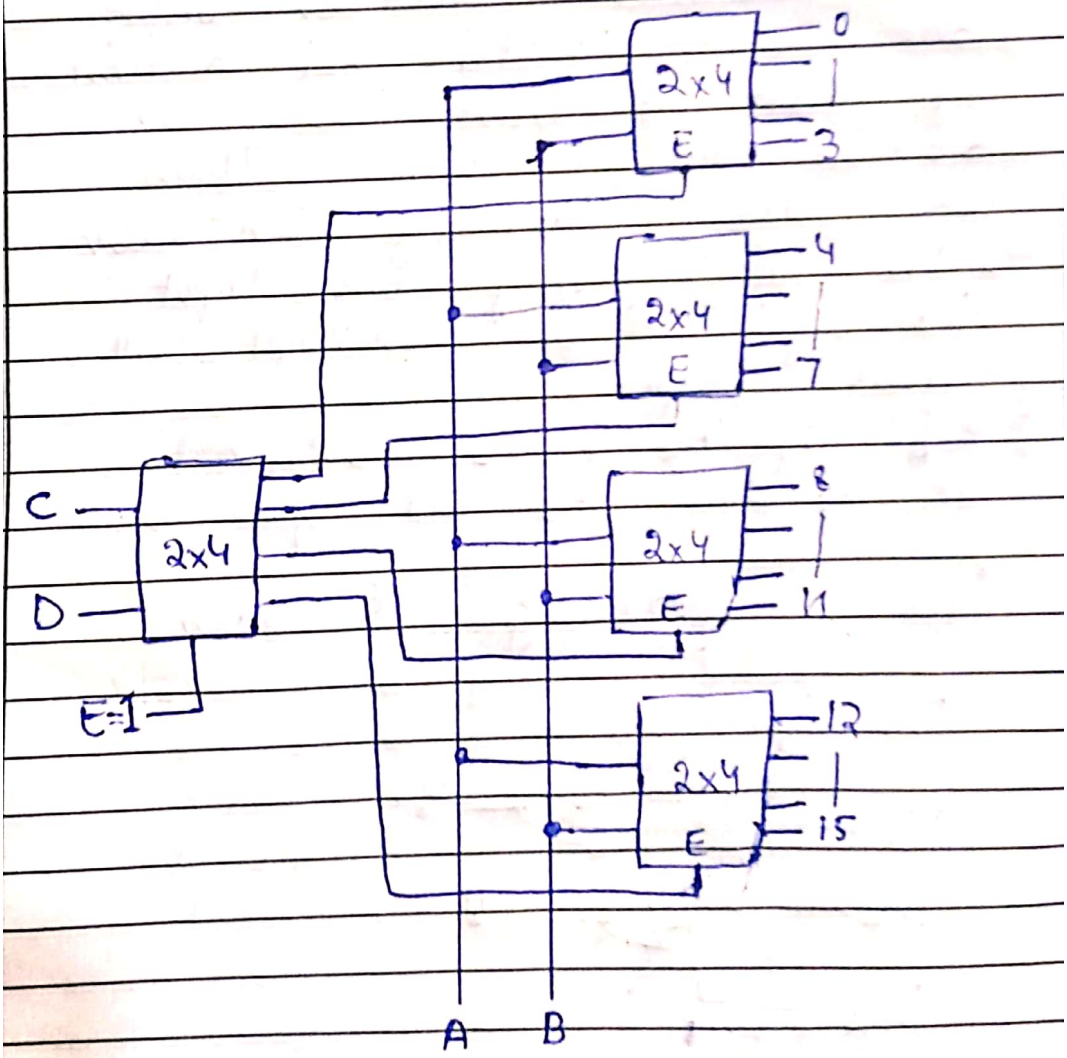


Castelli

Part → 1(c)

~~Design 2x4 Decoder~~

4x16 decoder using 2x4



DCBA = 0000

LSB

MSB

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Part → 1(d)

Proriety Encoder:

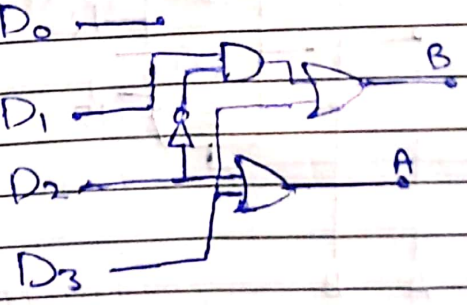
→ It is Combinational circuit that Compresses multiple binary Inputs into Smaller no. of outputs

→ In normal Encoder only one Input active at a time. if there is more than one active at a time then we use Proriety Encoder

→ In P.E only one Input having high Subscript will have output

→ eg: if A_2 & A_3 both active at a time A_3 will goes output.

4x2 Proriety Encoder



D/f b/w Proriety & regular Encoder:

→ In case of Proriety Encoder more than one Inputs can be active at a time.

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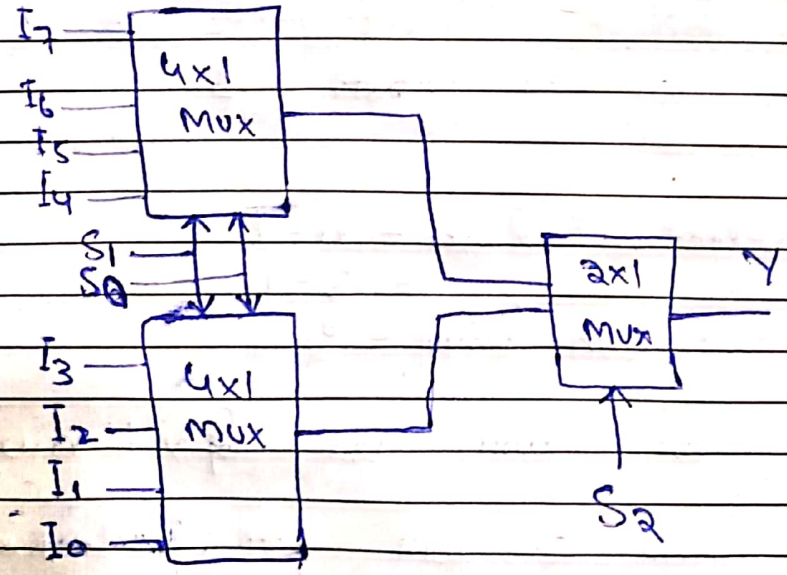
→ While Incase of ruzuler Encoder only one Input will be active at a time.

Problem : (2)

(Mux & de-mux)

Part → 2(a)

8x1 Mux using 2(4x1) and one 2x1 mux.



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Part → 2(b)

Given:

$$F(A,B,C) = \sum_m(1,4,6,7)$$

Sol

T.Table

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

As no of Inputs = 3

So

Selection lines = n - 1
= 3 - 1
Selection lines = 2

So we will use 4 x 1 mux

→ B and C will be Selection lines and A will be consider as inputs.

Now we will make Implementation table for A

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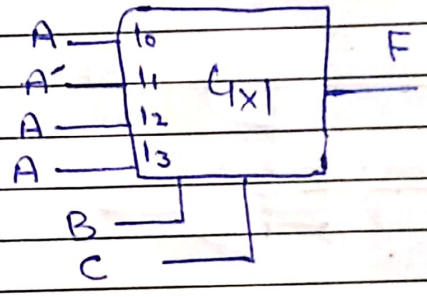
	I_0	I_1	I_2	I_3	→ Inputs of MUX
A'	0	1	2	3	
A	4	5	6	7	
	A	A'	A	A	→ these are new inputs of MUX.

Circuit Diagram:



Part → 2(c)

→ 1x4 De-MUX using gates,

T. Table:

Inputs = 1
Selection lines = 2
Outputs = 4

I	S_1	S_0	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

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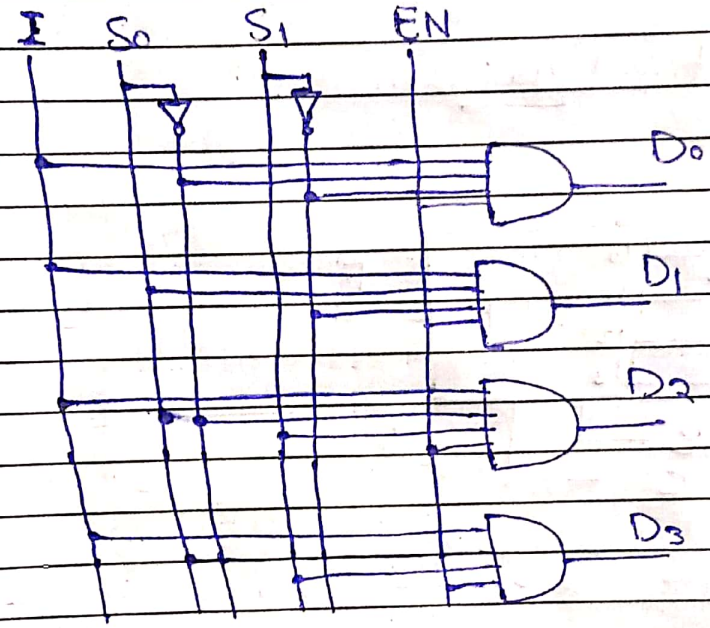
→ Expressions

$D_0 = I \bar{S_0} \bar{S_1}$ $D_0 = LSB$

$D_1 = I \bar{S_1} S_0$ $D_3 = MSB$

$D_2 = I S_1 \bar{S_0}$

$D_3 = I S_1 S_0$ $I = Input$



if EN=0 Circuit will be Disable

if EN=1 circuit will be enable.

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Problem (3)

Latches & Flip-Flops

Part → 3(a)

Difference b/w latch & F/F:

→ Both are differ from each other on the basis of triggering but same on the basis of functionality.

→ Latch is level sensetive while Flip-Flop is Edge Sensetive.

→ Latches are used in Asynchronous circuits, while Flip-Flops are used in Synchronous circuit.

→ Output of latch is change at any time while while output of Flip/Flop change on clock-pulses

→ Latch dosn't need clock while Flip-Flop need a clock

→ Latch require less gates while Flip-Flop require more gates,

→ Latch require less power while Flip-Flop require more power.

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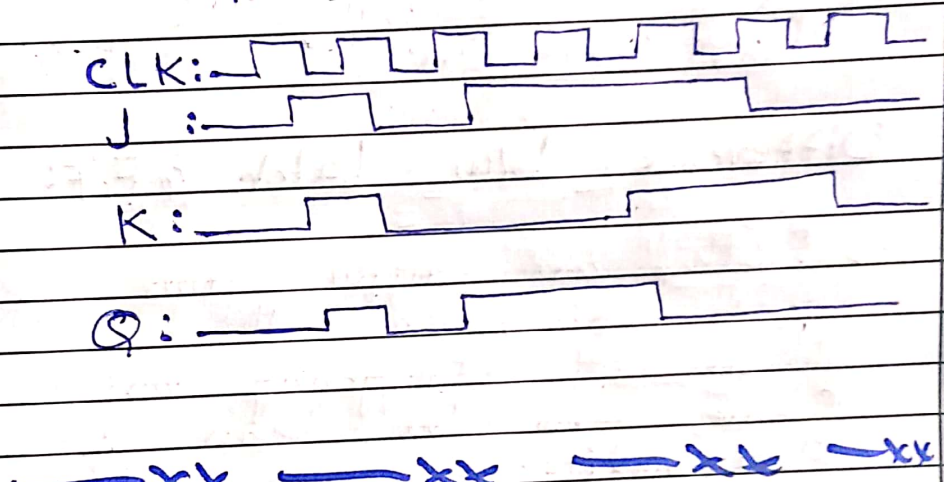
Part → 3(b)

Sol:



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