*Name: _____

*Registration: _____

Department of Computer Systems Engineering
University of Engineering & Technology Peshawar

Digital System Design
CSE 308

Midterm Examination Spring 2021
27 May 2021, Duration: 135 Minutes

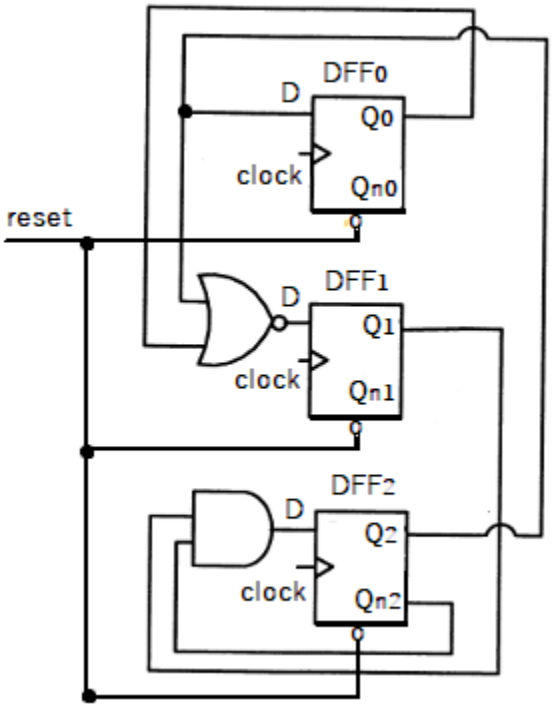
Start Time: **2:00 PM (Sharp)**
End Time: **4:15 PM (Sharp)**

****Exam Rules****
Please read carefully before proceeding.

1- This exam is open books/notes/Internet.
2- It's good to share but sharing of books, notes, and other materials during this exam is not permitted.
3- Answer all problems.
4- Problems will not be interpreted during the exam.

Good Luck!

Problem 1. (10 pts.)
In this problem, design a 3-bit counter (the circuit diagram and state table are shown in Figure 1) using as building block the D flip-flop given in Figure 2.



Input		Output
reset	clock	$Q_2Q_1Q_0$
0	X	000 **(0)**
1	↑	010 **(2)**
1	↑	110 **(6)**
1	↑	001 **(1)**
1	↑	000 **(0)**

Figure 1. The circuit diagram (left) and state table (right) of the 3-bit counter

```
module DFF (D, clock, reset, Q, Qn);

      input D; // Data input
      input clock; // Clock input
      input reset; // Asynchronous active-low reset
      output Q, Qn; // Outputs Q and Q'
      reg Q;

      always @ (posedge clock or negedge reset)
                  if (reset==1'b0)
                        Q <= 0;
                  else
                        Q <= D;

      assign Qn = ~Q;
endmodule
```

Figure 2. Verilog code for rising-edge D flip-flop with asynchronous active-low reset

The suggested skeleton file for the counter has been written below. The module has 2 inputs – **clock** and **reset** which is active-low. The output is **out** which is 3-bit in size.

```
module counter (clock, reset, out);

      input clock, reset;
      output [2:0] out;
      // Write your code here









endmodule
```

Problem 2. (10 pts.)
In this problem, write Verilog code for an 8-to-1 multiplexer. In this case, the value on the 3-bit select line will route 1 of 8 inputs to the output. This module is purely combinatorial.

The following are the ports of the module:

Sel	3-bit select line
I0, I1, I2, I3, I4, I5, I6, and I7	1-bit data inputs
OUT	1-bit output

Problem 3. (10 pts.)
For this design, combine the counter (from Problem 1) with the multiplexer (from Problem 2) to create a circuit such that the output of the counter controls the select lines of the multiplexer.

This top-level design has the following port definitions:

clk	1-bit clock
reset	1-bit reset line
D0, D1, D2, D3, D4, D5, D6, and D7	1-bit data inputs
OUT	1-bit output