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Department of Computer Systems Engineering
University of Engineering & Technology Peshawar

Digital System Design

CSE 308

Finalterm Examination Spring 2020

28 August 2020,   Duration: 150 Minutes

Exam Rules

Please read carefully before proceeding.

1- This exam is OPEN books/notes/Internet.

2- Sharing of books/notes and other materials during the exam is not permitted.

3- Answer all problems.

4- There are 5 problems in total. Some problems are harder than
   others. Answer the easy ones first to maximize your score.

5- Problems will not be interpreted during the exam.

6- This exam booklet contains 10 pages, including this cover. Count them to be
   sure you have them all.

Problem 1 ——————— (20 pts)

Problem 2 ——————— (20 pts)

Problem 3 ——————— (10 pts)

Problem 4 ——————— (20 pts)

Problem 5 ——————— (10 pts)

Exam Total ——————— (80 pts)

Good Luck!

Problem 1: (20 pts) Answer the following.

(a) (3 pts) The single stuck-at fault model assumes exactly one fault is present in the circuit. For the circuit given in Figure 1, give the test for **C s-a-0** and show that it is not possible to detect it when **A s-a-1** is also present in the circuit. What is this called?
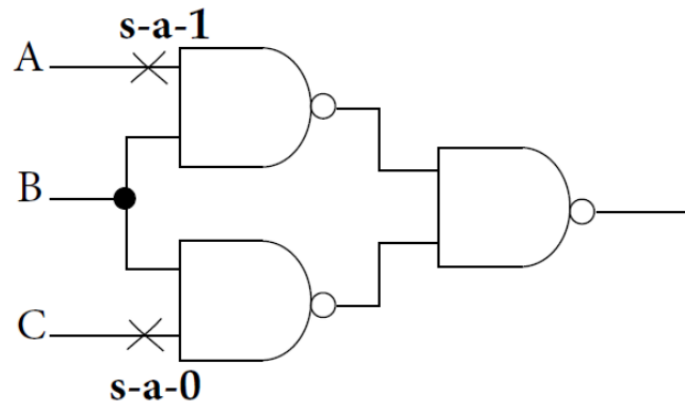

Figure 1: Circuit for Problem 1(a)

(b) (1 pt) A gate level circuit has 15 inputs, 10 fanouts and 5 outputs. What is the maximum number of tests we will need to test this circuit?
Hint: Checkpoint Theorem.

(c) (2 pts) In a 2-input NOR gate with inputs **A** and **B** and output **Z**, which of the following fault(s) can be removed due to dominance fault collapsing and why?

A s-a-0, A s-a-1, B s-a-1, Z s-a-0

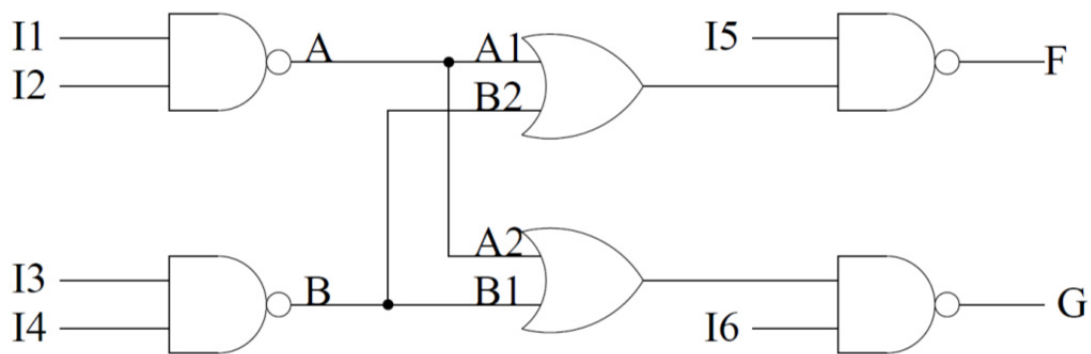(d) (4 pts) Consider the circuit given in Figure 2 below.

Figure 2: Circuit for Problem 1(d)

Tests shown in the table below are applied to this circuit. Indicate in the table if the single faults **A s-a-1** and **B s-a-1** will be detected or not by these tests. Give reasons.

Test #	I1	I2	I3	I4	I5	I6	A s-a-1	B s-a-1
1	0	1	1	1	0	1		
2	1	1	0	1	1	0		
3	0	1	0	1	1	1		
4	0	1	1	1	1	0		

(e) (2 pts) If a fault **f1** is equivalent to a fault **f2** and the fault **f1** dominates a fault **f3**, then which of these faults must be included in the reduced fault list for the purpose of fault detection. Give reasons.

(f) (8 pts) Check whether all single stuck-at faults in the circuit shown in Figure 3 are detectable. Recall that, in order to check this, it is sufficient to find tests for all primary inputs (**A**, **B** and **C**) and all fanout branches (marked by **D** and **E**). If faults on these lines are detectable, all faults are detectable. Fill the table below. Show all tests per fault. Do not use don't care symbol, always specify **A**, **B** and **C** to 0 or 1. If no test exists for a given fault, write "**−**".
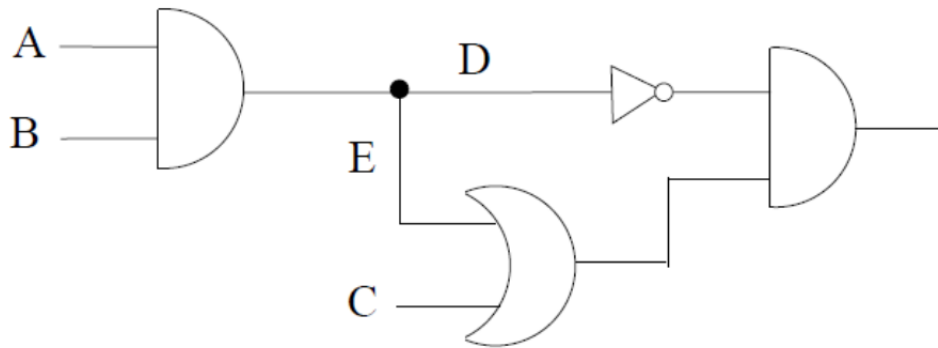

Figure 3: Circuit for Problem 1(f)

Stuck-at Fault	Test (a, b, c)
A s-a-0	
A s-a-1	
B s-a-0	
B s-a-1	
C s-a-0	
C s-a-1	
D s-a-0	
D s-a-1	
E s-a-0	
E s-a-1	

Problem 2: (20 pts) Consider the fanout free (tree) combinational circuit given below in Figure 4 and answer the questions related to this.
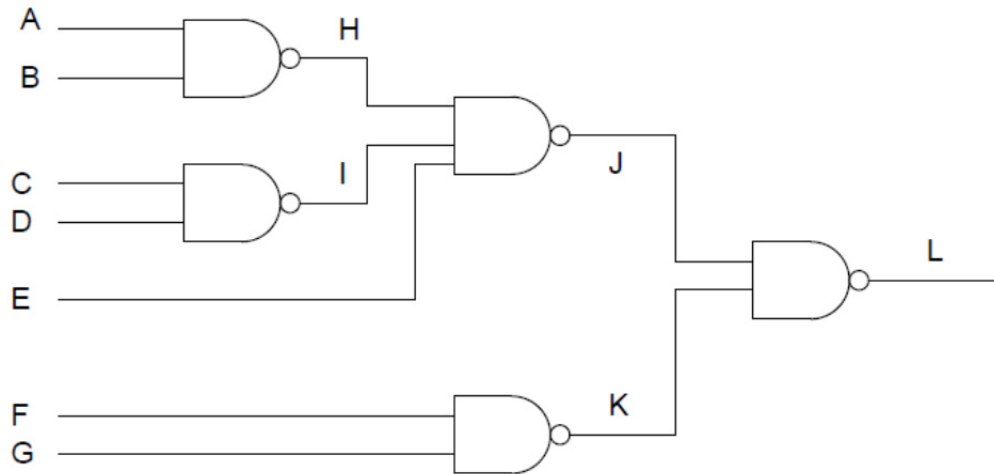

Figure 4: Circuit for Problem 2

(a) (2 pts) How many checkpoints does this circuit have? Give reasons.

(b) (10 pts) Write the collapsed fault list for the above circuit using the methods of checkpoint faults and fault equivalence reduction.
Note: Provide the number of faults and also the fault list in both cases.

(c) (3 pts) If in the Figure 4 all NAND gates were replaced by NOR gates, will the number of checkpoints change? Give reasons.

(d) (5 pts) Write the reduced faults if all gates were changed to AND gates in the circuit of Figure 4 and the fault list generation method consisted of checkpoint faults and fault equivalence method of fault reduction.
Note: Provide the number of faults and also the fault list in both cases.

Problem 3: (10 pts) Label the sequence of assignments made by the D-algorithm to generate a test for an **s-a-0** on the node indicated in Figure 5. Be sure to give the order and show the values for all nodes in the circuit.
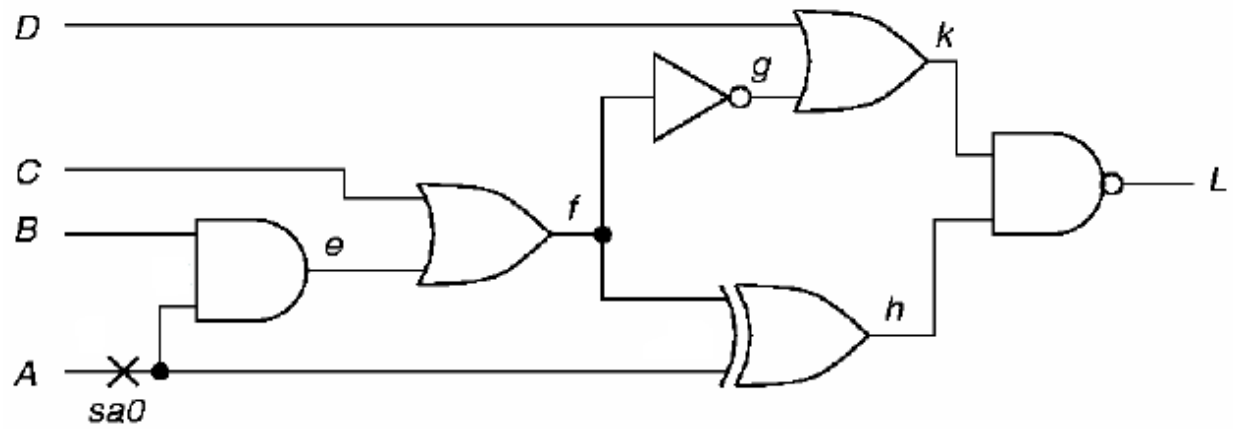

Figure 5: Circuit for Problem 3

Problem 4: (20 pts) Answer the following.

(a) (10 pts) In a certain coding scheme, when three consecutive **0s (zeros)** appear in a message, the receiver of the message knows that there has been a transmission error. Construct an FSM that gives a **0** as its current output bit if and only if the last three bits received are all **0s**.

(b) (10 pts) Implement the FSM in (a) in Verilog.

Problem 5: (10 pts) The logic in Figure 6 consists of three repeated parts. Write a Verilog explicit structural description of the logic which consists of two modules, one module, name it **partition**, will be for the part that's repeated, the other, name it **combine**, will instantiate **partition** three times and interconnect them appropriately. Choose appropriate inputs and outputs for the two modules based on the below diagram
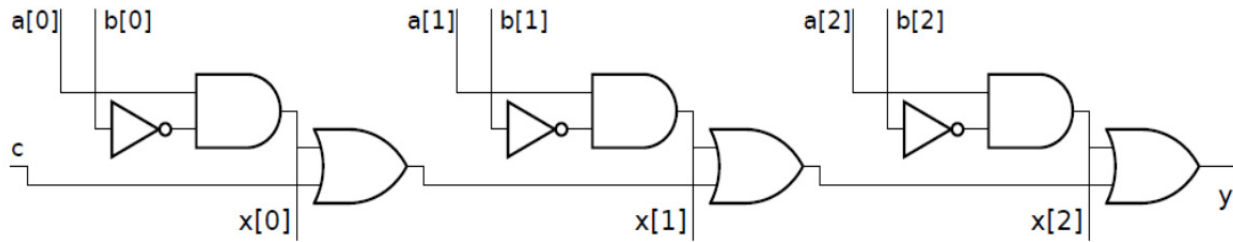

Figure 6: Circuit for Problem 5