



**University of Engineering and Technology (UET),
Peshawar, Pakistan**

Lecture 4

CSE-304: Computer Organization and Architecture

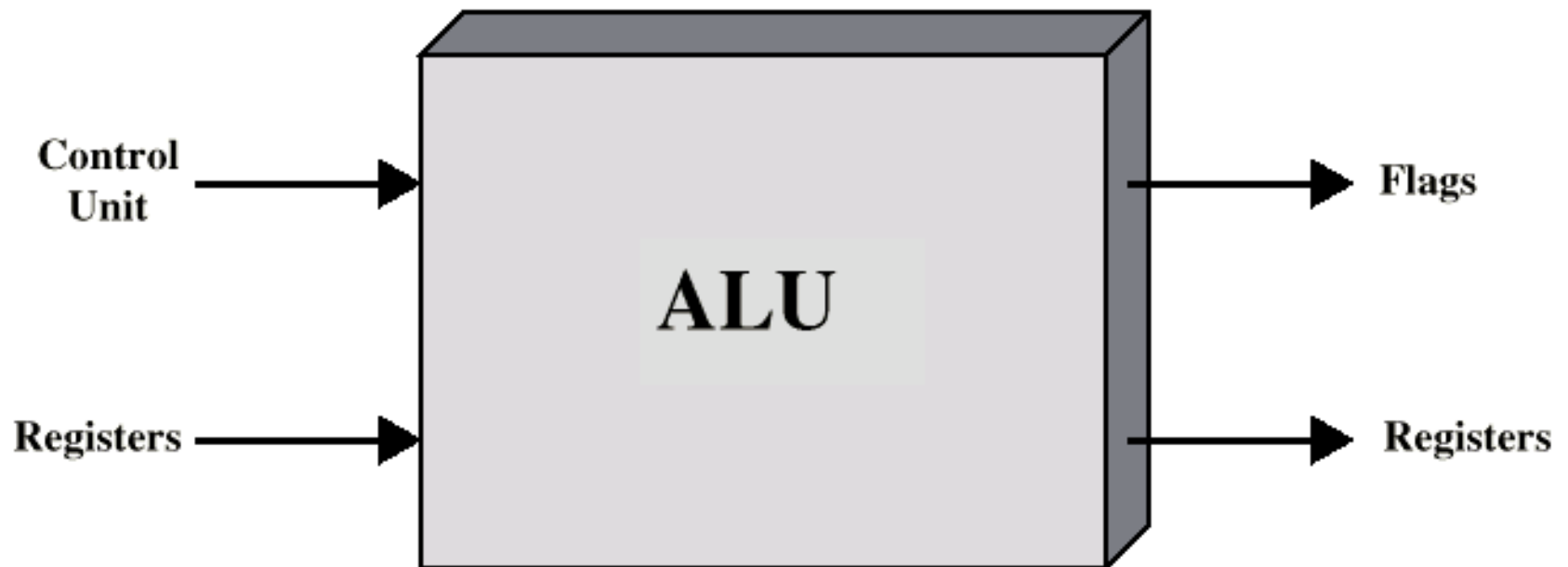
BY:

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Arithmetic & Logic Unit

- Does the calculations
- Everything else in the computer is there to service this unit
- Handles integers
- May handle floating point numbers
- May be separate FPU (maths co-processor)

ALU Inputs and Outputs



Integer Representation

- Only have 0 & 1 to represent everything
- Positive numbers stored in binary
 - e.g. $41 = 00101001$
- No minus sign
- No period
- Sign-Magnitude
- Two's complement

Sign-Magnitude

- Left most bit is sign bit
- 0 means positive
- 1 means negative
- $+18 = 00010010$
- $-18 = 10010010$
- Problems
 - Need to consider both sign and magnitude in arithmetic
 - Two representations of zero (+0 and -0)

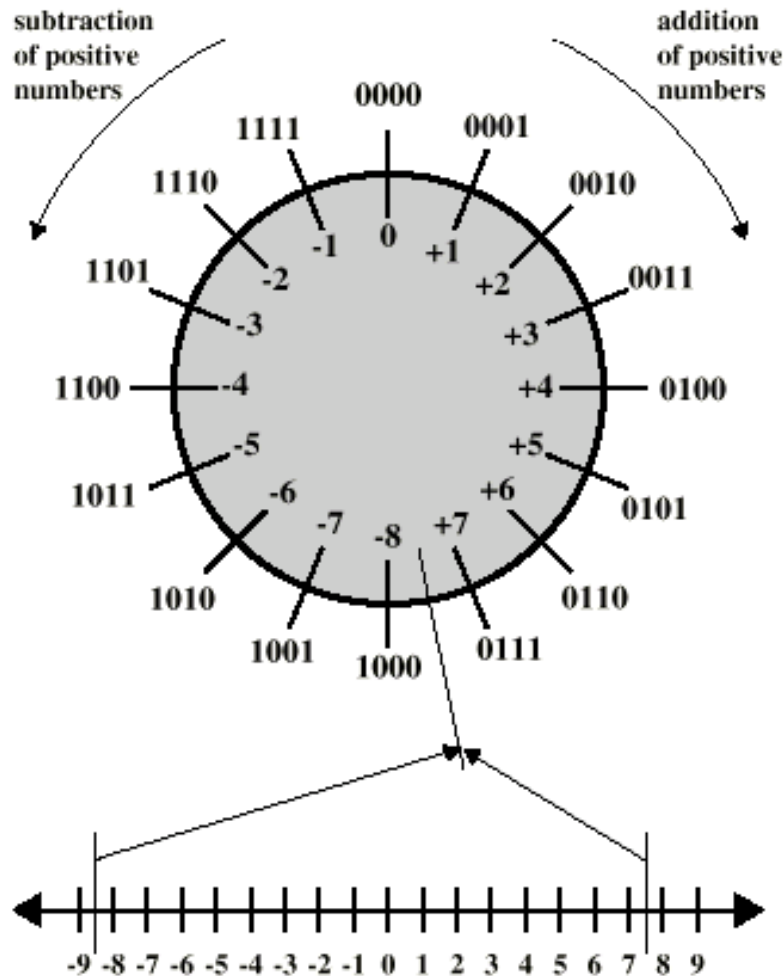
Two's Complement

- $+3 = 00000011$
- $+2 = 00000010$
- $+1 = 00000001$
- $+0 = 00000000$
- $-1 = 11111111$
- $-2 = 11111110$
- $-3 = 11111101$

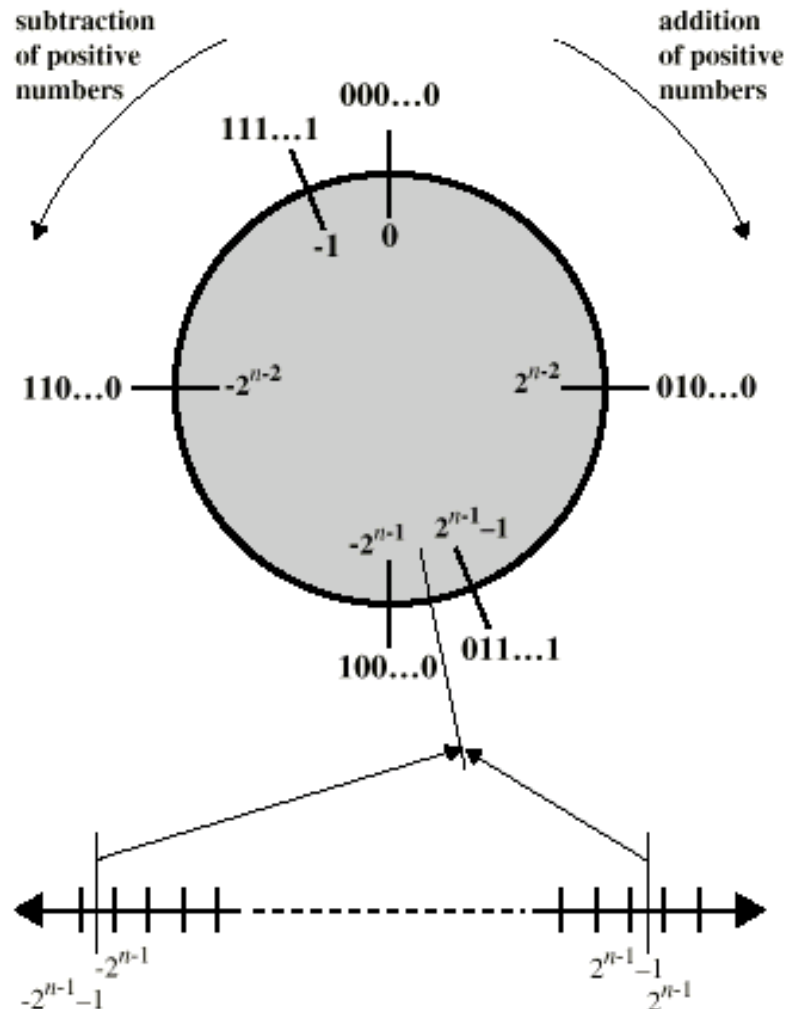
Benefits

- One representation of zero
- Arithmetic works easily
- Negating is fairly easy
 - $-3 = 00000011$
 - Boolean complement gives 11111100
 - Add 1 to LSB 11111101

Geometric Depiction of Twos Complement Integers



(a) 4-bit numbers



(b) n -bit numbers

Negation Special Case 1

- 0 = 00000000
- Bitwise not 11111111
- Add 1 to LSB +1
- Result 1 00000000
- Overflow is ignored, so:
- - 0 = 0

Negation Special Case 2

- $-128 = 10000000$
- bitwise not 01111111
- Add 1 to LSB $+1$
- Result 10000000
- So:
- $-(-128) = -128 \quad X$
- Monitor MSB (sign bit)
- It should change during negation

Range of Numbers

- 8 bit 2s compliment

- $+127 = 01111111 = 2^7 - 1$

- $-128 = 10000000 = -2^7$

- 16 bit 2s compliment

- $+32767 = 01111111 11111111 = 2^{15} - 1$

- $-32768 = 10000000 00000000 = -2^{15}$

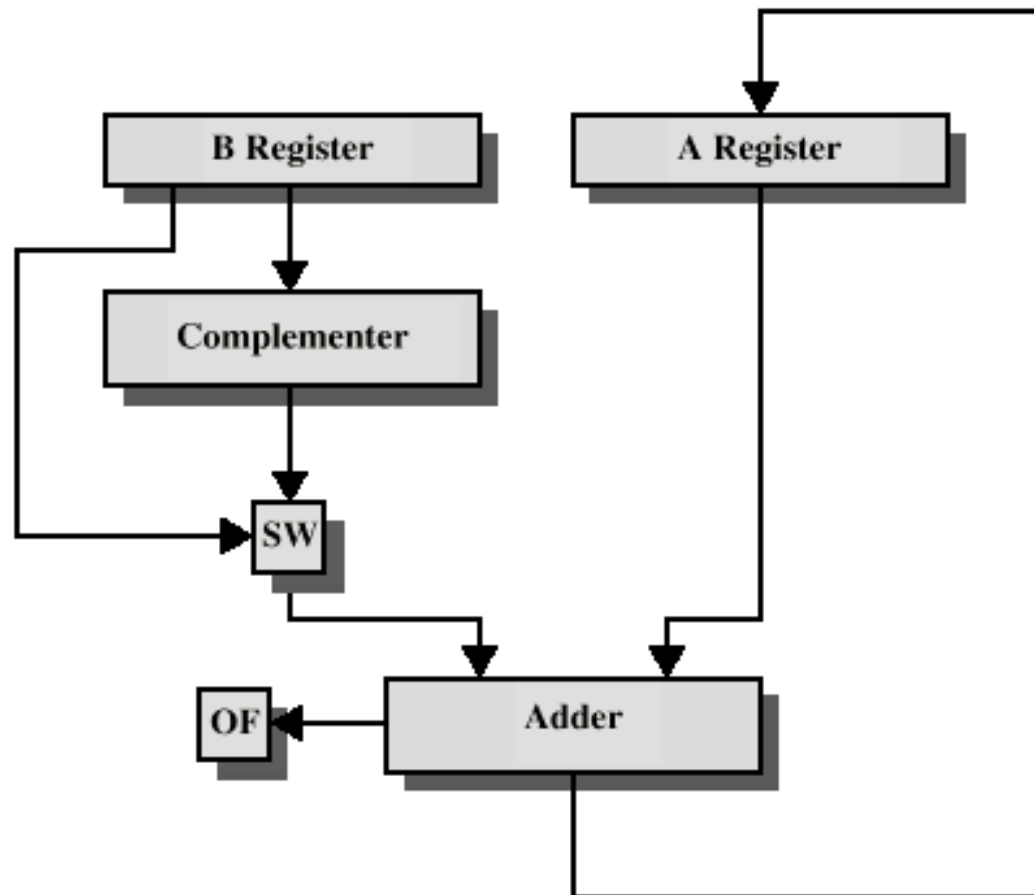
Conversion Between Lengths

- Positive number pack with leading zeros
- $+18 = \quad\quad\quad 00010010$
- $+18 = 00000000\ 00010010$
- Negative numbers pack with leading ones
- $-18 = \quad\quad\quad 10010010$
- $-18 = 11111111\ 10010010$
- i.e. pack with MSB (sign bit)

Addition and Subtraction

- Normal binary addition
- Monitor sign bit for overflow
 - Both number positive (no overflow) (e.g. 7+4)
 - Positive number with magnitude larger than negative number (overflow, discard carry) (e.g. 15-6)
 - Negative number with magnitude larger than positive number (no overflow) (e.g. 16-24)
 - Both numbers negative (overflow, discard carry) (e.g. -5-9)
- Take two's complement of subtrahend and add to minuend
 - i.e. $a - b = a + (-b)$
- So we only need addition and complement circuits

Hardware for Addition and Subtraction



OF = overflow bit

SW = Switch (select addition or subtraction)

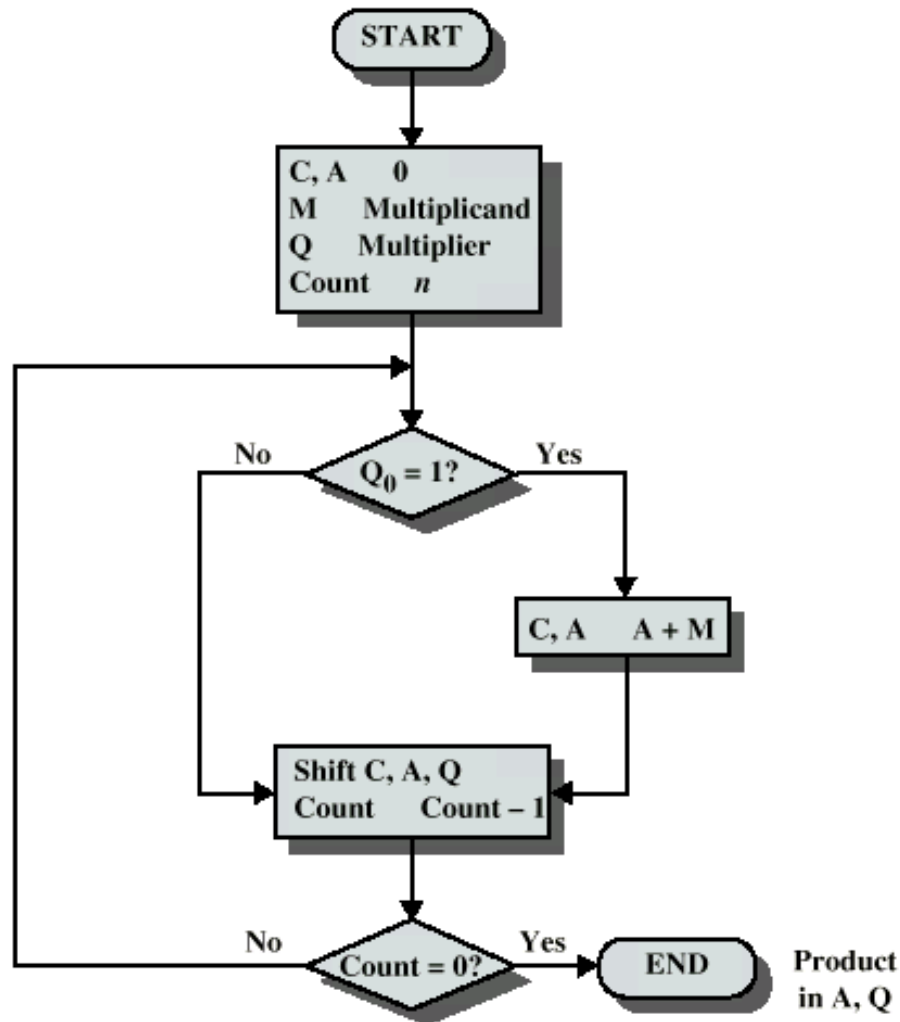
Multiplication

- Complex
- Work out partial product for each digit
- Take care with place value (column)
- Add partial products

Multiplication Example

- 1011 Multiplicand (11 dec)
- x 1101 Multiplier (13 dec)
- 1011 Partial products
- 0000 Note: if multiplier bit is 1 copy
- 1011 multiplicand (place value)
- 1011 otherwise zero
- 10001111 Product (143 dec)
- Note: need double length result

Flowchart for Unsigned Binary Multiplication



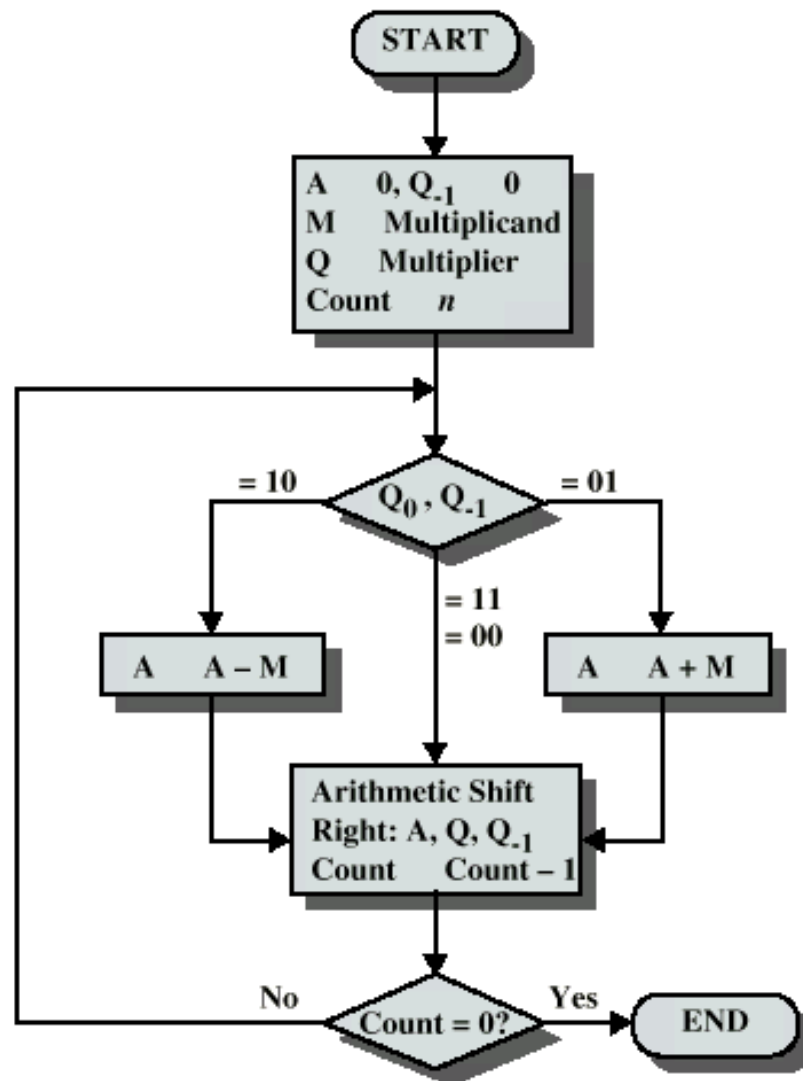
Execution of Example

C	A	Q	M		
0	0000	1101	1011	Initial Values	
0	1011	1101	1011	Add	} First Cycle
0	0101	1110	1011	Shift	
0	0010	1111	1011	Shift	} Second Cycle
0	1101	1111	1011	Add	
0	0110	1111	1011	Shift	} Third Cycle
1	0001	1111	1011	Add	
0	1000	1111	1011	Shift	} Fourth Cycle

Multiplying Negative Numbers

- Solution 1
 - Convert to positive if required
 - Multiply as above
 - If signs were different, negate answer
 - E.g. 9×3
- Solution 2
 - Booth's algorithm

Booth's Algorithm



Example of Booth's Algorithm

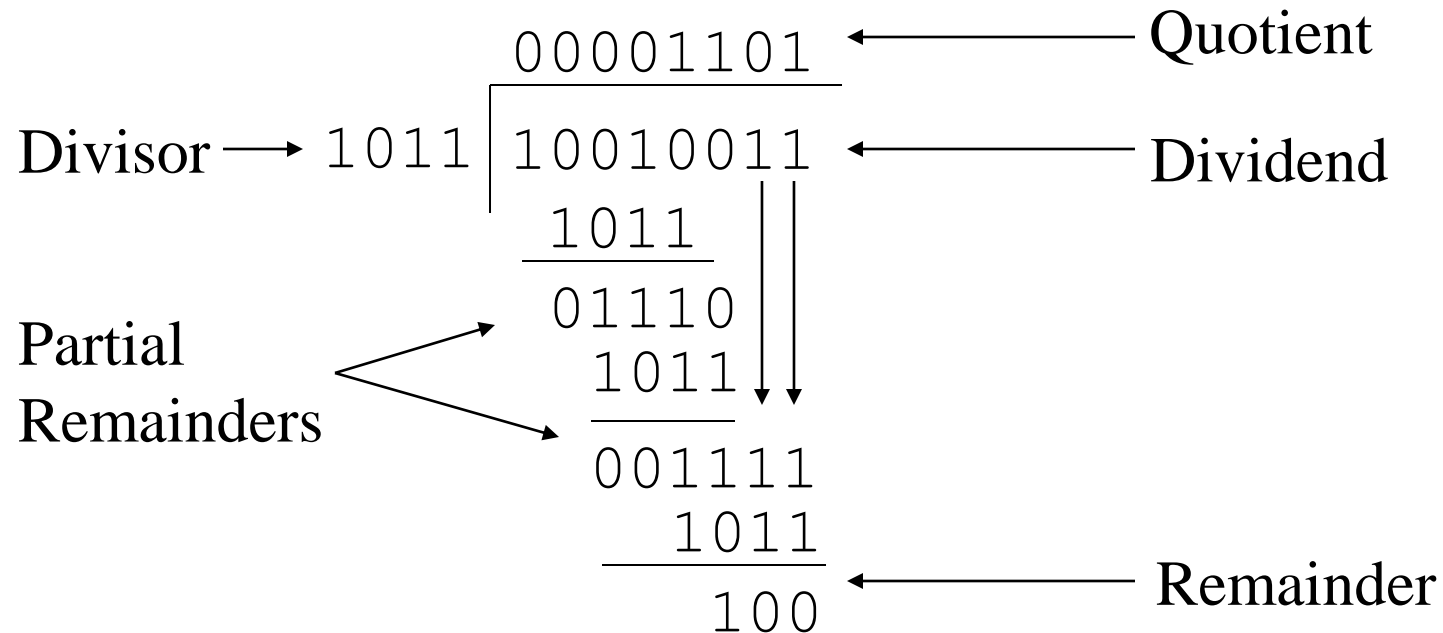
A	Q	Q ₋₁	M	Initial Values	
0000	0011	0	0111		
1001	0011	0	0111	A A - M	} First Cycle
1100	1001	1	0111	Shift	
1110	0100	1	0111	Shift	} Second Cycle
0101	0100	1	0111	A A + M	
0010	1010	0	0111	Shift	} Third Cycle
0001	0101	0	0111	Shift	
					} Fourth Cycle

Division

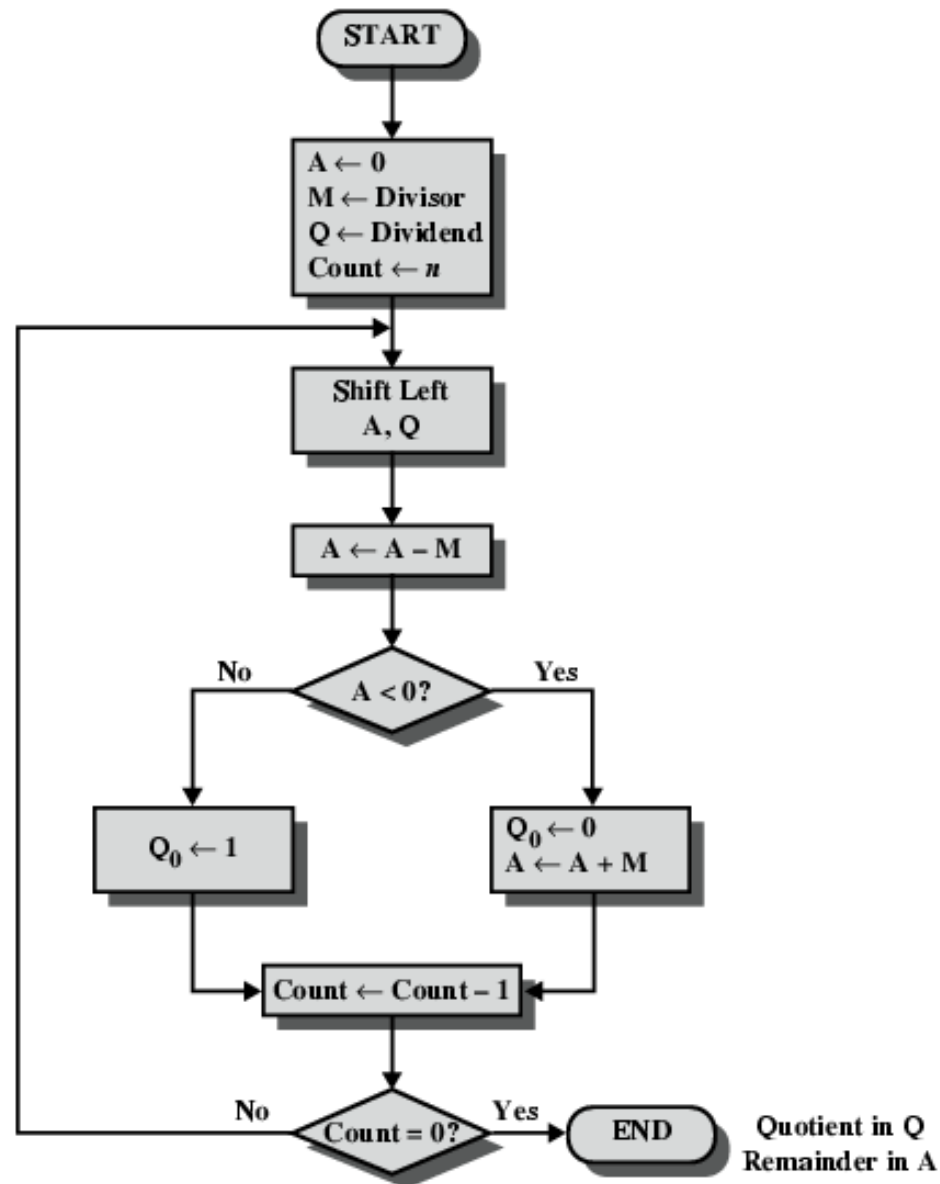
- More complex than multiplication
- Negative numbers are really bad!
- Based on long division

Division of Unsigned Binary Integers

Question: 147/11



Flowchart for Unsigned Binary Division



Steps for Signed Binary Division

1-Load the divisor into the M register and the dividend into the A, Q registers. The dividend must be expressed as a $2n$ -bit two's complement number. Thus, for example, the 4-bit 0111 becomes 00000111, and 1001 becomes 11111001.

2-Shift A, Q left 1 bit position.

3-If M and A have the same signs, perform $A=A-M$; otherwise, $A=A+M$.

4-The preceding operation is successful if the sign A is the same before and after the operation.

- a. If the operation is successful or $A=0$, then set $Q_0=1$.
- b. If the operation is unsuccessful and $A \neq 0$, then set $Q_0=0$ and restore the previous value of A.

5-Repeat steps 2 through 4 as many times as there are bit positions in Q.

6-The remainder is in A. If the signs of the divisor and dividend were the same, then the quotient is in Q; otherwise, the correct quotient is the two's complement of Q.

Example

A	Q	M = 0011	A	Q	M = 1101
0000	0111	Initial value	0000	0111	Initial value
0000	1110	shift	0000	1110	shift
1101		subtract	1101		add
0000	1110	restore	0000	1110	restore
0001	1100	shift	0001	1100	shift
1110		subtract	1110		add
0001	1100	restore	0001	1100	restore
0011	1000	shift	0011	1000	shift
0000		subtract	0000		add
0000	1001	set $Q_0 = 1$	0000	1001	set $Q_0 = 1$
0001	0010	shift	0001	0010	shift
1110		subtract	1110		add
0001	0010	restore	0001	0010	restore

(a) (7)/(3) (b) (7)/(-3)

A	Q	M = 0011	A	Q	M = 1101
1111	1001	Initial value	1111	1001	Initial value
1111	0010	shift	1111	0010	shift
0010		add	0010		subtract
1111	0010	restore	1111	0010	restore
1110	0100	shift	1110	0100	shift
0001		add	0001		subtract
1110	0100	restore	1110	0100	restore
1100	1000	shift	1100	1000	shift
1111		add	1111		subtract
1111	1001	set $Q_0 = 1$	1111	1001	set $Q_0 = 1$
1111	0010	shift	1111	0010	shift
0010		add	0010		subtract
1111	0010	restore	1111	0010	restore

(c) (-7)/(3) (d) (-7)/(-3)