*Name: _____

*Registration: _____

Department of Computer Systems Engineering
University of Engineering & Technology Peshawar

Digital System Design

CSE 308

Finalterm Examination Spring 2018
26 June 2018, Duration: 120 Minutes

Exam Rules

Please read carefully before proceeding.

1- This exam is CLOSED books/notes/computers/mobiles.
2- No calculators of any kind are allowed.
3- Answer all problems on the problem sheet.
4- There are 4 problems in total. Some problems are harder than
   others. Answer the easy ones first to maximize your score.
5- Questions will not be interpreted during the exam.
6- This exam booklet contains 9 pages, including this cover. Count them to be
   sure you have them all.

Problem 1 _____ (20 pts)

Problem 2 _____ (20 pts)

Problem 3 _____ (15 pts)

Problem 4 _____ (15 pts)

Exam Total _____ (70 pts)

Don't Panic!

Problem 1 [CLO-2]: (20 pts) Implement a sequence detector in Verilog using
a **behavioral description**. It should be a **Moore FSM**, in which the output is dependent
only on the state in which the FSM is and not the current input. The FSM must detect
the last two digits of your student ID (i.e. 15-pwcse-dd**dd**), encoded in binary, and **zero
extended** to 7 bits. For example, if the last two digits are 89, the FSM should detect 101
1001. If the last two digits are 03, the FSM should detect 000 0011. The FSM output
should be high only after the entire sequence has been detected.
Note: Please clearly indicate the sequence that your machine detects. Write a Verilog
module which would implement this FSM for input variable "in" and output variable
"out." Use the same standard format as was presented in the class. (Define your states;
use one always block for next state; use one always block for state transitions and
output.)

Problem 2 [CLO-3]: (20 pts) Consider the circuit in Fig. 1 based on the **single stuck-at fault** assumption and answer the questions related to this.
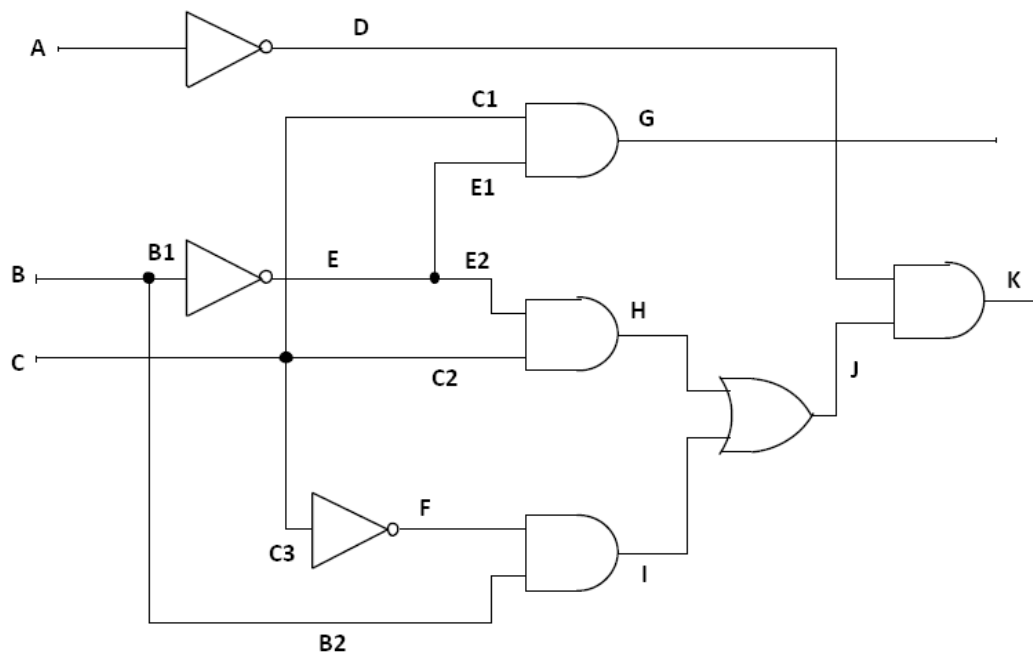

Fig. 1.

(a) (5 pts) What is the number of all possible faults?

(b) (5 pts) Write the reduced fault list using the method of fault equivalence reduction. What is the collapse ratio after you perform fault collapsing (based on the equivalent faults you find)?

(c) (5 pts) Write the reduced fault list using the method of fault dominance reduction. What is the collapse ratio after you perform fault collapsing (based on the dominance faults you find)?

(d) (5pts) How many checkpoint faults are in the circuit? How many of the checkpoint faults can be collapsed by fault equivalence and fault dominance relationships?

Problem 3 [CLO-3]: (15 pts) Consider the circuit in Fig. 2. Label the sequence of assignments made by the D-algorithm to generate a test for the **s-a-1** fault on line N. Be sure to give the order and show the values for all nodes in the circuit. To simplify the test generation process, whenever there is a choice, you first select the top input. For example, to justify M=1 in Fig. 2, you first justify I=1.
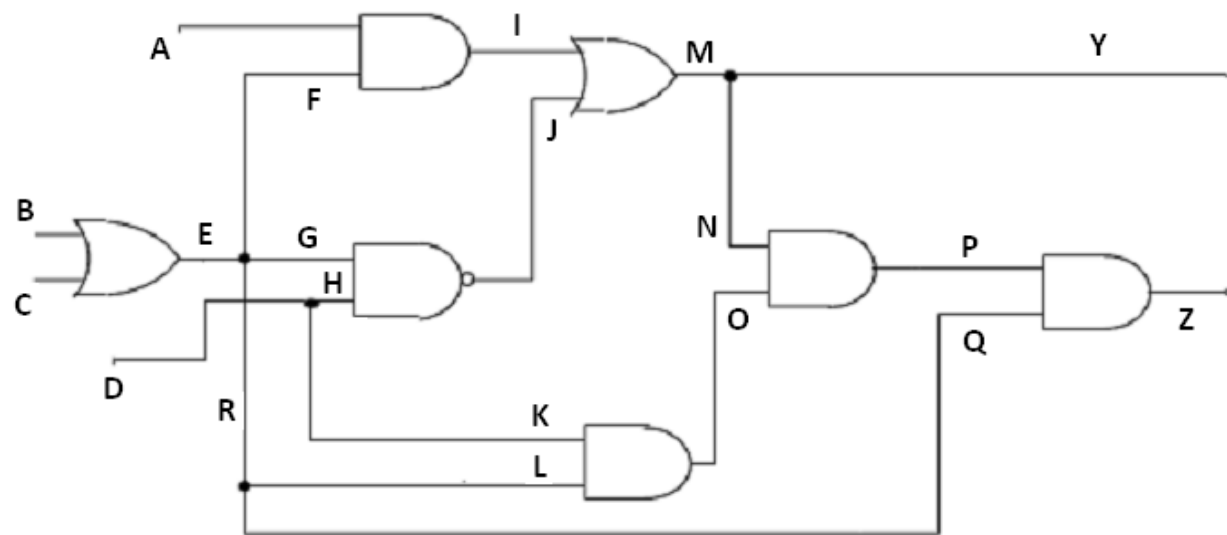
Fig. 2.

Problem 4 [CLO-3]: (15 pts) Using the circuit shown in Fig. 3, compute the set of all vectors that can detect each of the following faults using the Boolean difference.

(a) (5pts) e s-a-0
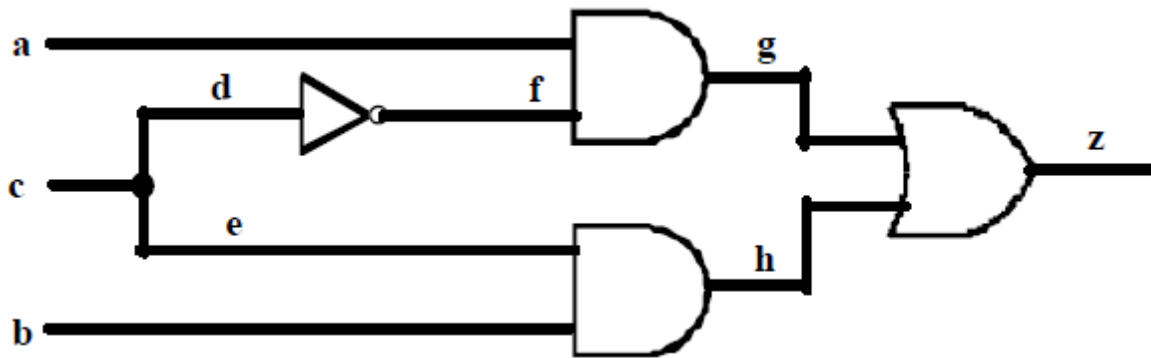(b) (5pts) e s-a-1
(c) (5pts) c s-a-0

Fig. 3.

<This page is intentionally left blank. This page can be used for scratch work or as extra space. If you write work here that you want me to grade, be sure to clearly indicate which problem(s) the work corresponds to!>