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Property 4	
TROBLEM I Draw the	logic circuit described
har ett a	Little described
by the verilog code	boonw.
	OC LO VV

module pie(x, \(\frac{1}{2}, \alpha, \beta, \cdot);

input a, b, (;

output x, \(\frac{1}{2};

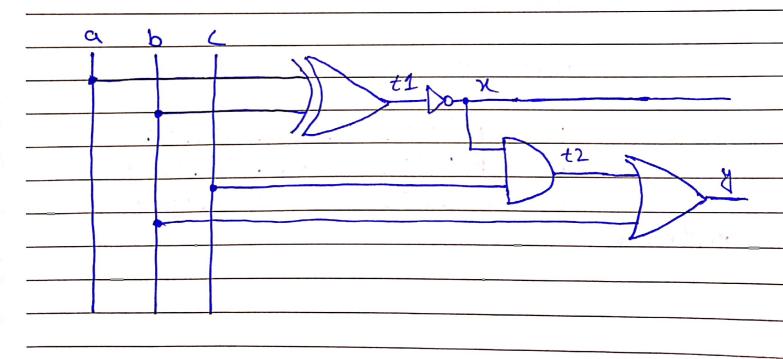
wire t1, t2;

XOY X1(t1, \alpha, \frac{1}{2};

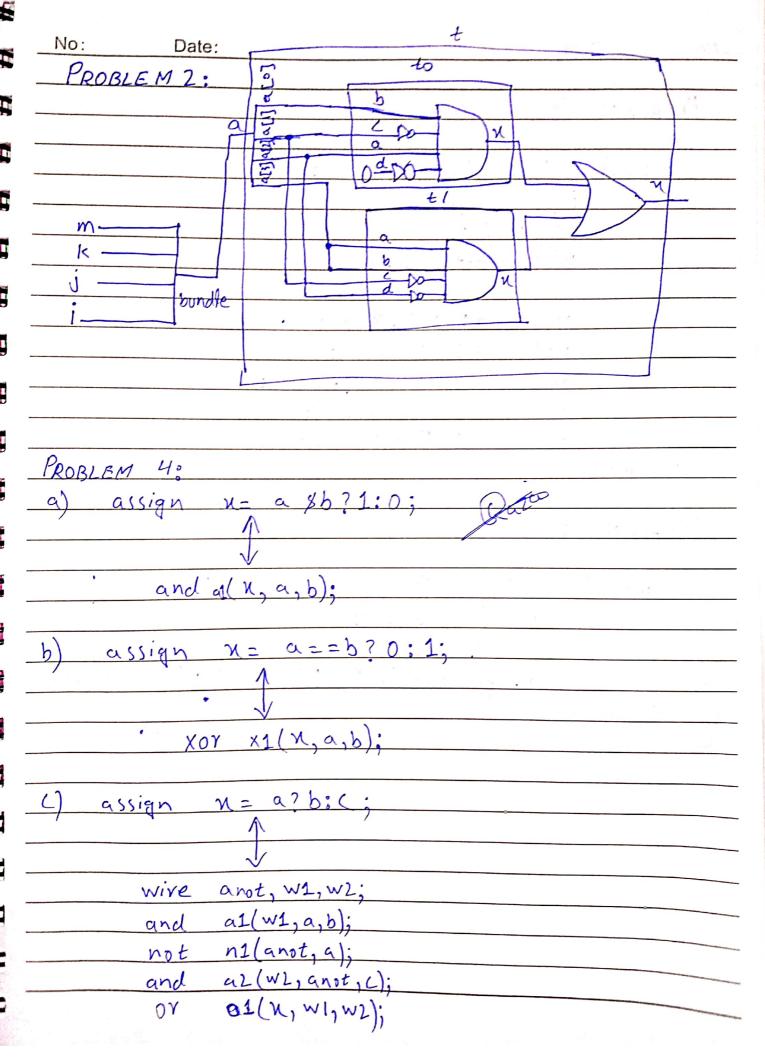
 $x_0 x_1(t_1, a, b);$ $x_1(t_1, a, b);$

endmodule

SOLUTION:



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PROBLEM 3:	
PARTS CARLOS SELECTIONS	-
module part(x, y, a, b, L);	1 1
ianut a l	
	27
output N. y;	
wive bnot;	
	8
and a1(x,a,bnot);	
or 01(4, x, c);	
end module gate	
WHOLE:	
module whole (x, y, a, b, C);	()
input [2:0] a, b=;	
Output [2:0] N;	100
input L;	
output y;	<u> </u>
wire w1, w2;	•
* - * * * * * * * * * * * * * * * * * *	1
part P1(x[0], w1, a.[0], b[0], ();	
part P2 (x[1], w2, a[1], b[1], w1);	i.
part: P3(N[2], 4, a[2], b[2], w2);	1.
	6
endmodule.	



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PROBLEM 5:	
module Logic (F, n, y, Z, w);	
input n,y,Z,W;	1. 50
output P;	•
wire Znot, w1, w2, w3;	:
	•
and a1(w1, x, y);	
not n1(Znot, Z);	-
and a2 (W2, N, y, Znot);	
1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	
or 01(F, w1, w2, w3); Qare	$\mathcal{L}_{}$
endmodule	
eramoaye	A.F
00 01 01 6	
PROBLEM 6:	
module Logic (F, x, y, Z, w);	
module Logic (F, x, y, Z, w);	
input Ny, Z, W;	*
output +;	11/x xxxx
output F; assign F = (x & y) (x & y & (~z)) (() ()
endmodule	
•	
	18
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