Practice Problem (4) (20 pts.)

Design an electronic lock system (**lockSys**, see Figure 1) for a garage door lock. The electronic lock accepts a 3-digit user code input, one digit at a time. If the input code sequence exactly matches 010, the electronic lock is opened (**openLock** is asserted). If any part of the 3-digit code input sequence is incorrect, the **Alarm** is activated and the user is forced to restart code entry i.e. all backward arcs go back to the initial state if a "wrong" digit is entered. When **openLock** is asserted after the correct code has been entered, the lock stays open. And the lock shuts itself (**openLock** is de-asserted) if the asynchronous input signal **rst** is asserted or a 0/1 is entered after the correct input code sequence, until the correct input code is again entered.

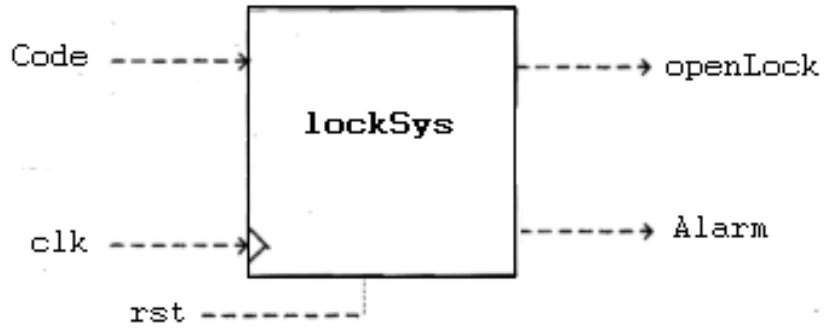

Figure 1. Electronic Lock System (lockSys)

(a) Design a Mealy/Moore FSM for **lockSys**. **(10 pts.)**

(b) Implement the FSM in **(a)** in Verilog. **(10 pts.)**