No: Date:

Name : Shah Raza

Reg No : 18PWCSE1658

Section : B

Subject : DSD

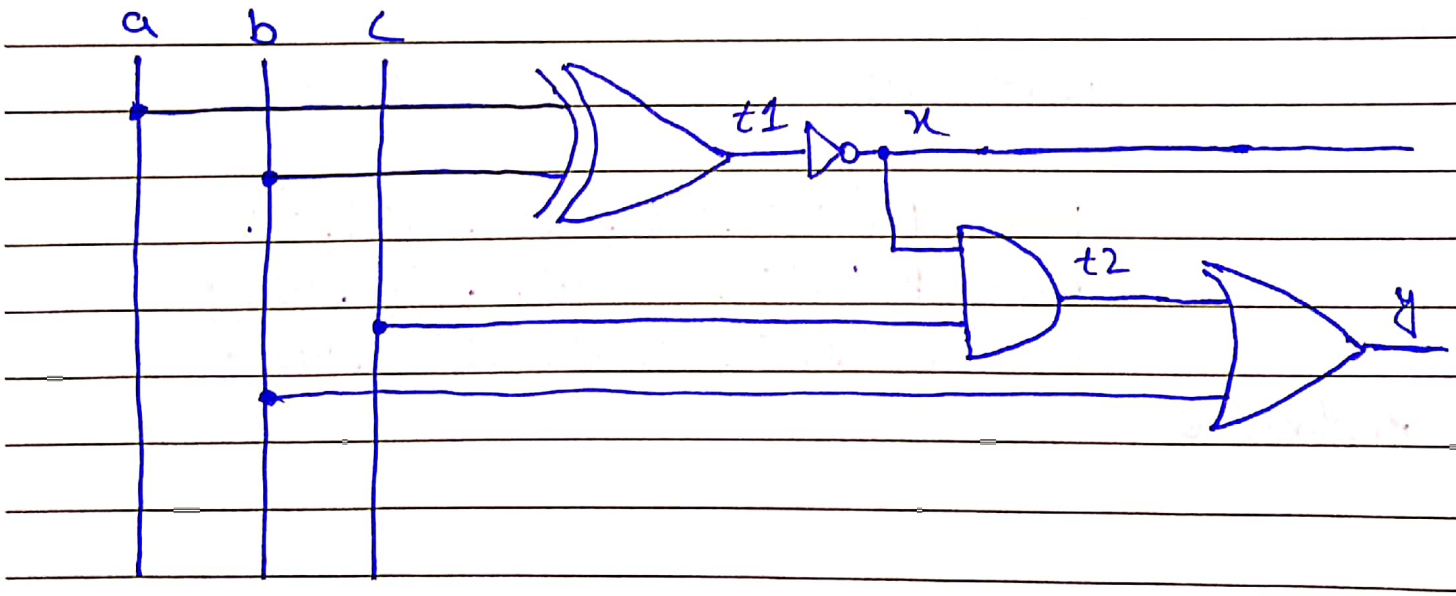
Assignment No : 1

No: Date:

PROBLEM 1: Draw the logic circuit described by the verilog code below.

```
module piel(x, y, a, b, c);
    input a, b, c;
    output x, y;
    wire t1, t2;
    xor  x1(t1, a, b);
    not  n1(x, t1);
    and  a1(t2, x, c);
    or   o1(y, t2, b);
endmodule
```

SOLUTION:



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PROBLEM 3:

PART:

```
module part(x,y,a,b,c);
input a,b,c;
output x,y;
wire bnot;

and a1(x,a,bnot);
or o1(y,x,c);
endmodule
```

WHOLE:

```
module whole(x,y,a,b,c);
input [2:0] a,b;
output [2:0] x;
input c;
output y;
wire w1,w2;

part p1(x[0],w1,a[0],b[0],c);
part p2(x[1],w2,a[1],b[1],w1);
part p3(x[2],y,a[2],b[2],w2);
endmodule
```

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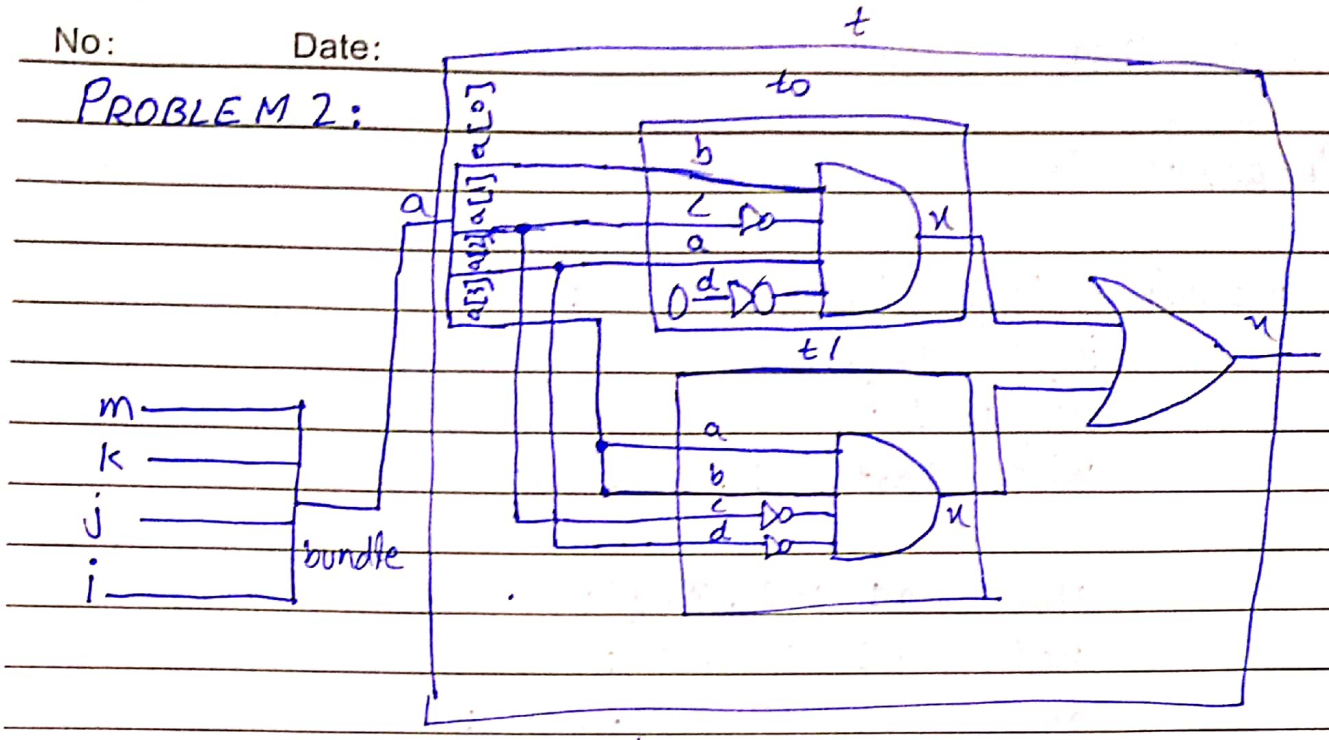
PROBLEM 2:



PROBLEM 4:

a) assign x = a && b ? 1 : 0;

↕

and a1(x, a, b);

b) assign x = a == b ? 0 : 1;

↕

xor x1(x, a, b);

c) assign x = a ? b : c;

↕

```
wire anot, w1, w2;
and  a1(w1, a, b);
not  n1(anot, a);
and  a2(w2, anot, c);
or   o1(x, w1, w2);
```

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PROBLEM 5:

```
module Logic(F, x, y, z, w);
    input x, y, z, w;
    output F;
    wire Znot, w1, w2, w3;

    and  a1(w1, x, y);
    not  n1(Znot, z);
    and  a2(w2, x, y, Znot);
    and  a3(w3, x, y, w);
    or   o1(F, w1, w2, w3);
endmodule
```

PROBLEM 6:

```
module Logic(F, x, y, z, w);
    input x, y, z, w;
    output F;
    assign F = (x & y) | (x & y & (~z)) | (x & y & w);
endmodule
```