Practice Problems on Memory Management

Problem 1

In a system there are 3 processes- P1 (10 bytes), P2 (6 bytes) and P3 (8 bytes) with page size of 2 bytes. Size of the main memory is 32 bytes. Page tables of processes are given below.

Page Tables					
Process P1		Process P2		Process P3	
p	f	p	f	p	f
0	7	0	15	0	2
1	12	1	13	1	6
2	1	2	9	2	3
3	5			3	8
4	4				

Find corresponding physical addresses of the following logical addresses:

a. Address 01001 of P1.
b. Address 00100 of P1.
c. Address 00111 of P1.
d. Address 00001 of P2.
e. Address 00100 of P2.
f. Address 10101 of P2.
g. Address 00010 of P3.
h. Address 11011 of P3.
i. Address 00110 of P3.

Answer:

a. 9 b. 2 c. 11 d. 31 e. 18 f. Invalid page number g. 12 h. Invalid page num. l i. 16

Problem 2

During TLB search, the associative lookup time (ε) is 3ns and hit ratio (α) is 70%. For each time memory access, 80ns is needed. Calculate the effective access time.

Answer:
107ns

Problem 3

During TLB search, the associative lookup time (ε) is 5ns and hit ratio (α) is 65.5%. For each time memory access, 200ns is needed. Calculate the effective access time.

Answer:
274ns

Problem 4

Consider logical address of a process is **118 bits** and the page size of the system is **16 KB**. Size of each entry in the page table is **8 Bytes**. Apply Hierarchical Paging or Two-Level Paging technique in order to fit the pages of the process in the main memory and illustrate the logical address space of the process including the necessary outer page bits, inner page bits and offset bits of every step during the paging technique.

Problem 5

A process runs in a system with single level paging and it has a logical address space of 8 bits. In the system page size is 16 Bytes and size of the main memory is 512 Bytes. Page table of the process is given below:

PMT		
Page #	Frame #	valid/invalid bit
0	5	v
1		i
2	12	v
3	3	v
4	25	v
5		i
6	0	v
7	18	v
8		i
9	31	v
10	7	v
11		i
12	21	v
13	9	v
14		i
15	14	v

When the CPU is executing the process it generates the following logical addresses: 3, 90, 167 and 241. Map the corresponding physical addresses of these logical addresses.

Answer:

3 => 83, 90 => invalid, 167 => 119, 241 => 225

Problem 6

A process runs in a system with multi level paging and it has a logical address space of 8 bits. In the system page size is 16 Bytes, size of each entry of the page table is 4 Bytes and size of the main memory is 512 Bytes. In order to fit the pages of the process in the main memory the OS applies two-level paging technique in outer page number bits of the logical address space until the outer most page table can be allocated in a frame of the main memory.

I. Illustrate the logical address space of the process including the necessary outer page bits, inner page bits and offset bits of every step with proper mathematical calculations during the paging mechanism of the system described above.

II. In this system, if the CPU generates logical addresses 179 and 90 then map the corresponding physical addresses of these logical addresses.
Necessary page table information is given below:

Outer page table		
Page #	Frame #	valid/invalid bit
0		i
1	6	v
2	11	v
3		i

Inner page tables					
PMT at frame 6			PMT at frame 11		
Page #	Frame #	valid/invalid bit	Page #	Frame #	valid/invalid bit
0	3	v	0	25	v
1	20	v	1		i
2		i	2	12	v
3	7	v	3	14	v

Problem 7

A process runs in a system with multi level paging and it has a logical address space of 16 bits. In the system page size is 16 Bytes, size of each entry of the page table is 2 Bytes and size of the main memory is 1 KB. In order to fit the pages of the process in the main memory the OS applies two-level paging technique in outer page number bits of the logical address space until the outer most page table can be allocated in a frame of the main memory.

III. Illustrate the logical address space of the process including the necessary outer page bits, inner page bits and offset bits of every step with proper mathematical calculations during the paging mechanism of the system described above.

IV. In this system, if the CPU generates logical addresses 49461 and 13742 then map the corresponding physical addresses of these logical addresses.
Necessary page table information is given below:

3rd outer PMT		
Page #	Frame #	valid/invalid bit
0		
1	2	v
2		
3		
4		
5		
6	3	v
7		

2nd outer PMT						Outer PMT						Inner PMT					
Frame 2			Frame 3			Frame 13			Frame 22			Frame 28			Frame 48		
Page #	Frame #	valid/invalidbit	Page #	Frame #	valid/invalidbit	Page #	Frame #	valid/invalidbit	Page #	Frame #	valid/invalidbit	Page #	Frame #	valid/invalidbit	Page #	Frame #	valid/invalidbit
0			0	22	v	0			0			0			0		
1	9	v	1			1			1			1			1		
2			2			2			2	48	v	2	60	v	2		
3			3			3	28	v	3			3			3	56	v
4			4			4			4			4			4		
5	13	v	5			5	29	v	5	49	v	5	61	v	5	57	v
6			6	24	v	6			6			6			6		
7			7			7			7			7			7		

Problem 8

In a system, there are 4 frames in the main memory. In a particular scenario main memory needs to accommodate 16 pages according to the order of the given reference string.

[1 5 4 3 0 4 7 1 2 9 1 2 7 3 1 7]

Apply FIFO, LRU and Optimal page replacement algorithms in order to accommodate the pages in the main memory and find out page hit ratio and page fault ratio of every algorithm. Lastly, logically explain which algorithm performs better for the given scenario.

Answer:

FIFO=> Hit ratio: 31.25%, Fault ratio: 68.75%

LRU=> Hit ratio: 37.5%, Fault ratio: 62.5%

Optimal=> Hit ratio: 43.7 5%, Fault ratio: 56.25%

For this scenario, optimal performs better.