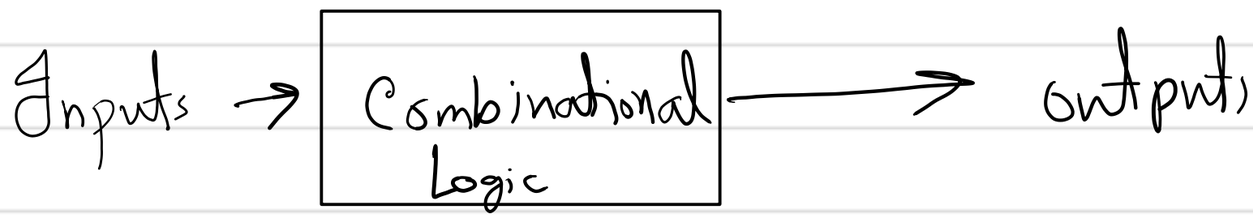
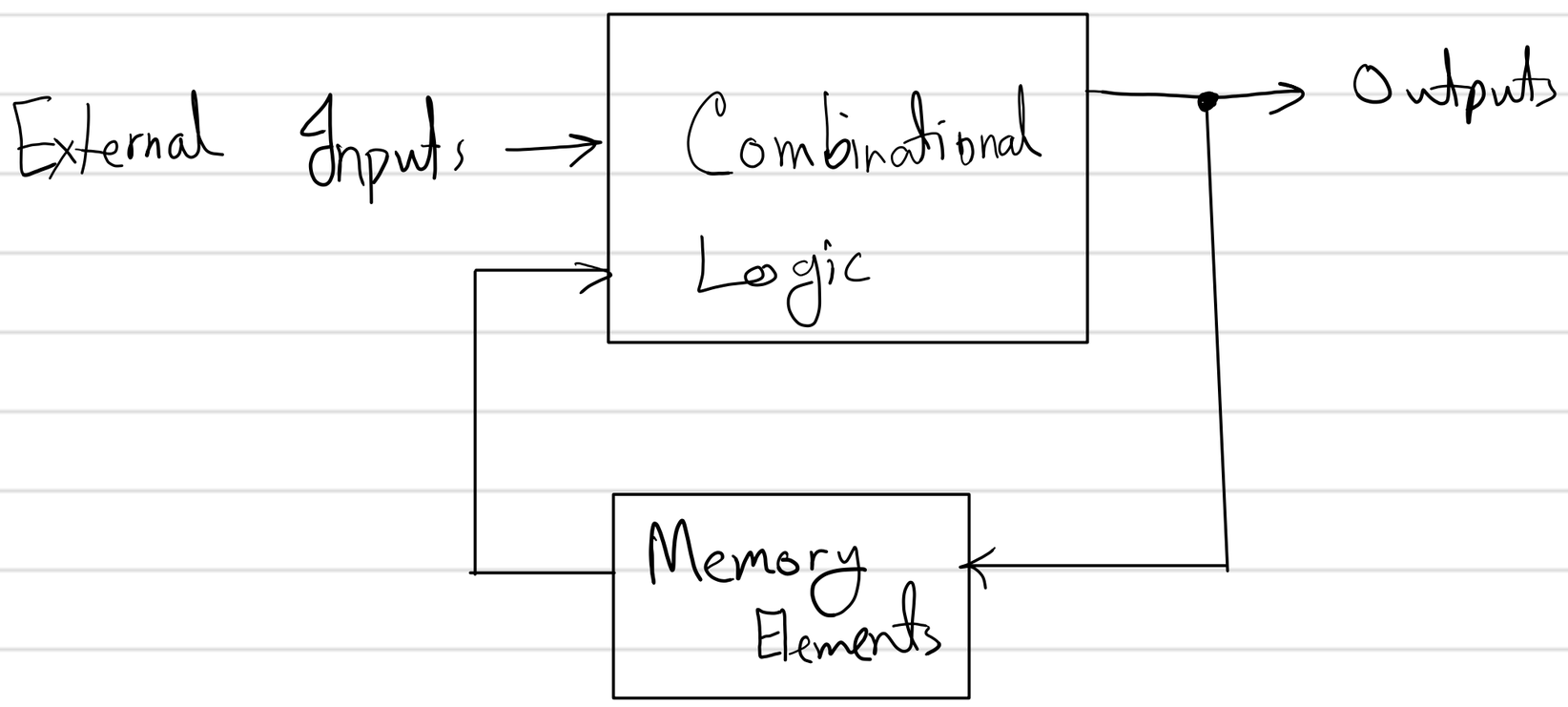
Lecture Note 9

Sequential Circuit

Combinational Circuits:



Sequential Circuits:



$$\text{Output}_s\left[Y(t+1)\right] = \text{External Inputs} + \text{Present state}\left[Y(t)\right]$$

Sequential circuits:

2 types: Synchronous: Output changes only at specific time. (Clock pulse)

Asynchronous: Output changes at any time. (Whenever we change inputs, doesn't depend on clock pulse.

Multivibrator: A type of sequential circuit with different stability properties.

1. Astable: No stable state. Continuously switches.

Example: Clock pulse generator

2. Monostable: (1 stable state, another is temporary.)

Ex: When we punch our id card at Bracu, the gate opens. After a while the gate automatically closes.

if gate open = 1, and close = 0

then stable state is 0 (close)

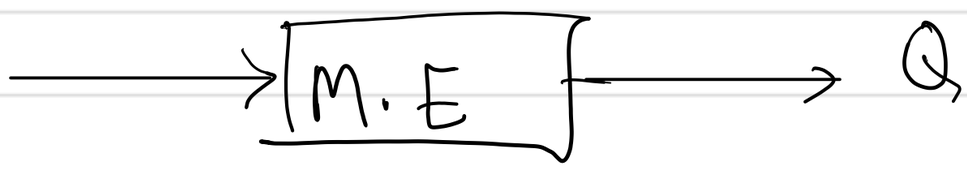
temporary " " 1 (open)

* (3) Bistable: 2 stable states (0,1).

Ex: Flipflop

Memory Elements:

→ A device that can remember value indefinately or change values in command.



Q(t) = present state / current state / Q

Q(t+1) = next state. / Q^+

To understand flipflop, we need to start from Latch.

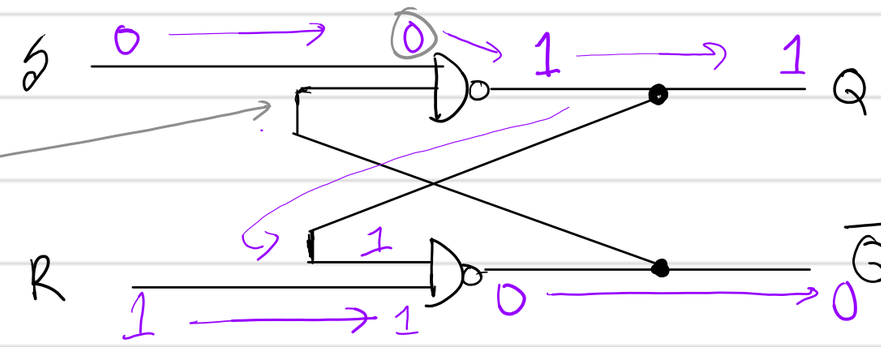
SR Latch (using NAND gate):

← Q(t)

← $\overline{Q}(t)$

Deriving Truthtable:

Case 1:



We dont need to know as one input is 0

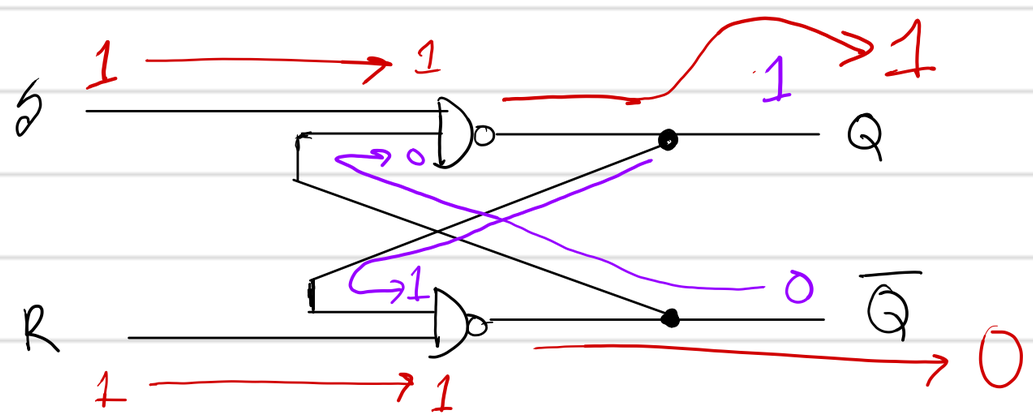
NAND

X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

∴ output 1 if any input = 0.

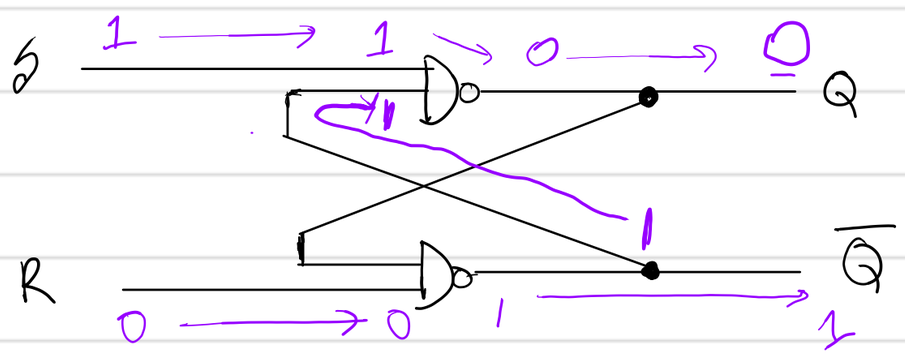
$S = 0$ $R = 1$ $Q = 1$ $\overline{Q} = 0$

next iteration,



$S = 1$ $R = 1$ $Q = 1$ $\overline{Q} = 0$

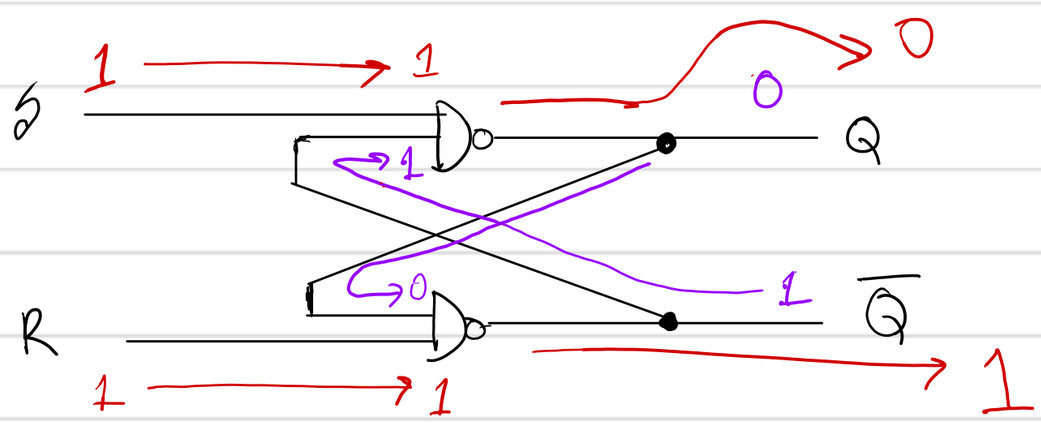
Case 2:



We dont need to know as one input is 0

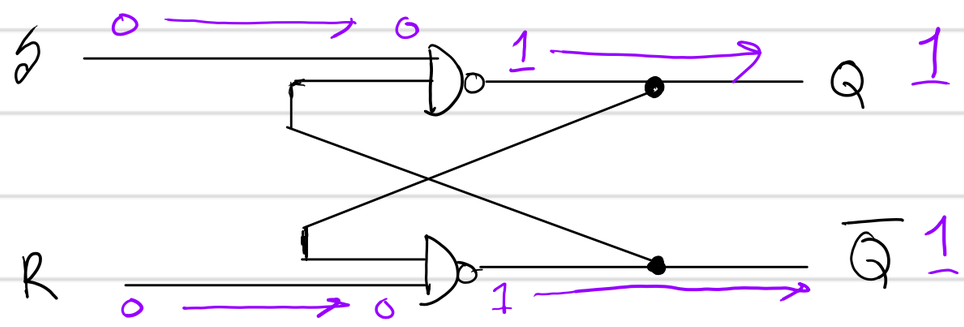
$S = 1$ $R = 0$ $Q = 0$ $\overline{Q} = 1$

next iteration,



$S = 1$ $R = 1$ $Q = 0$ $\overline{Q} = 1$

Case 3:



$S = 0$ $R = 0$ $Q = 1$ $\overline{Q} = 1$

Q & $\overline{Q}$ cant be one at the same time.

∴ Invalid / Not used

∴ Truth table:

S	R	Q	$\overline{Q}$
0	0	Invalid / Not used	
0	1	1	0
1	0	0	1
1	1	memory	

Difference Between SR Latch & flipflop:

* Latch: Input can be changed at any time
* Flipflop: Input can be changed only when clk = 1 or high.

Flipflops

We will learn about SR, D, JK & T flipflops.

We need to know their,

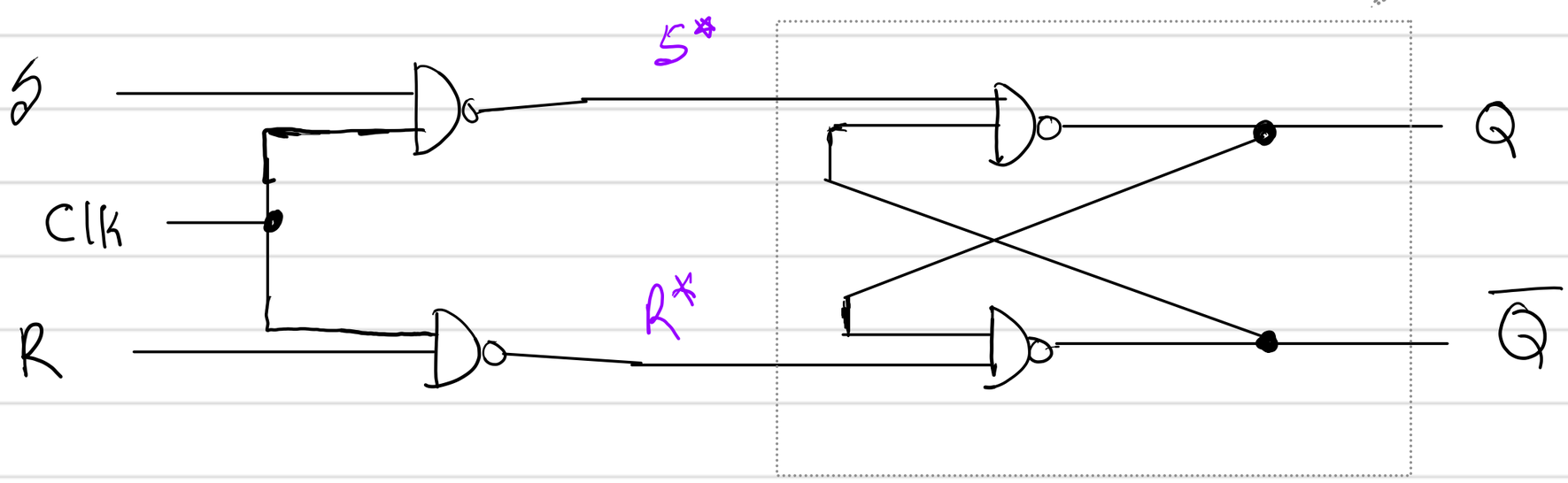
→ Circuit & Block Diagram

→ Truth table (Inputs | outputs)

→ Characteristic table (Present state + Input | next state)

→ Excitation table (Present state + Next state | Inputs)

SR Flipflop



$$S^* = (S \cdot clk)' = S' + clk' = S' + 1' = S' + 0 = S'$$

$$R^* = (R \cdot clk)' = R' + clk' = R' + 1' = R' + 0 = R'$$

Since, FF only work when clk = 1

Truth table:

This is written only to understand. On exams, you can skip S^* & R^*

S	R	S^*	R^*	Q	$\overline{Q}$
0	0	1	1	memory/no change	
0	1	1	0	0	1
1	0	0	1	1	0
1	1	0	0	not used	

Characteristic Table:

(Depending on flipflops inputs & present state, what would be the next state?

Present state Q(t)	inputs S	R	next state Q(t)+1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	not used
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	not used

Excitation Table:

* Analyzing the flipflop present & next state, we try to determine the inputs. (we fill the input column by analysing characteristic table.

Present state | next state | inputs

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

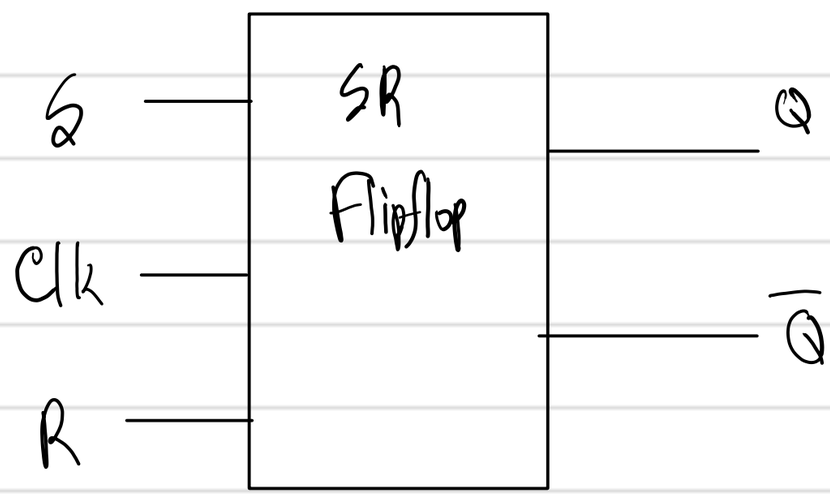
Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	not used
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	not used

∴ Excitation table

Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

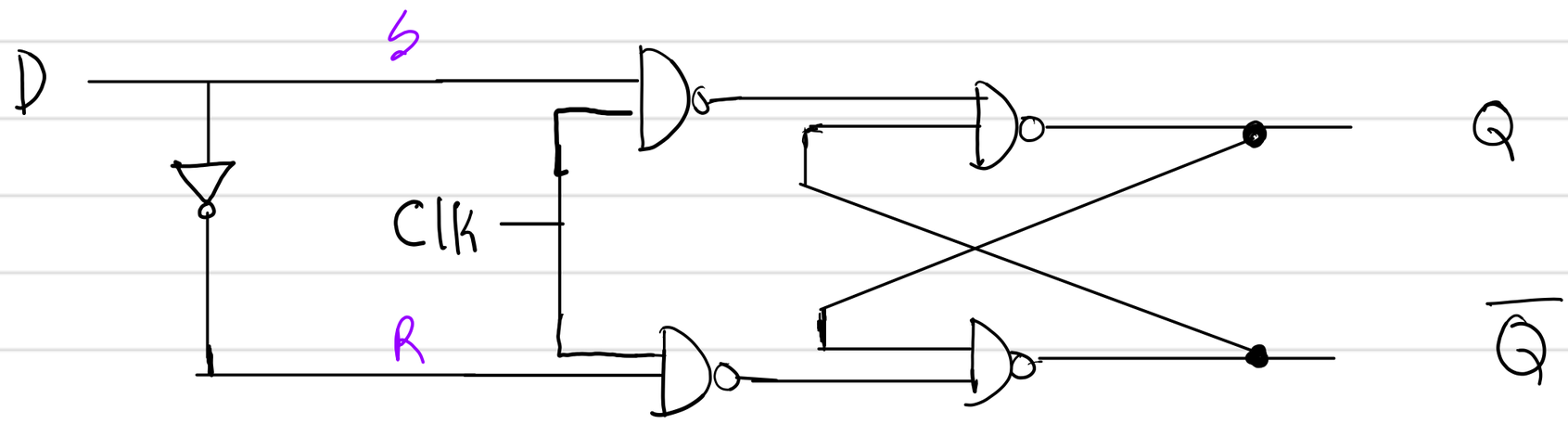
If we have different value for S or R in different rows, then we write X, Dont care

Block Diagram:



D Flipflop:

→ Motivation : SR has invalid input which can be removed.



we merged S & R using NOT Gate and call it D.

Then, $D = S$

$D = R = S'$

Truthtable:

D	Q	$\overline{Q}$
0	0	1
1	1	0

Characteristic Table:

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

next state doesn't depend on Q(t)/ present state.

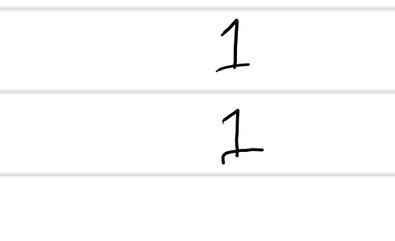
∴ It doesn't have memory state.

Excitation Table:

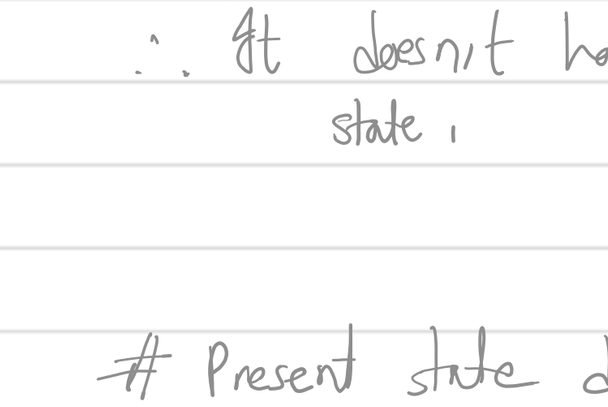
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present state doesn't matter

Block Diagram:



using SR,



JK Flipflop:

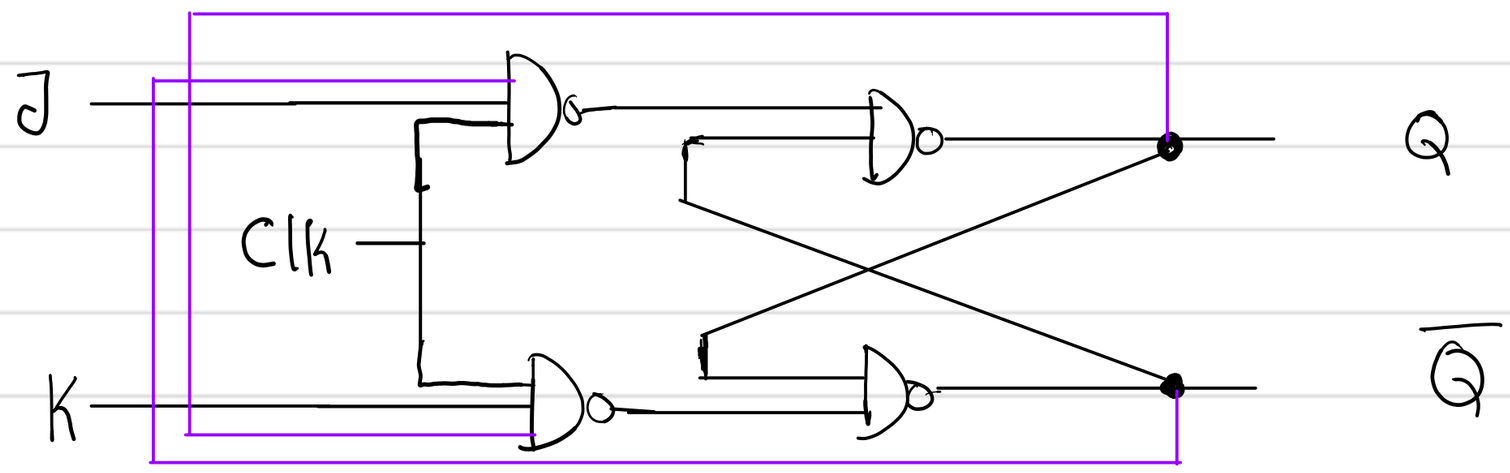
Motivation: SR FF has invalid state / unwed input (11)

D FF has no present state / memory

JK Flipflop has a new output, Toggle.

↳ next state = previous state

$Q(t+1) = [Q(t)]'$



Truthtable:

J	K	Q	$\overline{Q}$
0	0	Memory	
0	1	0	1
1	0	1	0
1	1	Toggle	

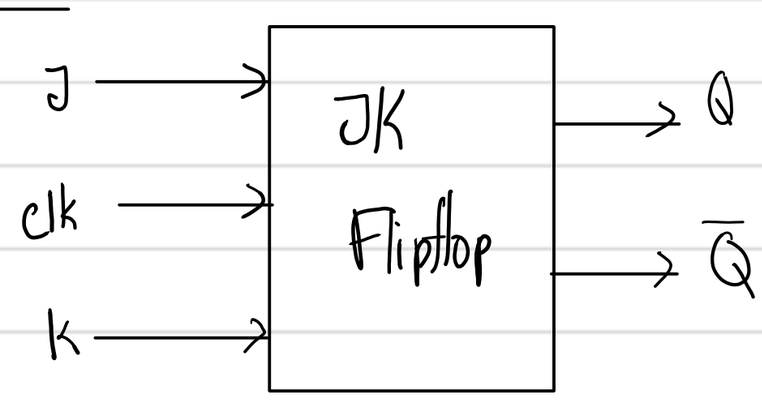
Characteristic Table:

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table:

Q(t)	Q(t+1)	J	k
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

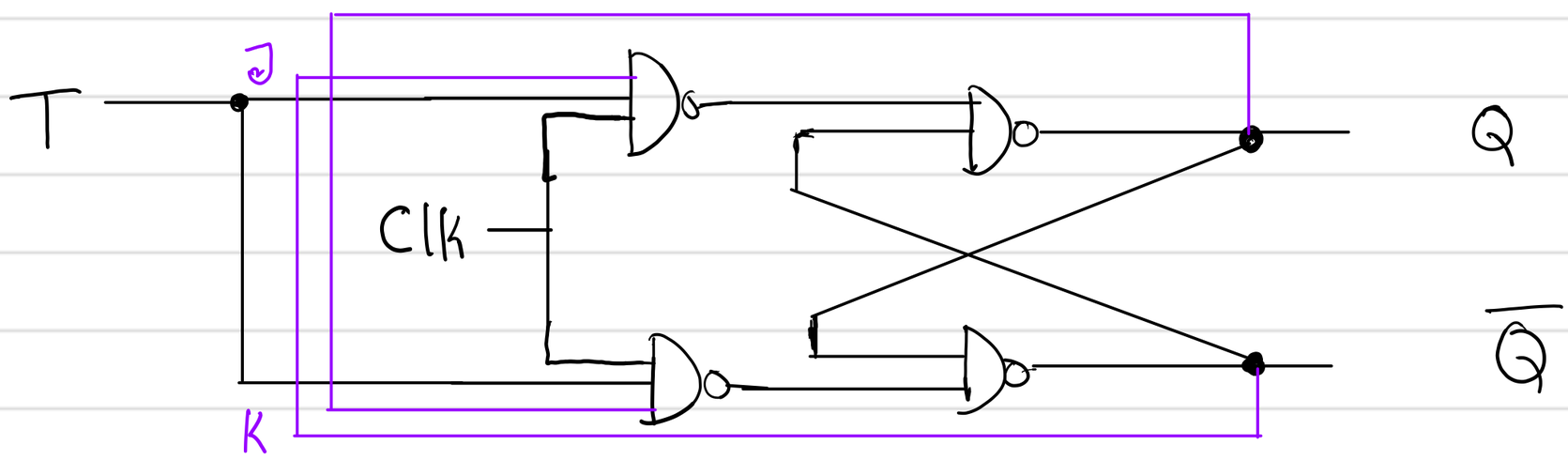
Block Diagram:



T flipflop:

* If we short J & K in JK Flipflop, we get T flipflop

$$J = T$$
$$K = T$$



Truthtable:

T	Q $\overline{Q}$
0	No change
1	Toggle

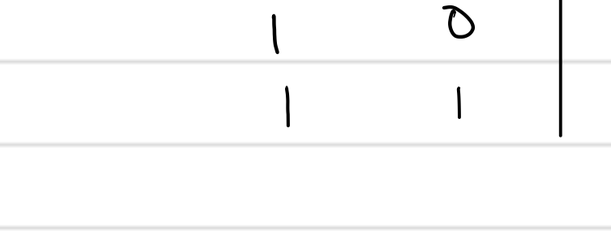
Characteristic Table:

Q(t)	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table:

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Block Diagram:



using JK,