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Electrical and Electronic Engineering

**Verification of Variable Frequency Drive
Circuit Model**

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partial fulfilment of the requirements for the degree of

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Abstract

Variable Frequency Drives (VFDs) are electrical devices placed upstream of an AC motor to control the speed and torque of a motor. The inclusion of a VFD, which is a non-linear load, can produce spurious earth leakage currents which falsely trip earth leakage protection devices. Consequently, there has been an emphasis placed on modelling these earth leakage currents in circuits which contain an AC drive. Therefore, the primary aim of this thesis was to prove that the current circuit model, developed by John Pennisi (2012) [1], could produce circuit characteristics with similar trends to that produced in typical industry VFD environments. To do this, a practical hardware simulation of a typical industry VFD – motor environment was constructed to test the accuracy of the circuit model and make recommendations on which conditions could lead to problematic earth leakage levels. The investigation involved the recording of voltage and current waveforms at important circuit nodes such as at the input harmonic filter node, input VFD node, output VFD node and earth conductor node. Generally, the model and measured responses showed similar trends, though it was found that the circuit model did not maintain an accurate motor load model (excluding the effect of motor inductance) and negated to include the stray reactances prevalent in actual industry environments. However, this investigation was successful as it proved that the circuit model can still satisfactorily represent the trends apparent in actual environmental conditions and could be used as a tool to approximate conditions that may spuriously trip earth leakage devices. Furthermore, it was found that a high carrier frequency and low duty frequency can exacerbate spurious earth leakage current issues. This thesis was supported by an industry partner Orana Engineering.

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CHAPTER ONE

1 INTRODUCTION

1.1 Statement of Intent

The purpose of this thesis was to prove that the current circuit model, developed by John Pennisi (2012) [1], could produce circuit characteristics with similar trends to that produced in typical industry Variable Frequency Drive (VFD) environments.

1.2 Need for Thesis

Variable Frequency Drives (VFDs) are electrical devices placed upstream of an AC motor to control the speed and torque of that motor. They are becoming an extremely common device used in industry, as the adjusting of motor torque and speed to load requirements can provide much higher levels of energy efficiency, as well as many other important advantages too. Due to the introduction of relatively modern technologies such as Insulated Gate Bipolar Transistors (IGBTs), the manufacturers of these VFDs are now able to produce significantly faster switching drives. However, the introduction of these faster drives to the industry has resulted in issues with the generation of spurious earth leakage currents. Important earth leakage protection devices (ELPDs), which monitor the earth conductor for any circuit fault behaviour, can be sensitive to such earth leakage currents. These ELPDs will isolate the downstream circuit by opening a circuit breaker when a certain level of current is registered through the earth conductor for certain amount of time.

The coal mining industry maintains strict regulations in the Queensland Coal Mining Health and Safety Act about the requirement for earth leakage protection of no more than 30 mA sensitivity for all electrical equipment, so as to avoid fatal electrocution to mining personnel. Consequently, the coal mining industry, as well as various other industries, has an issue with VFDs producing some earth leakage currents above 30 mA and therefore isolating pieces of critical equipment. This repetitive false tripping behaviour of protection devices can result in production downtimes which can cost hundreds of thousands of dollars. Also, it can breed cultures of inappropriately using ELPDs to reduce the number of spurious trips. Inappropriately using such critical safety devices has the potential to cost significant outlays of money to replace damaged equipment from an earth fault and can pose serious safety risks to personnel.

Consequently, there has been an emphasis placed on modelling circuit characteristics, such as earth leakage currents, in circuits which contain a VFD – motor environment. By utilising the tool of modelling, clients can determine whether certain design conditions will cause spurious tripping before performing the install. This allows the client to reassess the option of changing these conditions to achieve a smaller earth leakage level, or reconsider using a

VFD for that situation before significant costs are incurred. Furthermore, the tool of modelling can be used to help troubleshoot possible causes of the high earth currents in existing industry situations. Without modelling, the client would need to go through the time consuming process of going out to the actual VFD circuit and testing all circuit characteristics, whilst maintaining little knowledge as to where the earth current problem originates from.

VFD circuit models will likely only be used for the purposes of investigative troubleshooting or providing clients with estimated conditions that could cause earth leakage current issues. Therefore, the circuit model does not require the production of node voltages and currents that exactly replicate the existing industry VFD circuit. This extremely high level of accuracy would be impossible to achieve as all VFDs on the market are different and it is extremely difficult to include the effects of all practical stray circuit impedances and noise. Therefore, a generic VFD – motor circuit model is required which can provide similar circuit characteristic trends to typical industry VFD circuits.

The current circuit model has not been verified with results from typical existing industry VFD environments. Consequently, there is a need to verify that this circuit model can provide similar circuit characteristic trends to typical VFD circuits whilst exposed to different industry conditions.

1.3 Project Goals

The primary goal of this thesis was to prove that the current circuit model could produce circuit characteristics with similar trends to that produced in typical industry VFD environments. To achieve this goal, multiple project objectives were formed. The first objective involved constructing a practical hardware simulation of a standard industry VFD – motor environment. The next objective was to expose the practical hardware simulation to various typical industry conditions whilst testing the circuit characteristics. These same industry conditions would then be simulated in the circuit model and the results between the two different models compared to test the accuracy of the circuit model. The penultimate objective was then to make recommendations on how to improve the circuit model and conclude if this model could appropriately forecast circuit characteristic trends for different install situations. The last objective was to determine, based on the results from the circuit model and hardware simulation, which industry conditions could lead to problematic earth leakage levels.

CHAPTER TWO

2 LITERATURE REVIEW

This review covers the background theory relating to VFDs, earth leakage protection and any associated equipment. It will detail what VFDs are and why they are used in the industry. Furthermore, this review will give a brief summary of how AC motors work and relate this theory back to the functioning of a VFD. Also, the theory behind the construction and operation of a VFD will be investigated and any effects that they produce will be outlined. Moreover, this section will explain what an earth leakage protection relay is used for and outline the theory behind its functioning.

2.1 Basic Summary of VFD Industry Usage

A VFD controls the speed and torque of an AC motor. This piece of equipment can often be referred to as a Variable Speed Drive (VSD), Adjustable Speed Drive (ASD) or Variable Voltage Variable Frequency Drive (VFD). There are many advantages to utilising a VFD in industry. These consist of:

- Smoother operation as speed of the motor can be adjusted according to process requirements, instead of cycling the fixed speed motor on/off (which creates electromagnetic and thermal stresses) [3]
- Allow for slow operation during motor start-up to limit large motor inrush current [3]
- Acceleration, torque and tension control which is extremely difficult for a fixed speed motor [3]
- ASDs are more energy efficient than fixed-speed motors as the torque and speed can be adjusted to load requirements, as opposed to always running the motor at a fixed speed [3].

2.2 Brief Summary of AC Motors

AC drives are typically used in tandem with either synchronous or induction motors [4]. Induction motors comprise of a stator and rotor. In a three-phase induction motor, each phase of the power supply is connected to opposing wire coils (electromagnets) on the stator. These coils produce a magnetic field with a polarity that rotates in one direction at a constant speed as shown in Figure 1[5].

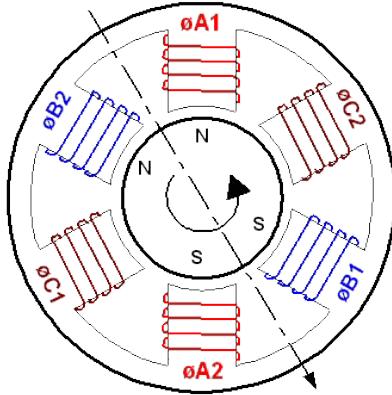


Figure 1 - Stator Opposing Electromagnet Pairs [6]

The rotor maintains wire coils wound onto an armature (mounted on the axle). The rotating magnetic field produced by the stator will produce eddy currents in the rotor. These eddy currents will interact with the magnetic field and effectively apply a torque on the rotor [5]. Induction motors are typically used for small variable loads (such as pumps and fans) due to being physically and electrically rugged. This is because the exact matching and speed control are less important for induction motors in comparison to synchronous motors [4].

Synchronous motors have an external power supply connected to the rotor (via a commutator or various other methods) which creates its own magnetic field. This magnetic field needs to be synchronised with the rotating magnetic field created by the stator to produce a torque on the axle. A synchronous motor will run at synchronise speed and produce synchronise torque in accordance with (1) [7].

$$n_s(\text{RPM}) = \frac{120f}{P} \quad (1)$$

where f = supply frequency and P = number of poles

Synchronous motors are usually used for large steady loads because they have to be matched more carefully [4]. Whereas, in an AC induction motor the rotor must rotate more slowly than the synchronous speed of the stator field to ensure that the stator's magnetic field will still rotate in relation to the rotor (rotating magnetic field interaction causes torque). This difference in speed between rotor and stator is called slip and can be calculated in (2) [8].

$$\text{Slip \%} = \frac{n_s - n_r}{n_s} \quad (2)$$

where n_s = synchronous speed and n_r = operating speed

It can be seen from Equation (2) that an easy way to vary the synchronous speed of a motor is to alter the input frequency. This is the basic principle of how a VFD works.

2.3 Explanation of VFD Functioning

A VFD controls the torque and speed of a motor by producing a waveform at an appropriate frequency. However, the voltage of the output waveform must also be varied to ensure that the applied voltage to applied frequency ratio (V/Hz) is kept close to constant [3]. This is important because keeping a constant V/Hz ratio will maintain a constant magnetic flux in the motor and therefore maximise torque (as magnetic flux can significantly decrease at lower frequencies) [9].

There are several internal VFD modules which contribute to the process of varying voltage and frequency. Firstly, the line side supply three phases are connected to the input rectifier and filter module which converts the AC three phases into a DC voltage. The command unit module then receives user inputs (VFD settings) and performs the necessary operations on a microprocessor. The microprocessor will communicate with and instruct the output module. This module converts the DC voltage to an appropriate frequency output waveform using an inverter circuit [10].

2.3.1 Input Rectifier and Filter Module

This module typically consists of a three phase diode bridge rectifier circuit and a capacitor filter as shown in Figure 2. The bridge rectifier circuit converts the AC waveform into a DC voltage with a ripple and the capacitor smooths the ripple [10]. A typical three phase bridge rectifier circuit is shown in Figure 2.

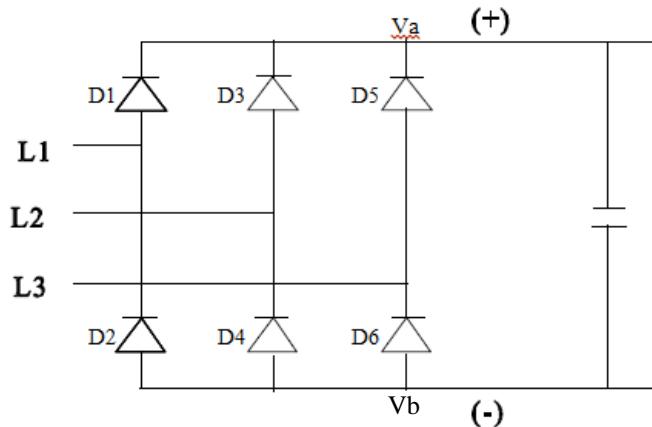


Figure 2 - Typical Rectifier and Filter Circuit for PWM Drive [10]

When examining Figure 2, it can be noted that node Va must be 0.7V greater than each phase input node (L1, L2, L3) for the diode to conduct. Therefore, the diodes will follow a sequence of conducting the phase with the highest voltage, as the other diodes won't conduct because Va will be less than their phase node voltage [11]. This results in node Va outputting the envelope of the three phase waveform as shown in Figure 3.

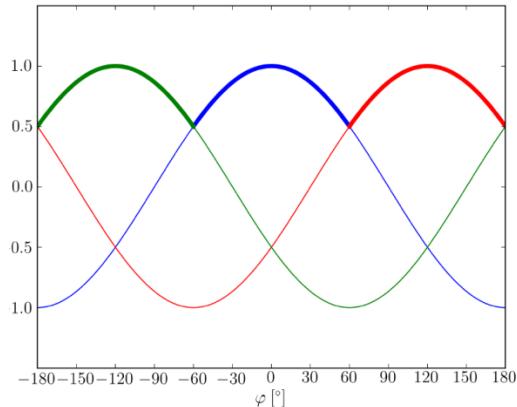


Figure 3 - Positive Half-Wave Rectifier Waveform (Bold waveform = output from diodes D1, D3, D5) [11]

The diodes D2, D4 and D6 will also conduct in a similar sequence, except only conducting for the minimum crest of the input waveform as shown in Figure 4.

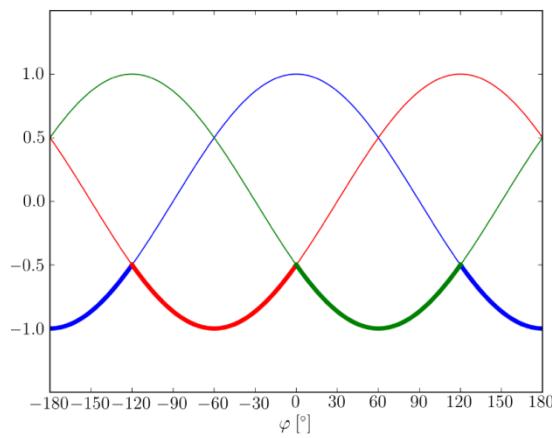


Figure 4 - Negative Half-Wave Rectifier Waveform (Bold waveform = output from diodes D2, D4, D6) [11]

When examining Figure 2, it can be seen that the output waveform from the rectifier circuit will be $V_a - V_b$. Therefore, by subtracting the waveform in Figure 3 from the waveform in Figure 4, it can be seen that the output waveform from the rectifier circuit will resemble Figure 5.

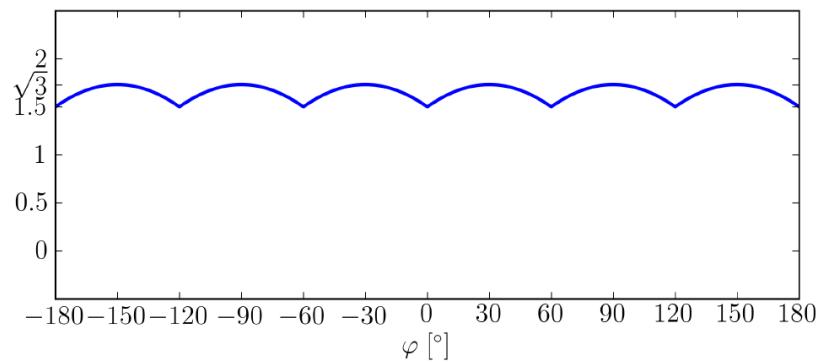


Figure 5 - Rectifier Circuit Output Waveform [11]

As can be seen in Figure 3 and Figure 4, each phase will only draw current during a maximum and minimum peak, which is shown in Figure 6. This pulsating of current creates

harmonics in the supply side and can cause major distribution problems as discussed in Section 2.4 of this document.

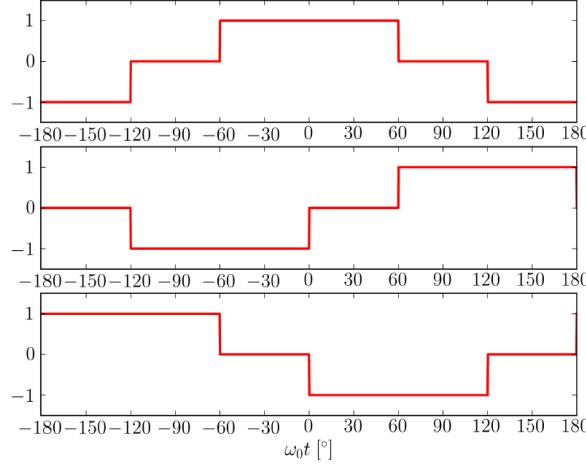


Figure 6 - Phase Current Amplitudes Generated from Full Wave Rectifier Circuit [11]

After the rectifier circuit, the waveform in Figure 5 is then exposed to the capacitor filter. Here, the capacitor charges rapidly during the positive rate of change of the input waveform to close to the peak value. This fast charging time is due to the RC charge time of the circuit being relatively short because of the low conducting diode resistance. The capacitor then slowly discharges during the negative rate of change of the input waveform [12]. This slow discharge causes a smoothing effect of the waveform as shown in Figure 7.

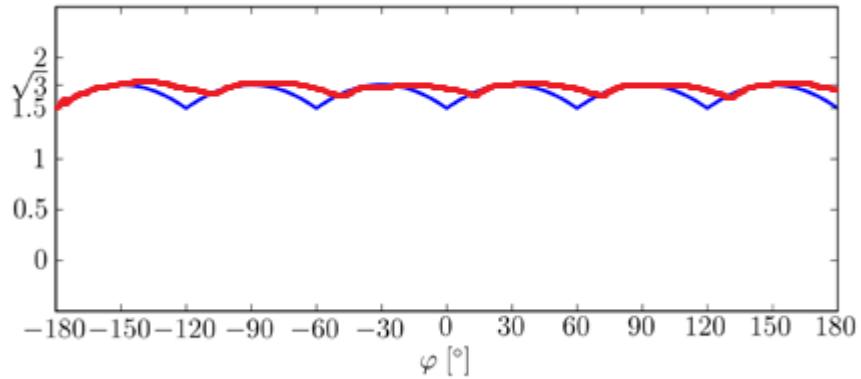


Figure 7 - Output from Capacitor Filter [11]

In reality, the DC filter will have more than just one capacitor which is used to smooth the DC ripple. Two simple types of DC filter are: a capacitive input filter and an inductive input filter. The capacitive input filter maintains a capacitor bank with resistors (which are used to lessen the effect of excess heating from overcurrent on capacitors) as shown in Figure 8. The inductive input filter places an inductor in front of a capacitive input filter, as shown in Figure 8, to stop large changes in current, which cause harmonics and excess heating of rectifier and capacitors [9]. This inductor is commonly referred to as a DC Bus Choke and is further explained in Section 2.5 of this document.

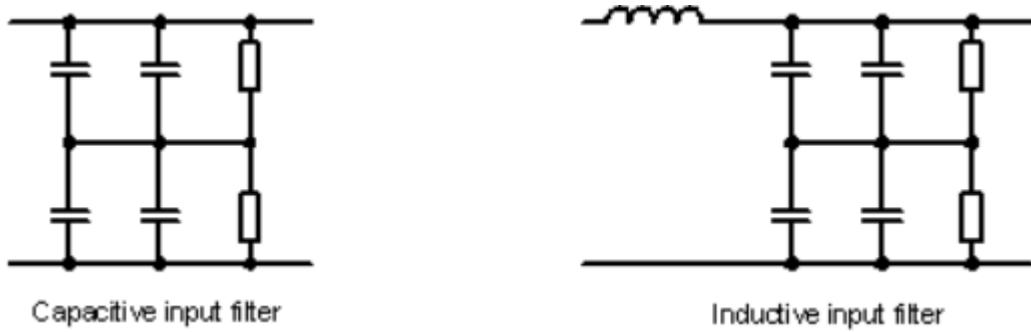


Figure 8 - Two Different DC Bus Input Filters [9]

2.3.2 Output Module Inverter

There are various methods used to generate the output waveform. However, the most common method for motors ranging from 1/2 hp to 500 hp is Pulse Width Modulation (PWM). This is because these drive controllers are reliable, cost-effective and reflect the least amount of harmonics, in comparison to other controllers, back into the power source [13]. For this reason, this investigation will focus on VFDs with PWM drive controllers.

PWM operates by varying the widths of a series of short pulses in accordance with the voltage amplitude of the AC waveform to be modelled as shown in Figure 9. The average power of these pulses is very similar to the desired AC waveform. The frequency of the waveform is determined by the number of positive to negative transitions per second [13].

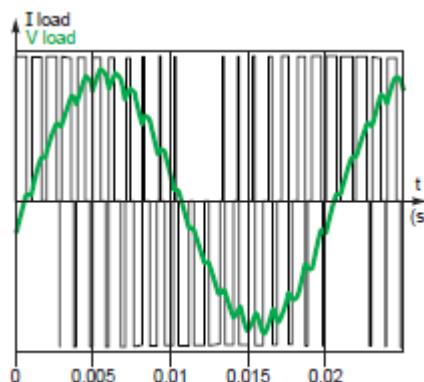


Figure 9 - Example of Pulse Width Modulation [2]

To achieve the high rate of switching required for PWM, insulated gate bipolar transistors (IGBTs) are often used [2]. The control base input to these IGBTs (which controls the IGBT on/off state) is supplied by the command unit module. This unit will relay instructions from the user to the IGBTs [2].

To generate 3-phase pulse width modulation, the inverter circuit in Figure 10 is often used.

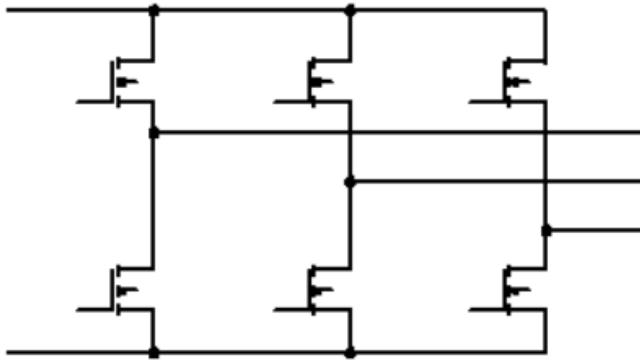


Figure 10 - Typical Inverter Circuit in VSD [9]

A driver circuit is provided for each switching element. This circuit is isolated from the control electronics and provides a sufficient voltage/current to control the switches. Furthermore, an interlock delay between the switch turning ‘off’ and the other turning ‘on’ must be used to prevent the upper and lower switch of one phase being turned on at the same time [9].

The switching rate of these IGBTs is controlled by the VFD carrier frequency parameter [14]. A higher carrier frequency creates a smoother output as the resolution size of the quasi-sinusoidal waveform decreases [15]. Also, the pulses generated by the PWM cause vibrations in the motor that sound like a high-pitched whine [14]. A slow switching rate in the order of 1 – 3 kHz will sound very loud as this is the most audible tone range for humans; faster switching rates will appear not as loud [15]. According to a study performed by the IEEE in 1994, increasing the switching frequency has the following effects:

- AC drive losses increase [15]
- Large acoustic noise drop up to switching frequencies of 6 kHz [15]
- Harmonic losses decrease up to switching frequencies of 10 kHz then begin to increase again [15]
- Does not affect motor losses [15]

Furthermore, voltage spikes are generated by faster switching which can damage motor insulation. Therefore, designers will limit the maximum rate of change of voltage with respect to time (dv/dt) to minimise motor insulation stress. Moreover, designers must attempt to minimise the switching time of each individual IGBT to allow for higher carrier frequencies without derating the motor HP [15]. The IEEE study recommended 6 kHz as the optimum carrier frequency when considering acoustic noise and minimising losses [15].

2.4 Harmonics

A harmonic is a signal at frequencies that are multiples of the base frequency [16]. Based on knowledge of the Fourier series, a continuous periodic signal can be made up of a summation of sine waves (harmonics). Harmonics that occur at odd-numbered multiples of the base frequency (third, fifth, etc.) are known as ‘odd order harmonics’ and are caused by symmetrical distortion of the waveform. ‘Even order harmonics,’ which occur at even numbered base frequencies, are caused by asymmetric distortion; where the positive and negative halves of the waveform are unequally distorted. A full wave rectifier equally distorts negative and positive halves of the waveform. Therefore, VFDs will produce odd order harmonics only [16].

In three phase systems, even order harmonics cancel out and odd order harmonics are additive in the ground and neutral paths. Harmonics that are multiples of three are called triplens and cause major problems in electrical distribution systems (particularly the third harmonic). These triplens currents return to the transformer source through the neutral and cause heat dissipation across cables and loads [17].

In a diode bridge rectifier circuit, the output harmonic multiple numbers can be calculated by (3). Therefore, a standard 6-pulse rectifier circuit characteristic harmonics will be 5th and 7th harmonics, 11th and 13th and so forth [18].

$$h = (n \times p) \pm 1 \quad (3)$$

where n = integers and p = number of pulses or rectifiers [18]

2.5 Harmonic Filters

To reduce harmonics there are three main filters used in tandem with VFDs. One such filter is the line reactor as shown in Figure 11, which is electronically placed after the VFD. The line reactor comprises of a coil wound around a magnetic core, creating an inductor. The voltage across an inductor is equal to $L \cdot (di/dt)$. Therefore, it can be seen that the inductor opposes instantaneous current changes as the existing magnetic field opposes the current flow [19]. This has the effect of smoothing out the current impulses and therefore reduces harmonics.

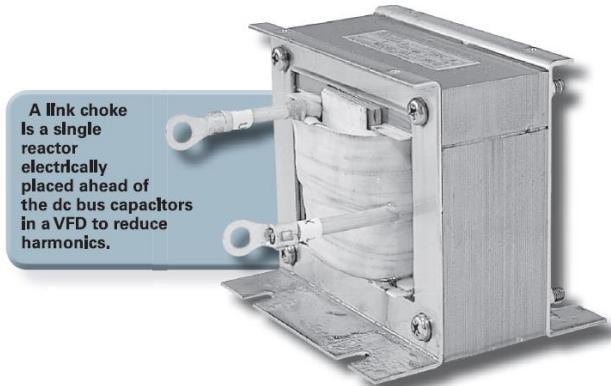


Figure 11 - Example of a Line Reactor [19]

Another typical filter used is the link choke, which is a single link reactor placed ahead of the dc bus capacitors. However, this filter does not provide protection against voltage transients, like the line reactor, because the main source of voltage transients is in the inverter which is electronically positioned after the link choke [19].

Another typical filter is the swing choke. The swing choke reduces current harmonics and also reduces DC bus ripple. When VFDs are partially loaded they produce more current harmonics (less load means more current and therefore more harmonics). The swing choke increases its inductance when current passing through it decreases [19].

2.6 Different VFD Rectifier Circuits to Minimise Harmonics

The generic three-phase rectifier circuit contains six diodes. Since six transitions occur during each period of the input source signal, these rectifier circuits are called six-pulse rectifiers. More complex and expensive VSDs often use 12-pulse rectifier circuits which create a smoother DC waveform in the DC link and reduce the harmonics in the system by eliminating the 5th and 7th order harmonics [20]. The 12-pulse rectifier circuit is constructed from two 6-pulse rectifiers which are connected to the power source via phase-shift transformers as shown in Figure 12. These phase-shift transformers significantly reduce the harmonic reflection back to the power source. The windings of the transformers are offset to cancel the largest harmonics from the VFD and can be tuned to reduce harmonic distortion to less than 10% of the VFD input terminals [21].

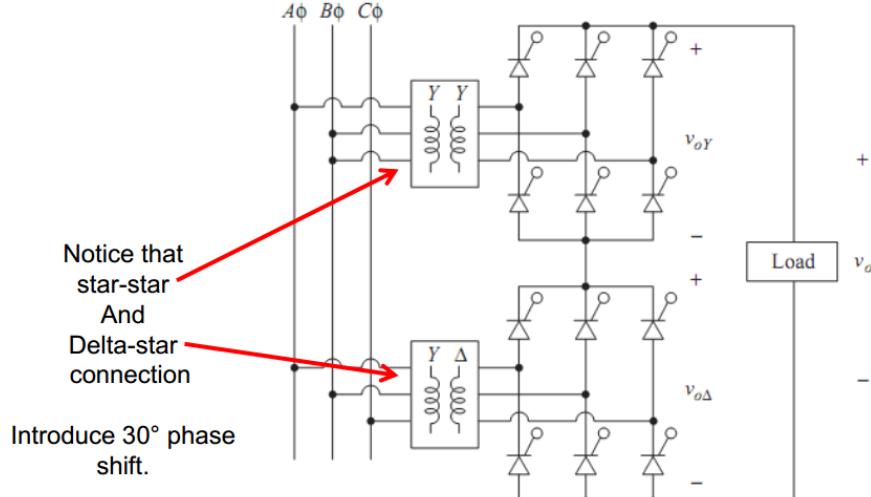


Figure 12 - A Typical 12-Pulse Three Phase Rectifier Circuit [20]

As shown in Figure 12, the different phase transformer connections (wye-wye and wye-delta) introduce a 30° phase shift in between the waveforms produced by the 6-pulse rectifier circuits. It can then be seen from Figure 13 that the superposition of these two waveforms produces a DC waveform with a smaller ripple factor than that experienced with a 6-pulse rectifier circuit.

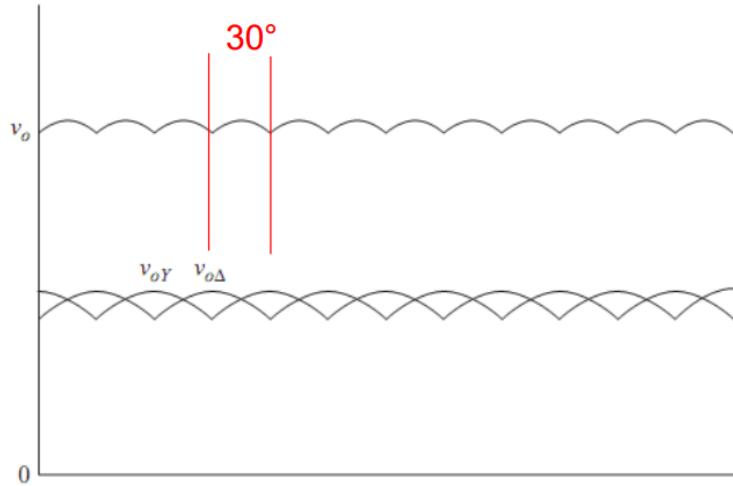


Figure 13 - Output Waveform from 12-Pulse Rectifier Circuit [20]

The disadvantage of the 12-pulse rectifier VFD is that it will cost more (sometimes up to 50% more) and will be physically larger than the 6-pulse VFD [21]. Due to the high cost involved with producing high-power phase-shift transformers, 18-pulse rectifier circuits are only considered when designing VFDs in high harmonic resonance situations [20].

2.7 VFD Leakage Current

Leakage currents can spuriously occur due to parasitic capacitances found in the circuit which are exacerbated by the presence of a VFD. The characteristics of these leakages currents depend on the PWM modulation frequency (carrier frequency), incommutator line

impedance, type of earthing system used, type and length of the motor cable and the motor rating [2].

The carrier frequency affects the leakage current because the output PWM creates a high rate of change of voltage. Since current through a capacitor is equal to $C \cdot (dv/dt)$, these high rates of the change in voltage can cause large enough currents (despite low capacitance) to spuriously trip current sensing devices [19]. The length of the motor cable also affects leakage current as the length of the cable influences the cable capacitance value (a longer cable maintains a higher capacitance). Furthermore, the type of cable will influence leakage current as some cables are shielded to reduce capacitive coupling to earth [2].

Typically these leakages currents are influenced by:

- capacitance of IGBT components (between conductor and earthed enclosure) [2]
- capacitance between motor windings and earth [2]
- capacitance between line supply and neutral (short circuited if neutral connected to earth) [2]
- capacitance between output conductors and earth (related to cable length) [2]
- interference suppression capacitance at drive input [2]

These capacitances have been illustrated in Figure 14.

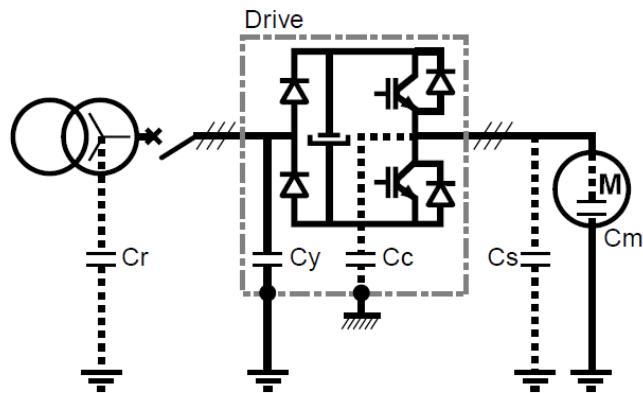


Figure 14 - Typical Capacitances in a VFD Circuit [2]

2.8 Explanation of ELPRs

Earth leakage protection relays are designed to give earth leakage protection and monitoring for electrical equipment (such as motors, transformers, etc.). To detect the earth leakage current, the phase conductors (including neutral) are passed through a core balance current transformer (CBCT) [22].

It is important when passing the conductors through the CBCT that each conductor be running in the same direction and be perpendicular to the CBCT [22].

CHAPTER THREE

3 METHODOLOGY

This section details the method that was used for this investigation to gain data that was necessary for refining the existing VFD circuit model. To summarise the method, a flow chart was created containing brief explanations of each important project milestone. This flowchart can be viewed in Section 3.9 of this document.

3.1 Initial Analysis of Project Goals

It was decided that the voltages and currents of all nodes in a practical hardware VFD circuit needed to be acquired to validate that these appropriate circuit characteristic trends existed in the circuit model. Moreover, to fully test the model, different practical industry conditions needed to be generated and tested. There were many conditions that could influence VFD circuit node voltages, which could have been chosen. However, due to the time restrictions involved in this investigation, it was decided to only focus on four simple conditions (two conditions for each group member). These conditions were chosen based on information obtained in the literature review, Section 0 of this document.

The literature review suggested that the carrier frequency of the VFD, the cable capacitance and motor load impacted on circuit characteristics. Therefore, these three conditions would be tested. Also, it was decided to test how the model performed when an actual fault occurred. These four factors are only some of the different practical conditions that affect VFD circuit characteristics and consequently, subsequent investigations should investigate other conditions such as earthing types, other circuit capacitances and the usage of different types of earth leakage protection devices.

It was deemed prudent to next investigate the equipment that had been provided by Orana Engineering to construct the practical circuit, before commencing any further detailed analysis of the methodology.

3.2 Overview of Provided Equipment

A 6 kW squirrel cage rotor motor (which is shown in Figure 15) was provided by Orana Engineering to replicate a VFD circuit. The provided motor configuration also maintained a DC generator which was coupled to the motor shaft to act as a load. This allowed for different loading conditions to be tested. Furthermore, CSE Uniserve donated a VFD and harmonic filter to be used in tandem with the motor.



Figure 15 - 6 kW Squirrel Cage Rotor Motor which was used

The provided motor configuration also included fault simulation circuitry, which contained a variable resistor circuit connected between the motor input active phase and protective earth (PE) to simulate a ground fault. Specifically, this circuit maintained a rheostat, adjustable resistance, (which is shown in Figure 16) and allowed for the earth leakage current to be varied in the range of 0 mA – 300 mA over all VFD output states. However, it was highlighted that the VFD would vary voltage when frequency was changed. This meant that the earth leakage current needed recalibrating after any speed changes.

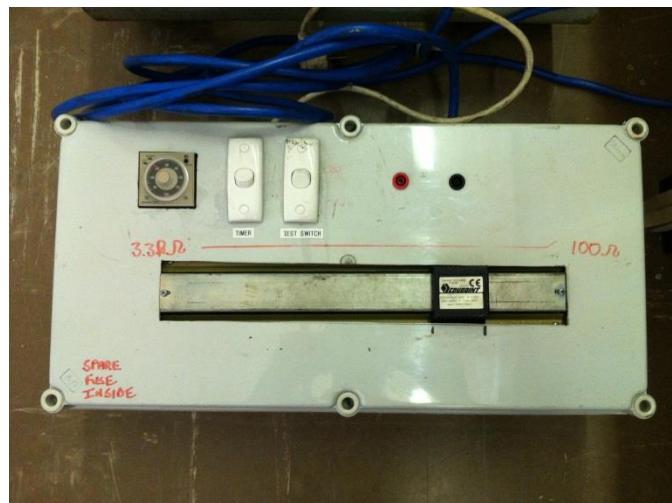


Figure 16 - Rheostat which was provided by Orana Engineering

Orana Engineering also provided 100m cable reels containing two different types of cable. One cable was shielded against capacitive coupling, which is specifically designed for VFD environments, and the other cable was a generic Steel-Wire Armoured (SWA) cable. However after consulting with electricians, it was decided that the SWA cable was not appropriate for the test circuit. This was due to the rigidity and inappropriate core size of this

cable. Therefore, it was decided that only the VFD rated cable would be used for this investigation.

Furthermore, a pico-scope (PC Oscilloscope), which can communicate with a laptop or PC via a USB connection, was provided by Orana Engineering. This allowed for all voltage waveforms to be recorded. Due to the high cost of the test equipment, a methodical approach was devised to ensure that the risk of personal hazards and equipment damage was minimised. Once this equipment was examined, the investigation moved onto analysing each of the project tasks.

3.3 Initial Analysis of Project Tasks

3.3.1 Selection of Testing Room

Careful consideration was required when selecting the appropriate room to conduct testing in. Firstly, the room required a 415V three-phase supply to power the motor. Furthermore, arrangements needed to be made to isolate the earth leakage terminal from the upstream Residual Current Devices (RCDs) as earth leakage current would be intentionally produced during testing. This was because the upstream RCDs could have tripped the associated busbar and isolated other important pieces of university equipment.

3.3.2 Testing Motor's Operational Functionality

Since the motor had been previously located in a storage area exposed to the elements, the motor needed to have its insulation and cable integrity tested by performing a mega-test (test the insulation by measuring resistance from active to earth). Moreover, the motor needed to be powered up and tested to ensure its functionality before continuing with setting up subsequent parts of the test environment. To do this short test, Orana Engineering provided a 415V 3-phase plug connected to a rotary switch.

Also, a contingency plan was developed to manage any functional issues with the motor. The plan consisted of scheduling the motor testing dates at least a month before the actual test date. This was to ensure that there was adequate time to either contract an electrician to help repair the motor or source another motor altogether.

3.3.3 Testing and Recording Circuit Currents

A Fluke i30 AC/DC Current Clamp was provided by Orana Engineering to test the current at certain points in the circuit. To ensure that the current clamp was adequately rated, the specifications sheet for this device was accessed. According to FLUKE: The Most Trusted Tools in the World [23], the current clamp could measure currents in the range of 30 mA to 20 A (AC RMS). It was found that the three-phase supply delivered a maximum 20 A

current rating. Therefore, this current clamp device was deemed suitable for usage with this investigation. According to FLUKE: The Most Trusted Tools in the World [23], the current clamp uses a toroidal CT to measure current and produces a proportional DC voltage at the output plug. Therefore, the output plug was connected to the Pico-scope to effectively record the circuit current.

3.3.4 Testing and Recording Circuit Voltages

The large transient voltages that were experienced in the PWM output from the VFD would have damaged the pico-scope if it were directly connected to the circuit. Therefore, it was initially planned to use a voltage divider circuit to appropriately limit the voltage as this was thought to be the easiest method of limiting voltage. The Pico-scope could then be easily connected across this smaller fixed resistance.

3.3.5 Simulating Load Conditions

According to Dr Graham Woods (Electrical Engineer at Orana Engineering), the DC generator maintained a self-excitation armature winding configuration to produce field current through the electromagnets. However, Dr Graham Woods detailed that this field circuitry was faulty and needed to be repaired. After consultation with contractor electricians, it was established that repairing the DC generator would require an electro-fitter, which would be both costly and time-consuming. Therefore, the load simulation test for this investigation was abandoned.

3.4 Analysis of Circuit Experiment Procedures

The testing procedure for each test was extremely flexible and was tailored as each test was performed to avoid gaps in important data or the unnecessary repetition of tests.

3.4.1 Test #1: Testing the effects of different VFD settings

To refine the existing model, the original plan was to test the voltages and currents at each node of the VFD circuit. These nodes included the input VFD node, output VFD node, input motor node and the earth leakage conductor node. When analysing these nodes, it was decided easier to refine particular elements of the existing model independently. Therefore initially, the VFD harmonic filter was not used during testing. The plan was then to perform the same tests again with the VFD harmonic filter placed upstream of the VFD. A comparison of the data from this test and the previous test would then show the effect that the harmonic filter had on all circuit voltages and currents. Moreover, the shorter cable length was used for these tests so as to minimise the effects of cable capacitance, as this was to be tested in subsequent tests.

A range of duty frequencies (VFD speeds) and carrier frequencies were tested to help refine the existing model. It was decided that varying the VFD speeds from 10 Hz, 30 Hz to 50 Hz would sufficiently test the impact of adjusting speed on the circuit. However, the performing of other tests with further speeds would depend on the results from these two tests. Furthermore, it was decided to vary the carrier frequency from 2 kHz, 6 kHz to 15 kHz. Therefore, a total of 9 tests for each circuit nodes were initially planned.

3.4.2 Test #2: Testing the effects of faults to ground

To test that the model would perform accurately under fault conditions, the motor was intentionally faulted to ground with fault simulation circuitry provided by Orana Engineering. Using a rheostat, the resistance of the fault to ground was varied from $100\ \Omega$ to $3.3\ k\Omega$, to gain a variety of earth leakage currents. A specific duty frequency and carrier frequency of 10 Hz and 6 kHz was chosen to use during this test was chosen based on the results from Test #1.

3.4.3 Test #3: Testing the effects of cable capacitance

This test produced data to refine the cable capacitance element of the existing model. During this test, different lengths of cable were used to join the VFD and the motor. A short cable with a length of 10 m and a long cable length of 50 m were used during this test. This provided adequate data about how cable length affects cable capacitance with the minimum number of tests.

3.5 Setting up of the Test Environment

A meeting was scheduled to discuss the setting up of the test environment with university technicians, university estate electricians and university contractor electricians. During this meeting, the room selection and required safety features for the environment were further considered.

3.5.1 Selection of Testing Room

It was decided that there were only two rooms available that were both on the ground floor (too hard to transport heavy motor upstairs) and were not publicly accessible (for other students' safety). These two rooms were the Green Room and High Voltage (HV) Lab located in DD014-007. Out of these two rooms, the Green Room was the only room to already have a 3-phase power supply installed. However, the HV Lab maintained a high voltage cage as can be seen in Figure 17.



Figure 17 - High Voltage Lab with Cage in foreground

This cage provided:

- an extra earth grid to use when earthing the motor
- an extra safety boundary to use during testing and further guard against unwanted access to student personnel
- potential for a safety interlock on the gate (cannot access power supply when cage gate is open)

Therefore, it was decided to use the HV Lab and get a 3-phase supply installed. This supply also had the earth terminal isolated from the main switchboard to stop accidental tripping of upstream RCDs. Fortunately the cost of this job was costed to the university infrastructure account, as a HV Lab should already have a 3-phase supply.

3.5.2 Test Environment Safety Features

During the meeting, it was also decided that the VFD and harmonic filter required an enclosure to guard the otherwise exposed live circuit connections. However, an enclosure of this size would be expensive. Therefore, provisions were made to source a second-hand adequate enclosure from university estates to minimise project cost.

It was also decided that an emergency stop button was required to be positioned next to the bench in the HV Lab. This was so that the safety observer, who would be sitting next to the bench, could immediately isolate power if an emergency occurred.

To minimise project cost, it was decided to make a single test set-up which required no further electrical work to be conducted in between tests. Although, this would make the initial set-up more expensive, it was deemed cheaper than increasing electrical contractor labour time. Furthermore, this would allow the set-up to be used for future university labs and practicals. It was thought that this additional attribute would prove useful when

requesting project funding from the university. It was also informed that Australian Standards required at least one qualified electrical engineer to be present during testing, due to the safety implications of the magnitude of voltage present in the three phases. However, this would not appreciate any cost, as a university lecturer with a qualified electrical engineering certificate could be asked to supervise.

A method of accessing each important circuit node, without performing electrical work, was required to make a single test set-up. Therefore, it was decided that placing banana plugs at each important node of each phase would be used as an easy way to access important nodes. The voltage recorder circuit (Pico-scope and voltage divider circuit) would then be connected to a banana connector. This voltage recorder circuit could then be individually connected to each circuit node of any phase without performing any electrical work. However, the electricians later informed that solder connections which are required for banana plugs were not suitable for voltages over 240 V. Therefore, proper circuit test points were used instead of banana plugs. Moreover, a space was allocated for each node inside the enclosure to fit tong clamps into to record the current of each phase.

To model the cable lengths in the cable capacitance test, two extension cables were created using 3-phase plugs and sockets. To change the cable length in between the VFD and motor, the two leads were interchanged without performing any electrical work. Furthermore, in order to test with and without the harmonic filter and not require any additional electrical work in between tests, it was decided to use a 6-pole bypass switch to isolate the harmonic filter when needed.

After the initial safety meeting, a single-line diagram was drafted outlining the chosen experimental set-up. This drawing was then given to the contractors so that a quote could be formulated and the project costing calculated. (This drawing can be found in Appendix 7.2)

3.5.3 Pico-Scope and Voltage Recorder Circuit Changes

Before commencing any actual testing, it was decided to simulate recording current and voltage. To do this, a function generator was connected to the pico-scope to create mock data. It was initially thought that using a laptop to record the data would be sufficient. However, upon testing the pico-scope which was provided by Orana Engineering, an issue with recording any data to the program on the laptop was established. Since the pico-scope continually disconnected during data transferral and the power was transferred across a USB cable, it was decided that there was a possible issue with current supply from the laptop. Therefore, a desktop PC and self-powered USB hub was trialled to see if this could solve the problem. However, a stable data connection still could not be achieved. Consequently, the university pico-scopes, which are built into PC towers, were used.

This presented a problem with the voltage divider circuit, as the university pico-scopes were only rated to 20 V. Therefore, a larger divider ratio was required which resulted in a greater voltage across the first resistor. As a result of this, larger power rated resistors were required to handle the load in the divider circuit. Furthermore, a larger resistance was required to ensure that minimal current drop would be experienced when the voltage recorder circuit was connected to a circuit node. Moreover, it was considered expensive to purchase a single high power large resistance device which would also generate a significant amount of heat. Consequently, two smaller power resistors, two 10 kΩ 50W resistors, were ordered. However due to a mistake from the manufacturer, only a 10 kΩ and 6.8 kΩ resistor were received.

It was then estimated that transients of 300 V could be achieved at certain parts of the circuit. This resulted in a required divider circuit ratio of approximately 15 (4).

$$\text{Divider Circuit Ratio} = \frac{300 \text{ V}}{20 \text{ V}} = 15 \quad (4)$$

Since the larger resistance equalled 16.8 kΩ (two purchased power resistors), the maximum value of the smaller resistance was calculated to be approximately 1.12k (5).

$$R_2 = \frac{16.8k}{15} = 1.12k \quad (5)$$

Therefore, a 1.2k power resistor was used as this was available in the university tech lab and would therefore incur no extra cost to the project. It was then decided that the power resistors would require a heat sink and jiffy box to be mounted in to enclose live connections. Both of these items were acquired from the university tech lab with no extra project cost.

3.5.4 Construction of Voltage Recorder Circuit

The voltage recorder circuit was constructed with the intent of eliminating all associated safety hazards. The following section details the construction process for this circuit.

Firstly, the power resistors were attached to the jiffy box and heat sink via nuts and bolts. However, due to the fin-like nature of parts of the heat sink, using a nut was sometimes impractical. Therefore, a thread was tapped into the box and heat sink for the bolt to screw into for these sections. Then the resistors and heat sink were attached to the jiffy box lid, as this was easier to access than the container. Banana plugs were then fixed to opposite sides of the jiffy box and were connected across the 1.2 kΩ resistor to act as easy access to plug the picoscope into. As the expected maximum voltage across these plugs was thought to be 20 V, there was no safety concern with having an exposed live voltage. Furthermore, a

longer length of cable was then used when connecting from the resistor to the banana plugs so that the lid could be removed without mechanically damaging these connections.

Both end plugs of an IEC power cable (jug cord) were then removed and the remaining cable used for egress and ingress to the jiffy box. These jug cords were then glanded to the box to ensure an adequate mechanical rating for the circuit. The egress jug cord (the earth cable) was then terminated with a lug, so that it could be easily screwed to the earth grid. The ingress jug cord (active cable) was then terminated with a 6.5mm bullet connector, as this would connect to the node circuit test-points.

Also, when connecting the internal resistor circuit, all live terminations were concealed using heat shrink to safeguard against shorts to the jiffy box. Lastly, a saddle was used to fix the active cable to the sides of the jiffy box and keep it away from the heat which would be generated by the power resistors. This would stop large amounts of heat from melting the active 240 V conductor sheathing. The end product voltage recorder device can be seen in Figure 18.

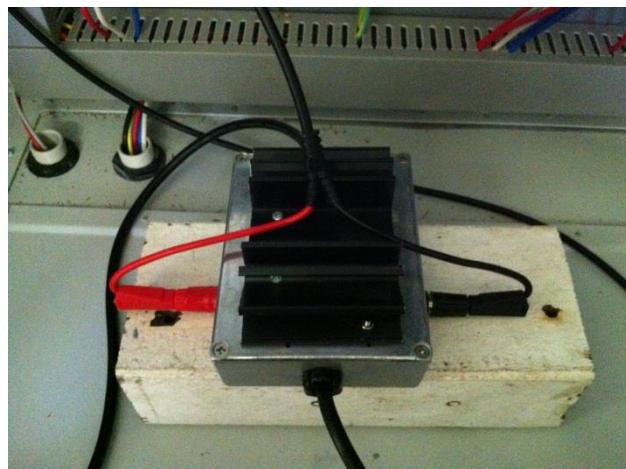


Figure 18 - Voltage Recorder Circuit

3.6 Project Costing

This project required many pieces of equipment that were quite expensive. Fortunately, some of these items were donated to the university or loaned by Orana Engineering and CSE Uniserve. This agreement entailed an obligation to forward all of the findings and reports to these two companies after the project had reached completion. Specifically, Orana Engineering donated a 6 kW Squirrel Cage Motor coupled to a DC Generator and loaned a pico-scope, Fluke i30 Current Clamp, two 100m cable reels, a rheostat, a heating element and related technical papers. Furthermore, Uniserve kindly donated the university a G11VFD and harmonic filter. Also, the university estate donated an enclosure to house the filter and VFD in.

However, there were also electrical labour costs and materials costs for a 6-pole bypass switch, four 3-phase plugs and two 3-phase sockets, an emergency stop button, nine test points and other important safety devices. After gaining a quote from FCOM (university electrical contractor), it was found that these additional labour and materials costs would amount to approximately \$4,000. This figure was substantially higher than was expected, which made securing the funds for the project from the university extremely difficult. As each student was only allocated \$250 from the thesis budget, another university funding source needed to be applied for. It was decided to apply for funds from the university infrastructure budget as the experimental set-up could be used for future university labs and practicals.

3.6.1 Difficulty Securing Project Funds

Initially, the construction of the testing environment and actual testing was to take place in the first week of semester break. However, due to the combination of unexpected high project cost and limited university funds, it took considerably longer than expected to convince the university to fund the project. Also, due to a combination of poor contractor reliability and confusion from the university about the sending of a purchase order, the construction of the testing environment did not occur until the second week of the university term. There had been some contingency time allocated during semester break. However, the five week delay affected the expected completion time of all of the remaining project tasks and resulted in the need for crashing the completion time of subsequent tasks.

3.7 Actual Testing Procedure

3.7.1 Preceding Circuit Tests

The electrical safety act required a qualified engineer to be present when changing any electrical part of the circuit. Therefore, Ahmad Zahedi (Lecturer) was asked to come down to the lab each time a circuit change was required. This requirement did not include changing the extension lead in between the motor and AC drive or reprogramming the settings in the VFD.

Before touching any part of the circuit, a safety observer (any person in the room at the time) was elected. The observer sat at the bench located next to the emergency stop button so that the circuit could be isolated quickly in the event of an emergency. Furthermore, the safety observer also maintained a document detailing the step-by-step methodology instructions, so that no critical steps were accidentally omitted. The observer then instructed the rest of the team on what actions needed to be taken next.

The circuit was also tested to ensure no sparking or arcing occurred before commencing any further investigation. Then, the smaller extension cable was used to connect the drive and motor and the harmonic filter was isolated by opening the 6-pole contact switch. Lastly, the circuit was energised at the wall and the drive was switched into RUN mode. This preceding circuit testing ensured that the circuit functioned properly and confirmed that circuit was safe to work with. A picture of the test environment can be seen in Figure 19.



Figure 19 - Actual Testing Environment (inside enclosure)

3.7.2 Recording Circuit Voltages and Currents

To ensure that circuit changes only occurred when the circuit was isolated, a rigorous step-by-step procedure was followed each time a circuit current or voltage needed to be recorded. This section details the process which was followed.

Initially, the drive was switched to STOP mode and the power was isolated at the wall. Then the voltage recorder circuit was connected to the drive circuit node by plugging into a test point. The pico-scope was then connected across the smaller resistance by plugging into the recorder circuit banana plugs. The power was then reenergised at the wall as no further electrical changes to the drive circuit were required. The pico-scope recording was then initialised to capture any inrush circuit activity. The drive was then placed into RUN mode and then pico-scope recording was continued until it was deemed that the waveform had reached steady state.

The drive was then switched back to STOP mode and the power reisolated at the wall to allow for another small circuit change. The voltage recorder circuit was then removed and the current clamp secured around one of the drive circuit phases, so that the node current could be measured. The drive circuit was then reenergised at the wall again and the pico-scope recording was initialised to capture any inrush current. The drive was then placed into RUN mode and then pico-scope recording was continued until it was deemed that the waveform had reached steady state. Lastly, the circuit was isolated and the current clamp removed, to avoid performing any live work inside the enclosure.

3.7.3 Test #1

The methodology for this test basically included changing the carrier frequency/duty frequency and then recording the node currents/voltages. From the operational RUN mode, the [\wedge / \vee] arrow buttons were used to alter the duty frequency value and the [FUNC/DATA] button was then pressed to save the new value. However, changing the carrier frequency was a more complicated process and required the VFD to be firstly placed in operational STOP mode. Then the [PRG] button was pressed on the VFD display screen to start reprogramming of the VFD. After this, the [Data Setting] option was highlighted from the menu and the [FUNC/DATA] button pressed so that the function of the VFD could be changed. Furthermore, the VFD manual was then consulted to establish the appropriate functional code that changed the carrier frequency. Then this function code, [F26], was entered using the digital keypad and the appropriate carrier frequency was entered. The [FUNC/DATA] button was then pressed to save the change in carrier frequency.

Initially, the carrier frequency of 6 kHz and duty frequency of 50 Hz were chosen for the first test to act as a control throughout all experiments. Then carrier frequencies of 2 kHz and 15 kHz were also chosen to act as minimum and maximum carrier frequencies for Test #1. Also, duty frequencies of 10 Hz and 30 Hz were chosen to act as minimum and maximum duty frequencies. All four nodes, the input harmonic filter, input VFD, output VFD and earth conductor were tested for the control. However, only the output VFD and earth conductor were tested for the other carrier frequencies and duty frequencies. This was done to minimise the number of tests required as the input harmonic filter and input VFD node were independent of the carrier frequency and duty frequency anyway.

Also, the voltage waveforms were being clipped before the peaks using the designed voltage recorder circuit. It was realised that the actual peak voltage of the system was 340 V and the 240 V was the RMS value. Therefore, a quick fix 330 Ω power resistor was placed in parallel with the 1.2 k Ω resistor to limit the voltage appropriately.

3.7.4 Test #2

The methodology for this test included changing the resistance from the fault to ground. To do this test, the carrier frequency of 6 kHz and duty frequency of 50 Hz were chosen as control speeds to avoid further unnecessary testing. The power to the circuit was then isolated before adjusting the rheostat resistance, so as to avoid any undesired transient effects that would occur with a quick change of resistance. Resistances of approximately $3.3\text{ k}\Omega$ and the minimum resistance of $100\ \Omega$ were separately made and tested using a multimeter. The switch to activate the rheostat branch of the circuit was then closed and the power to the circuit reenergised. Lastly, the voltages and currents of the appropriate nodes were measured. However, it was noted that the rheostat fuse blew during the $100\ \Omega$ test, which indicated that more than 100 mA was being drawn. Consequently, the fuse was replaced and a true RMS multimeter was placed across the rheostat to ensure that the new minimum resistance did not draw more than 100 mA. The new minimum resistance that was used for this test was measured at $761\ \Omega$.

3.7.5 Test #3

The methodology for this test included changing the cable length in between the AC drive and motor. Initially, the power to the circuit was isolated and the shorter cable was replaced with the larger 50m extension cable. Then power was reenergised and the voltages and currents of the appropriate nodes were measured.

3.8 Model Revision and Recommendations

The existing model shown in Appendix Figure 55 could have potential to be improved to represent a more accurate model of a realistic VFD. Therefore, the tests performed with the practical environment were reproduced with the circuit model. The practical and simulated data was then compared to determine which parts of the model required improvement. The data was also used to make recommendations about using earth leakage devices with VFDs.

3.8.1 Setting up Testing Environment for Circuit Model

The previous circuit model was created on a program called MicroCap, which was installed at university. However, due to the number of op-amp components, a professional version of MicroCap was required to load this previous model. Therefore, this professional version was acquired from Dr Graham Woods (Orana Engineering) and installed on a laptop.

The first step was to establish how to vary the duty frequency and carrier frequency in the circuit model to replicate the method of Test#1. To do this, the functionality of the inverter circuit in the model needed to be understood. Figure 20 shows that a comparator (op-amp) was used with a sinusoidal duty frequency and triangular carrier frequency signal as inputs.

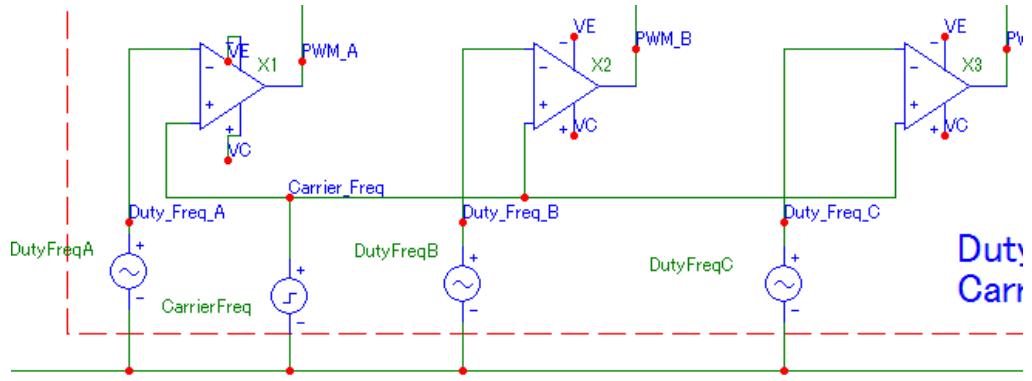


Figure 20 - PWM Generation in MicroCAP Inverter Circuit Model

The comparator generated the PWM signal by saturating high when the triangular wave was higher than the sinusoidal signal and saturating low when the triangular wave was lower than the sinusoid as shown in Figure 21.

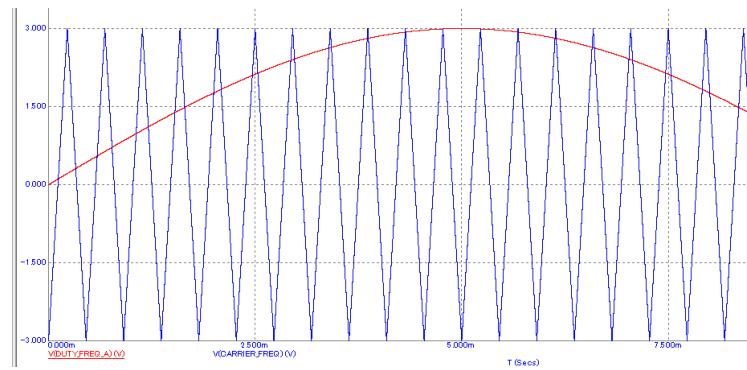


Figure 21 - Comparator Inputs in Inverter Circuit

To change the PWM frequency (duty frequency), the number of positive to negative transitions (comparator saturation points) needed to be changed. In order to do this, the frequency of the sinusoidal wave was changed, effectively changing the comparator saturation points. Therefore, changing the duty frequency involved changing the frequency component of each of the three duty frequency sinusoidal sources (one for each phase) in the inverter circuit (shown in Figure 20) as shown in Figure 22.

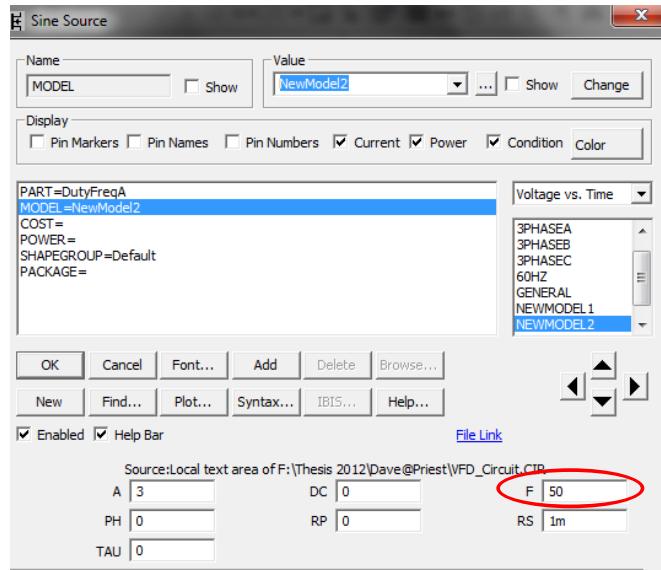


Figure 22 - Changing the Duty Frequency of the Circuit Model

Changing the carrier frequency involved changing the frequency of the triangular wave source. In MicroCAP, a triangular wave is modelled as a square wave source with the rise time and fall time equal to half the period and a negligible pulse width. Therefore, when changing the pulse source characteristics in Figure 23:

- The pulse starting time (P1) was kept at 0 seconds
- The rise time (P2) equalled half the period of the waveform
- The falling edge of the pulse (P3) equalled P2 as the pulse width was negligible
- The fall time (P4) equalled the period of the waveform
- The pulse ending time (P5) equalled P4

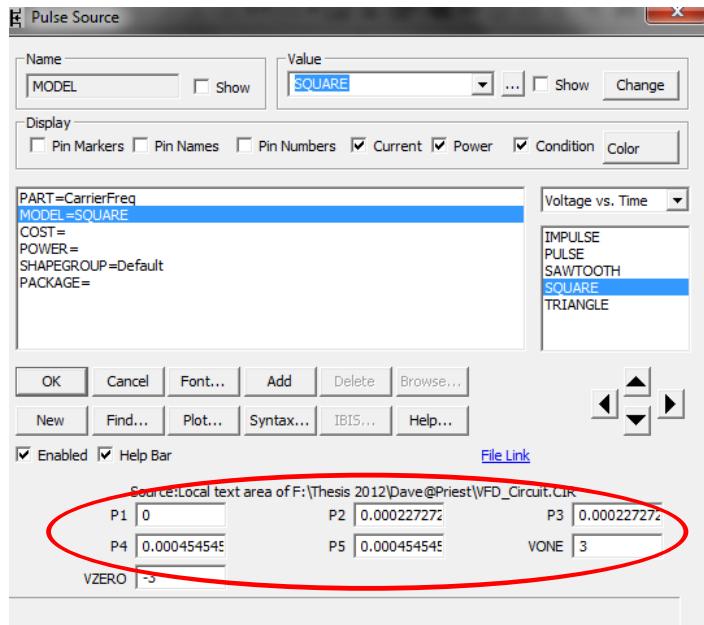


Figure 23 - Changing the Carrier Frequency of the Circuit Model

However, it was noted that this model did not automatically keep the output terminal voltage to frequency ratio constant as with the practical VFDs. Consequently, it was decided to investigate how to vary the output voltage from the circuit model AC drive to improve the model accuracy.

It was suggested that scaling the amplitude of the sinusoidal duty frequency sources could also scale the voltage of the output by the same factor. However, this theory needed to be proved before implementing this method. To prove this theory, it was decided that the VFD output waveforms should be plotted, with the initial duty frequency amplitude and then with a scaled duty frequency amplitude. Since the output waveforms were pulse-width-modulated, it was difficult to calculate the peak voltage. Therefore, a Butterworth low-pass filter with a 50 Hz cut-off frequency was designed to average the voltage and create an effective sinusoidal waveform as shown in Figure 24.

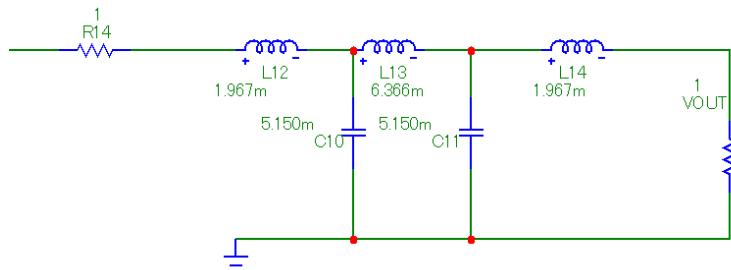


Figure 24 - LPF with 50 Hz Cut-off Frequency

The resulting plots showed that the scaled duty frequency amplitude scaled the output waveform by the same factor without affecting the output waveform frequency. Since the incoming signal to the VFD maintained a frequency of 50 Hz, it was decided that the voltage/frequency ratio for this speed would be held constant throughout all circuit model tests. Therefore, the initial amplitude values of the duty frequency sources were scaled by the ratio of the new duty frequency/50 Hz.

3.9 Methodology Summary

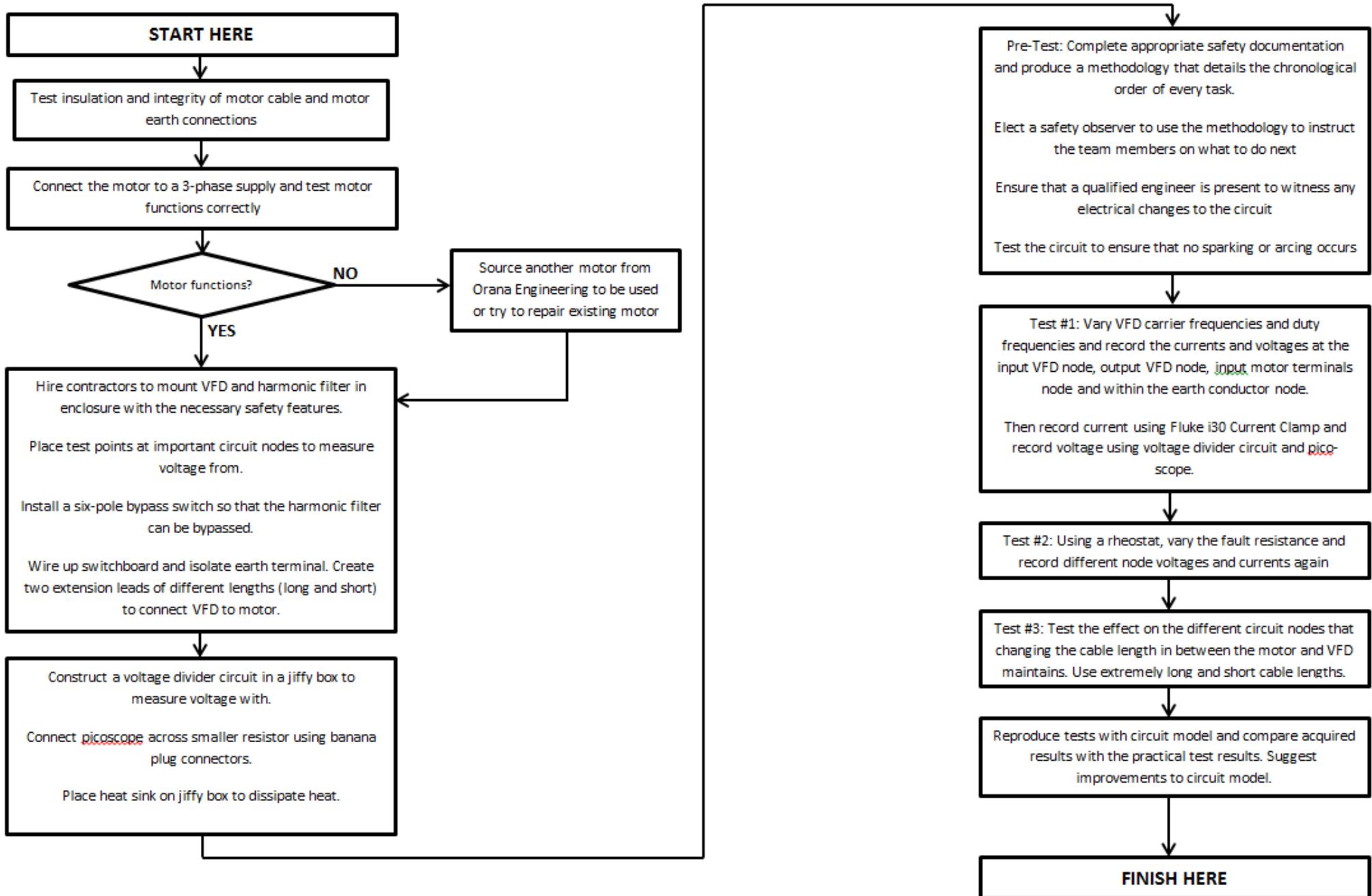


Figure 25 - Flowchart illustrating the tasks performed in the Methodology

CHAPTER FOUR

4 EXPERIMENTAL DATA

4.1 Comparison of Experimental and Simulation Circuit Model Results

4.1.1 Comparison of Node Voltage at Output of VFD (Test #1)

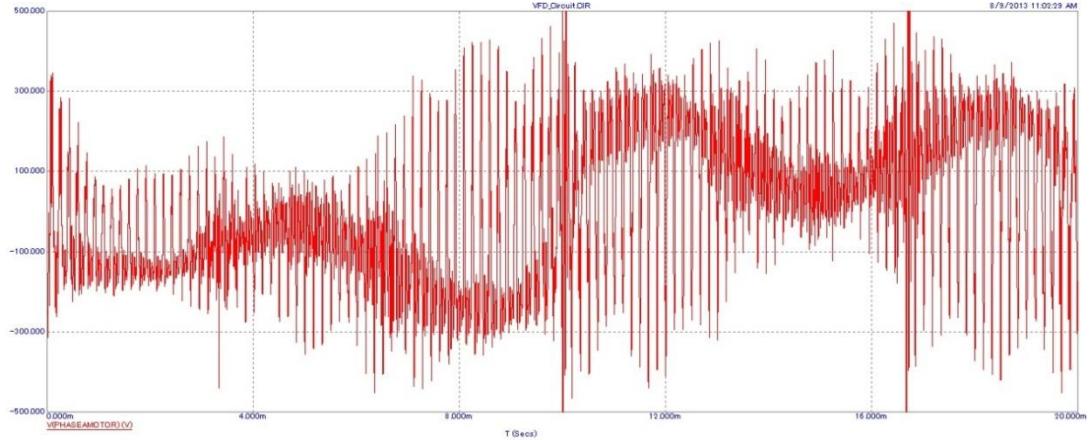


Figure 26 - Circuit Model Node Voltage at Output of VFD when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

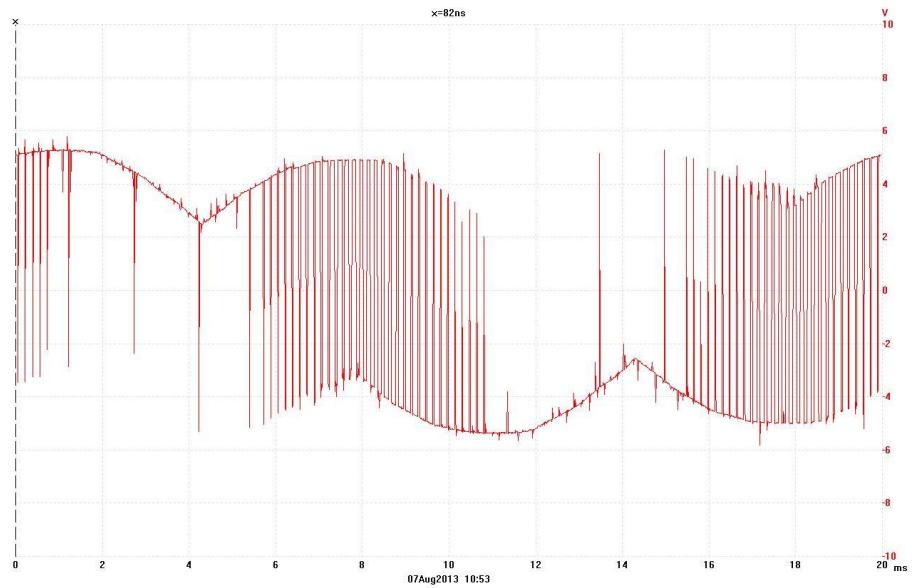


Figure 27 – Actual Node Voltage at Output of VFD when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

$$\text{Actual Experimental Voltage} = \frac{10k + 6.8k + 330||1.2k}{330||1.2k} \times \text{Measured Voltage Level} \quad (6)$$

Equation (6) was used to calculate the actual voltage level experienced at the nodes in the experiments. After applying this equation it was seen that the output VFD voltage experimental response peaked at 333 V and had transients of approximately 100 V about this value, as shown in Figure 27. The peaks of 333 V were expected as this is the peak voltage of the input phase signal to the VFD.

When comparing Figure 26 and Figure 27, it was seen that the circuit model response maintained significant oscillatory ringing behaviour prevalent in each pulse and had considerably sized transients which were sometimes in excess of 200 V. This was put down to the fact that the circuit model motor load did not include motor inductances, which would have the effect of filtering out some of the ringing. Also, it was deduced that the practical VFD internal circuitry must contain methods of limiting the oscillatory ringing behaviour which had not been encompassed in the circuit model. Consequently, the experimental waveform in Figure 27 maintained a lot cleaner pulses than the circuit model response in Figure 26. Furthermore, the waveform pulses in the circuit model appeared to peak at 240 V and not 333 V. This was due to the fact that the input generator for the circuit model maintained peak amplitudes of 240 V, when that is actually only the RMS value. Therefore, the model was changed and the correct input generator frequency value of 333 V was inputted. It was decided that the waveforms were similar in shape and were probably the best correlation which could be achieved for a generic model.

4.1.2 Comparison of Node Current at Output of VFD (Test #1)

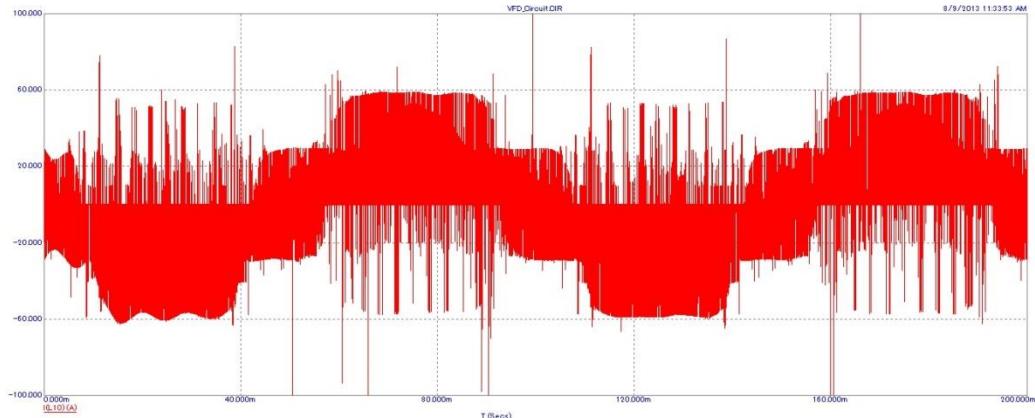


Figure 28 - Circuit Model Output VFD Current when Carrier Frequency is 6 kHz and Duty Frequency is 10 Hz

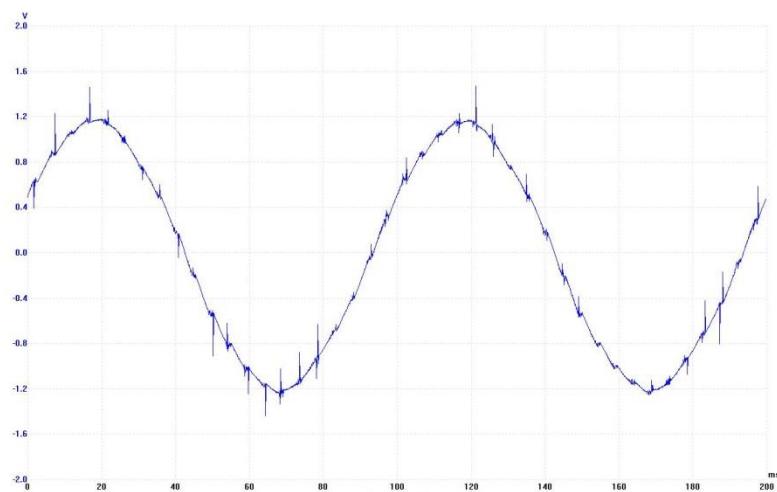


Figure 29 – Actual Output VFD Current when Carrier Frequency is 6 kHz and Duty Frequency is 10 Hz

$$\text{Actual Current Level} = \frac{\text{Measured Voltage Level}}{0.1} \quad (7)$$

Equation (7) was used to calculate the actual current level experienced at the nodes in the experiments. After applying this equation, it was seen that the output VFD current experimental response peaked at 12 A, as can be seen in Figure 29. However, Figure 28 showed that the simulation model did not accurately represent the current experienced in practical situations. There were significant transients and overshoots and the general sinusoidal shape experienced with the experimental results was definitely not encompassed in this simulation. This was yet again put down to the circuit model motor load not including motor inductances, which filter part of the waveform, and the VFD maintaining internal circuitry that limits the oscillatory ringing behaviour. Therefore, it was decided that the circuit model produced an unreliable current response at the output of the VFD.

4.1.3 Comparison of Earth Conductor Current (Test #1)

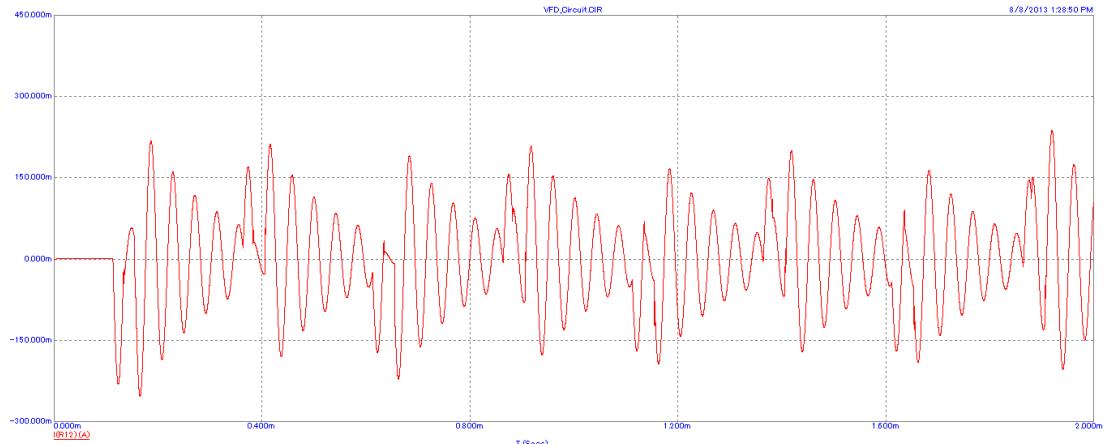


Figure 30 – Circuit Model Earth Conductor Current with Carrier Frequency of 2 kHz and Duty Frequency of 10 Hz

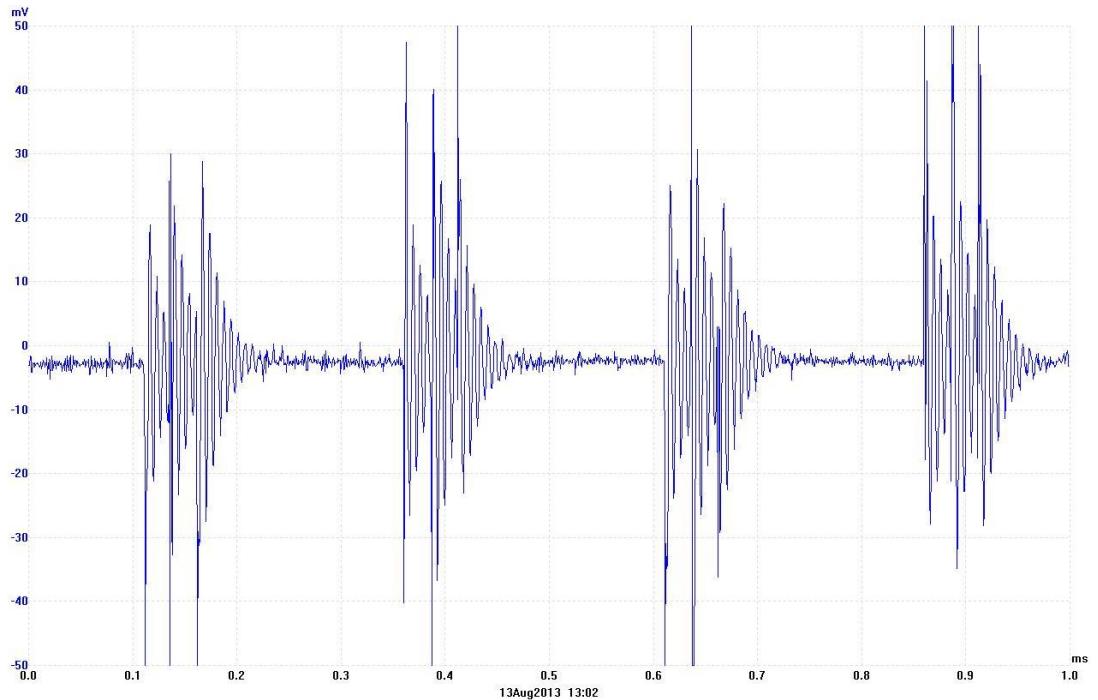


Figure 31 – Actual Earth Conductor Current with Carrier Frequency of 2 kHz and Duty Frequency of 10 Hz

When applying Equation (7) it was seen when viewing Figure 31 that the earth conductor current often peaked at approximately 150 - 200 mA for extremely short periods of time in the experimental response. There were also major sized transients over 500 mA, which occurred infrequently. Since these transient peaks occurred for such short periods of time, it was decided that they would not trip an earth leakage relay with appropriate time discrimination settings.

When Figure 30 and Figure 31 were compared, it was found that there was a definite correlation between the circuit model and experiment responses. The only difference was that the experimental response in Figure 31 had more oscillatory behaviour in the experimental results than in the circuit model response. This discrepancy was put down to the fact that the circuit model did not account for the practical stray reactances which would be prevalent and would cause more oscillatory ringing. Lastly, the circuit model suggested frequent peaks of 200 mA (which was similar to the experimental response).

4.1.4 Comparison of Circuit Reaction to Earth Fault (Test #2)

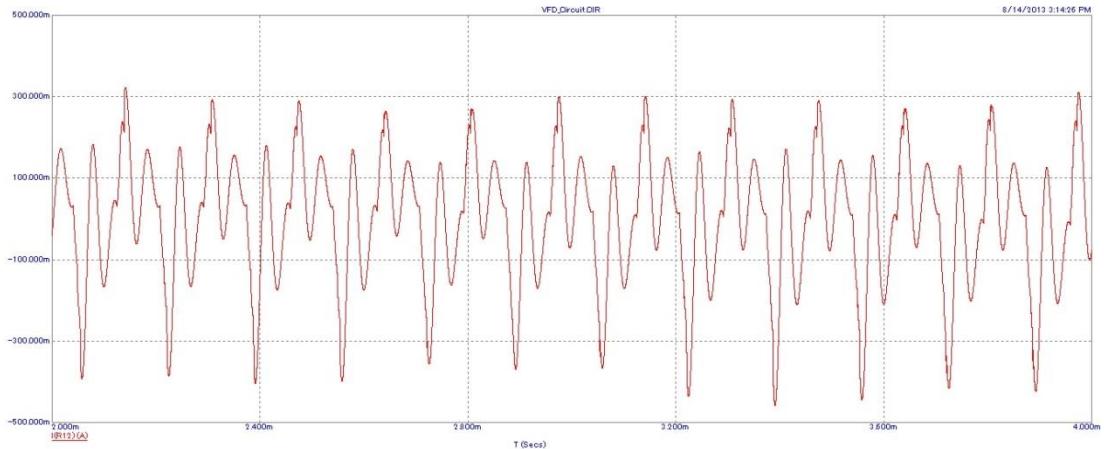


Figure 32 - Circuit Model Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with Earth Fault of 3.375 k Ω

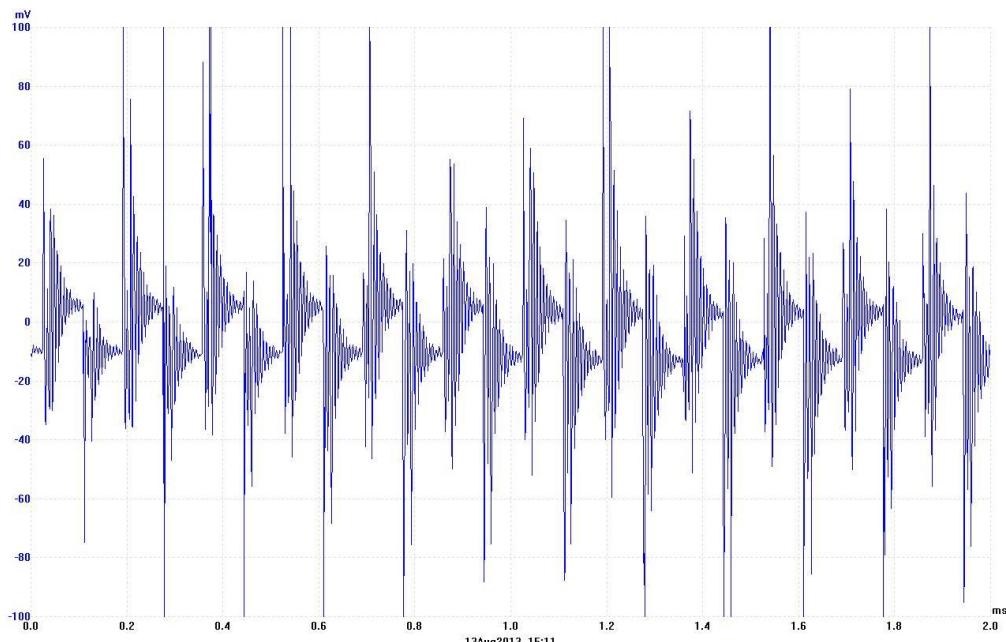


Figure 33 – Actual Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with Earth Fault of 3.375 k Ω

Using Equation (7), it was calculated that with an earth fault of 3.375 k Ω , the experimental current waveform in Figure 33 resembled a pulsed waveform with pulse heights of approximately 50 – 100 mA. Also, it was noted that there was considerable ringing and transients at the rising and falling edge of each pulse. It was decided that the pulse height value probably would come very close to tripping earth leakage relays, which normally have trip levels of 100 mA set. As can be seen in Figure 32, the circuit model response, with an earth fault of 3.375 k Ω , maintained a moderately similar waveform to that in Figure 33, with the outline of a pulsed waveform containing transient overshoots apparent. It appeared that the transients spiked to about 300 mA and the actual pulse heights were approximated to 100 mA (similar to the experimental response). With an earth fault of 3.375 k Ω , it was decided

that there was a definite correlation between the circuit model and experiment earth conductor responses.

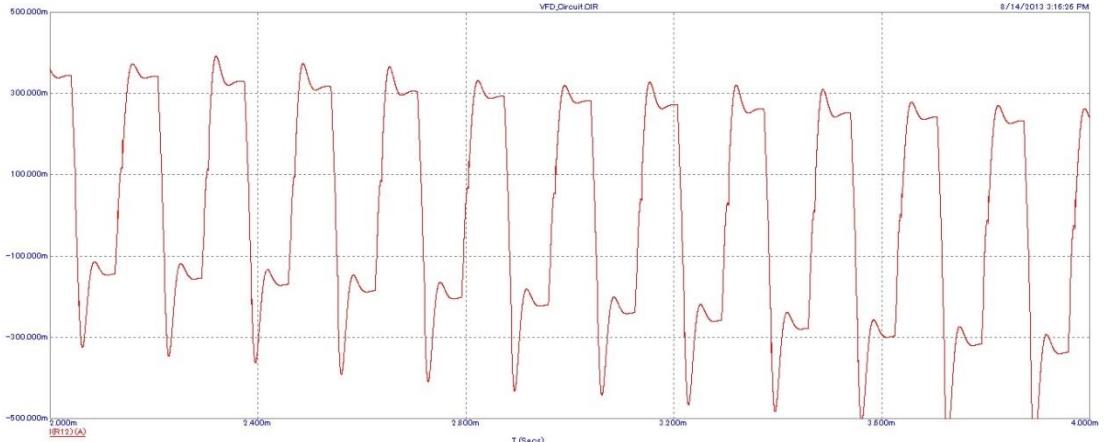


Figure 34 - Circuit Model Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with Earth Fault of $761\ \Omega$

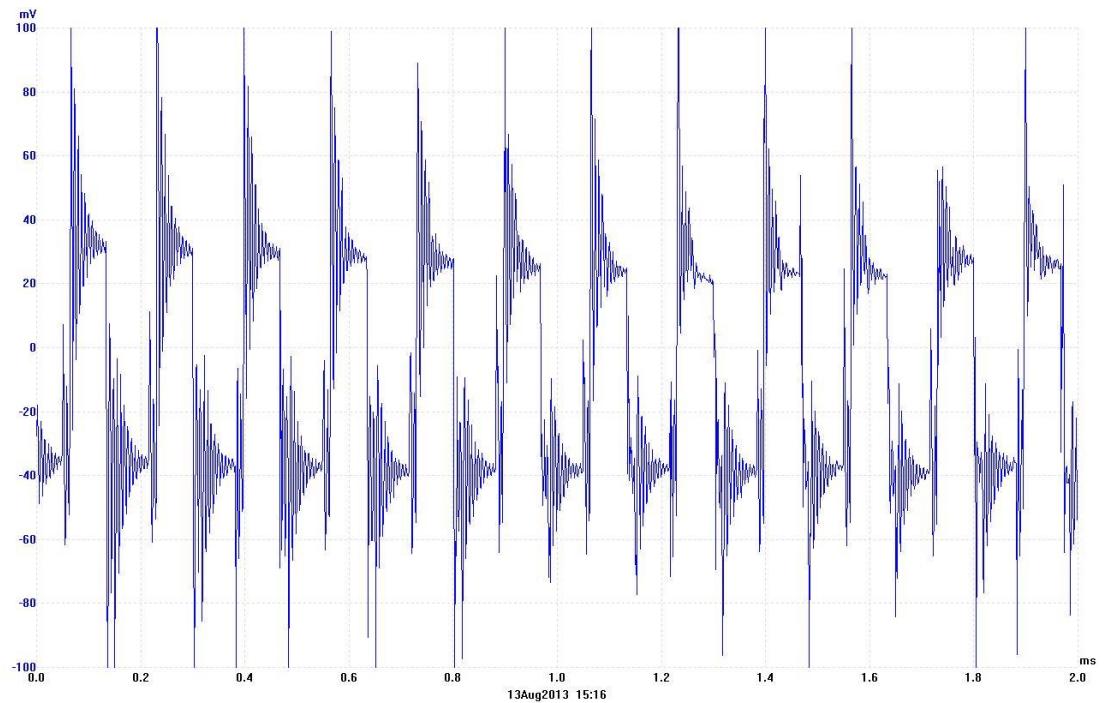


Figure 35 – Actual Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with Earth Fault of $761\ \Omega$

Using Equation (7), it was calculated that with an earth fault of $761\ \Omega$, the experimental current waveform in Figure 35 yet again resembled a pulsed waveform with pulse heights of approximately 300 mA. There was also yet again considerable ringing and transients at the rising and falling edge of each pulse. It was decided that this pulse height would definitely trip an earth leakage relay with a normal trip level of 100 mA.

When comparing Figure 34 and Figure 35, it was seen that the circuit model was fairly accurate in producing approximations of the experimental response. The circuit model pulse height peaked at the roughly the same as the experimental response pulse heights (300 mA),

but did not contain as many transients or have as much oscillatory behaviour present. This was yet again put down to the circuit model not including the effect of stray reactances. Therefore, it was decided that the circuit model did approximate earth conductor waveforms in the presence of a fault to ground.

However, it was observed that the experimental responses may not have best represented a real world situation as there was no loading on the motor. Also, this investigation had not given any evidence suggesting whether the circuit model would still give reasonably accurate approximations of the experimental results if a load was also used. Therefore, it was recommended that future investigations endeavour to fix the DC generator coupled to the motor and perform future tests with a loaded motor. However, an alternative future investigation, which would be easier, would be to look at updating the circuit model motor load with an accurate induction motor model. Since the circuit model gives similar results to the experimental model, the effect of loading a VFD circuit could be gauged without having to perform the costly process of repairing the DC generator.

4.1.5 Comparison of Circuit Reaction to Cable Length Change (Test #3)

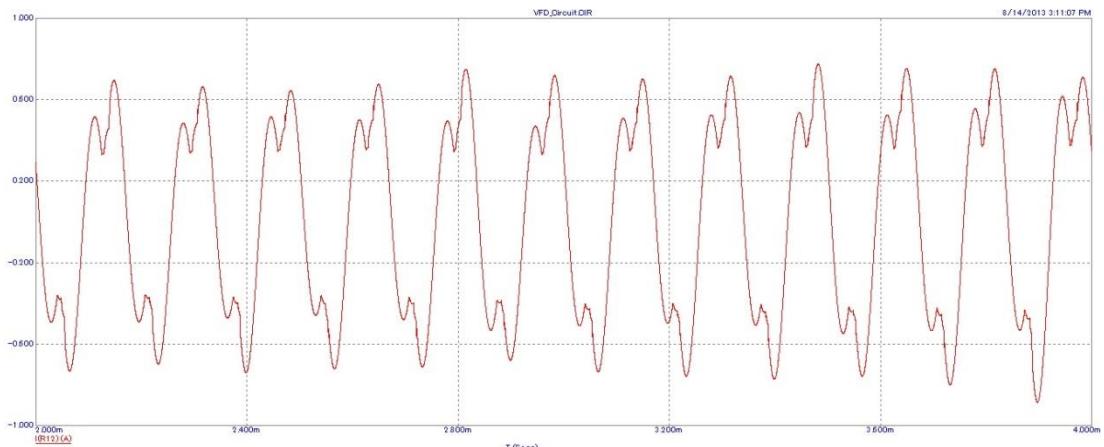


Figure 36 - Circuit Model Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with longer 50 m cable and original capacitance value of 15 nF

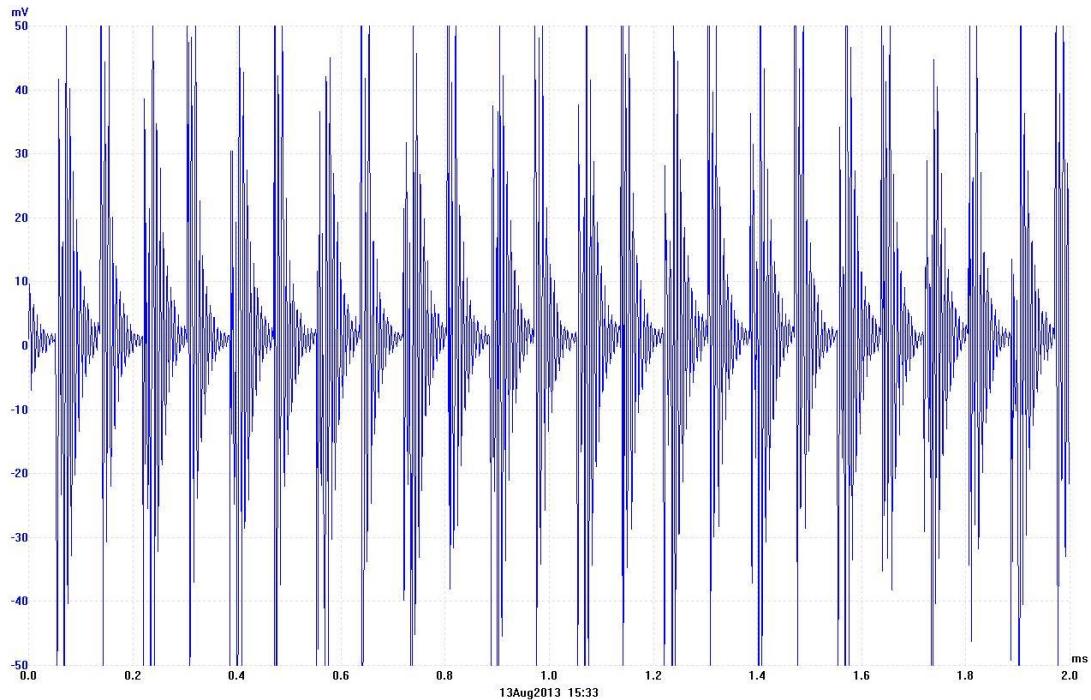


Figure 37 - Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with longer 50 m cable

To change the cable length in the circuit model, the capacitance value already assigned for 10 m of cable in between phase to earth (3 nF) was changed by a factor of five (15 nF) to simulate a cable five times longer. It was seen in Figure 37, that the experimental response maintained significant oscillatory ringing and had considerably sized transient in excess of 500 mA. It can be seen by comparing Figure 36 and Figure 37 that the circuit model was not reliably accurate in representing the earth conductor current with a longer cable. The circuit model in Figure 36 did not depict any evidence of ringing like the experimental responses did.

It was thought that the reason for this discrepancy may have been that the original capacitance value in the circuit model for 10 m of cable (3 nF) probably would not have accurately represented the capacitance value for the VFD rated cable. Therefore, the capacitance of the actual VFD cable was measured using a capacitance tester, giving the results shown in Table 1. It was seen that the circuit model capacitances were approximately out by a factor of three. Therefore, Test #3 was repeated again in the circuit model, with the new cable capacitance values, to see if the accuracy of the circuit model improved.

Table 1 - Comparison of Circuit and Actual Cable Capacitances

Length of Cable	Circuit Model Capacitance	Actual Cable Capacitance
10 m	3 nF	963.4 pF
50 m	15 nF	4.861 nF

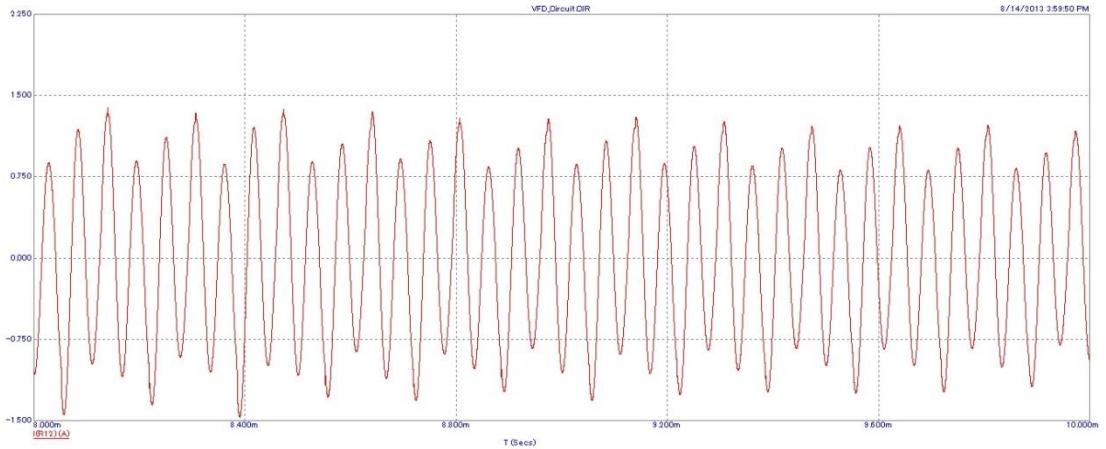


Figure 38 - Circuit Model Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with longer 50 m cable and new capacitance value of 4.861 nF

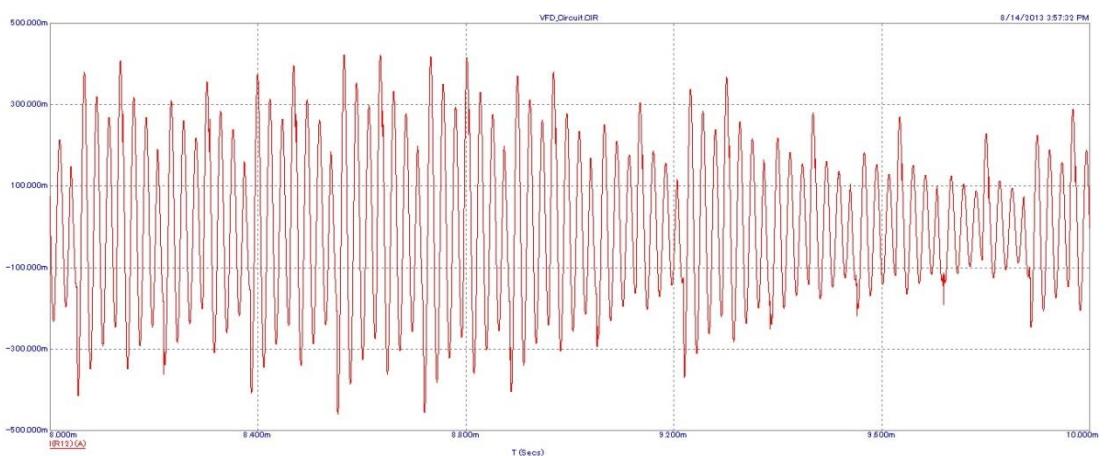


Figure 39 - Circuit Model Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz with short 10 m cable and new capacitance value of 963.4 pF

When Figure 38 and Figure 37 were compared, it was seen that the circuit model in Figure 38 now had a response with a similar shape to the experimental response in Figure 37. Furthermore, when comparing the length of the cables in the circuit model, it was seen that the longer cable response in Figure 38 maintained higher transients (approximately 1.3 A) than the shorter cable response in Figure 39 (with transient heights of approximately 400 mA). This proved the theory that longer cables in between the VFD and motor did exacerbate earth leakage issues. However, it was also decided that it would be prudent for future investigations to test using different cable types to see if the VFD rated cable is actually better than generic cable types for use with VFDs.

4.2 Effects of Changing Duty Frequency

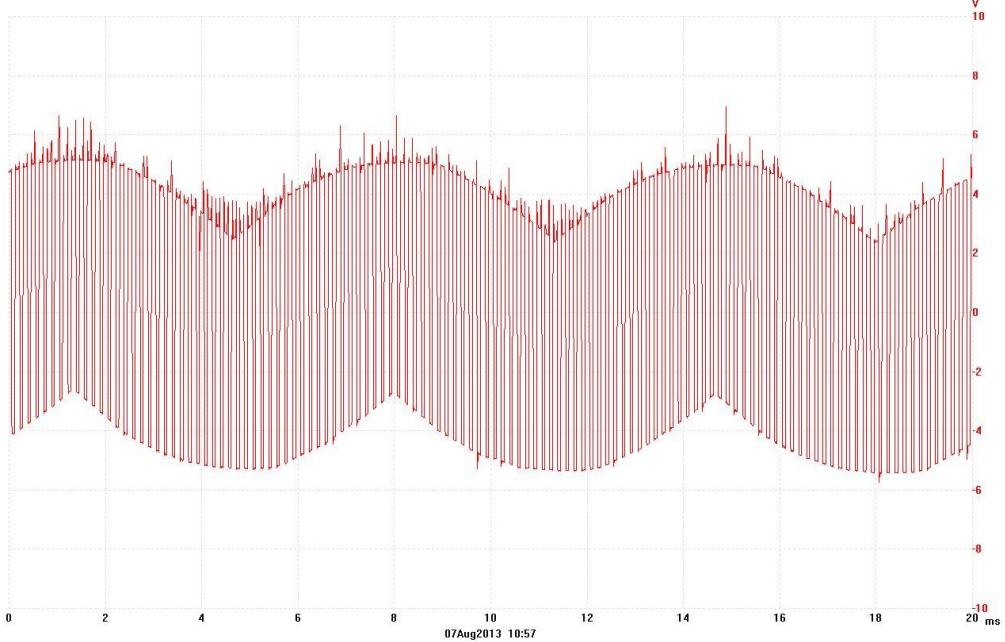


Figure 40 - Node Voltage at Output of VFD when Carrier Frequency is 6 kHz and Duty Frequency is 10 Hz

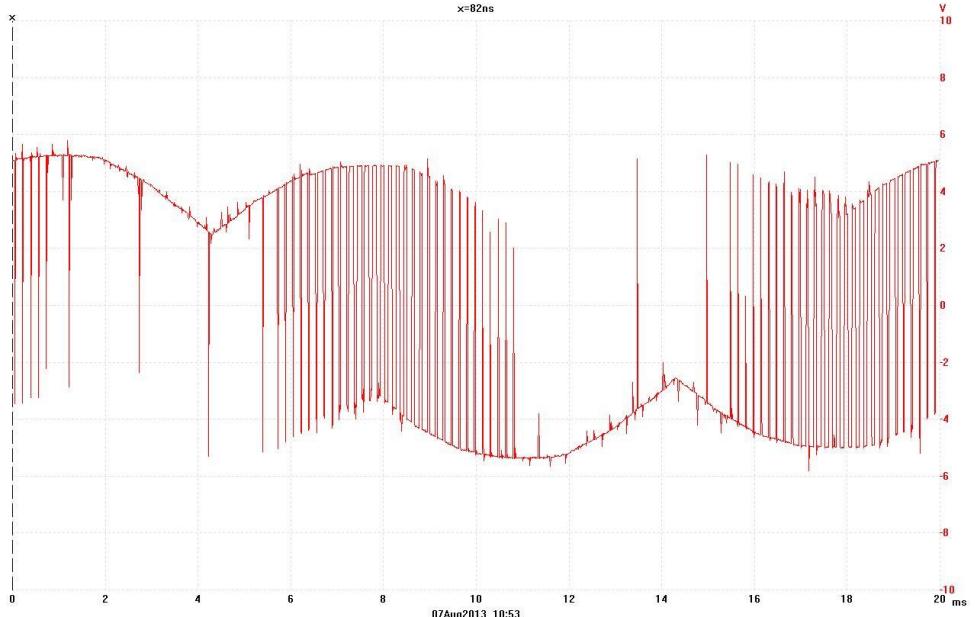


Figure 41 - Node Voltage at Output of VFD when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

When Figure 40 was examined (10 Hz waveform), it was seen that the pulse width was small and almost constant. However, for Figure 41 (50 Hz waveform), it was seen that the pulse width for the 50 Hz duty frequency varied from very wide to very small. There were large pulses in the 50 Hz waveform that stayed at the high/low saturation voltage levels for considerable periods of time during the cycle of the waveform. The reason for the smaller PWM pulse widths in the 10 Hz waveform was that to keep the voltage/frequency ratio constant (to maximise torque and maintain the V/F ratio), the voltage of the 10 Hz waveform

had to be decreased. Similarly, to keep the voltage/frequency ratio constant for the 50 Hz waveform, the voltage needed to be increased, which is why there were large pulse widths present in Figure 41. The reason for the variable pulse sizes in the 50 Hz waveform was that the higher duty frequency required more positive to negative transitions (pulses) to represent a higher duty frequency. Due to the presence of the larger pulses, these pulse transitions could only be squeezed in between the larger pulses, thus creating variable pulse widths.

It was seen that the constant nature of transitions for the 10 Hz waveform produced more transients than for the 50 Hz waveform, as can be seen in Figure 40. Theory therefore suggested that lower duty frequencies would result in greater earth leakage current issues as the larger number of rapid changes in voltages (unlike with higher duty frequencies where there are larger pulse widths) would cause higher capacitive leakage currents ($I = C \cdot dv/dt$).

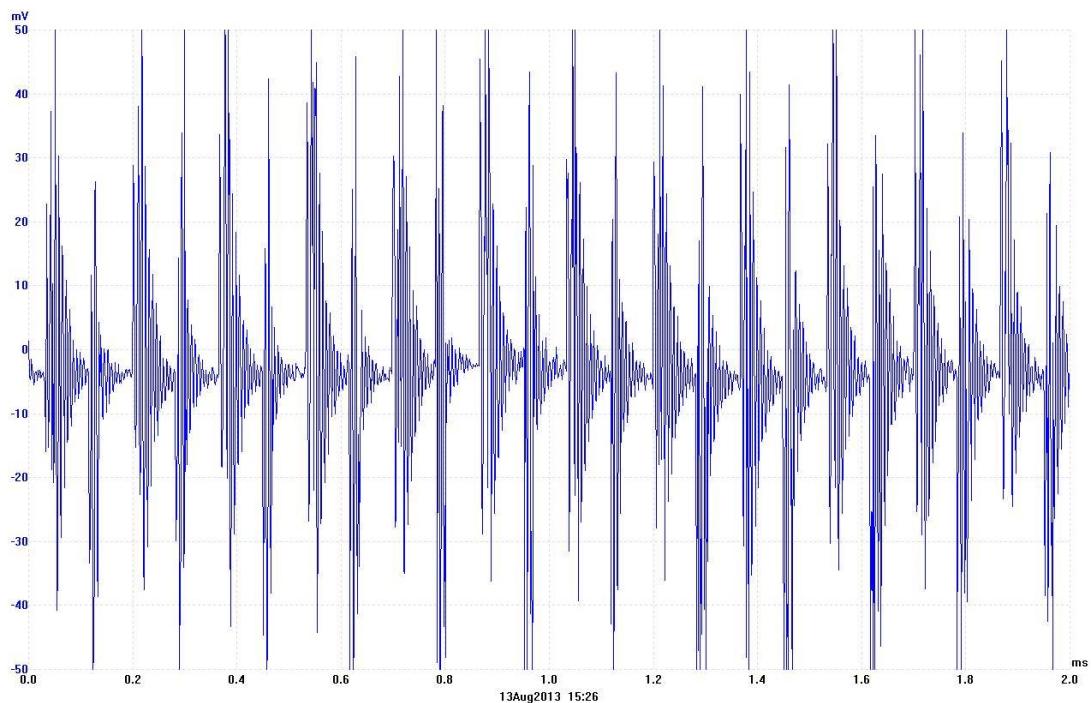


Figure 42 - Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 10 Hz

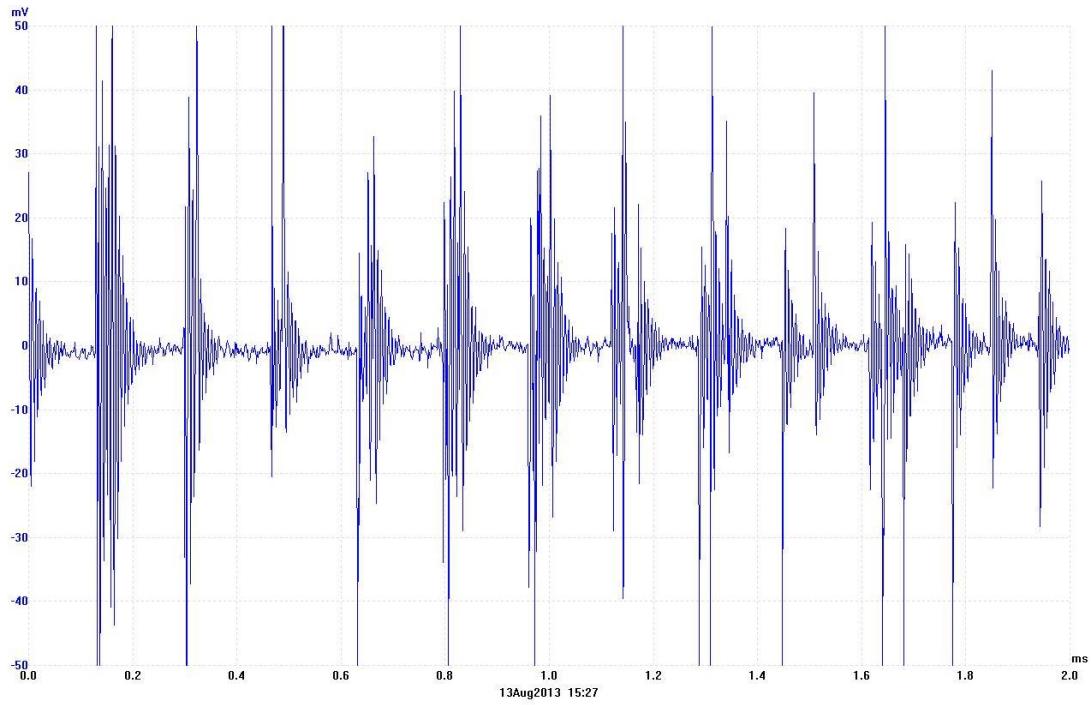


Figure 43 - Earth Conductor Current with Carrier Frequency of 6 kHz and Duty Frequency of 50 Hz

However, when Figure 42 and Figure 43 were compared (earth conductor current), it was seen that increasing the duty frequency in the constructed test environment decreased the frequency of the transients and therefore had a lower average earth conductor current. This aligned with the theory suggesting that the 10 Hz signal should have had more earth leakage current than the 50 Hz.

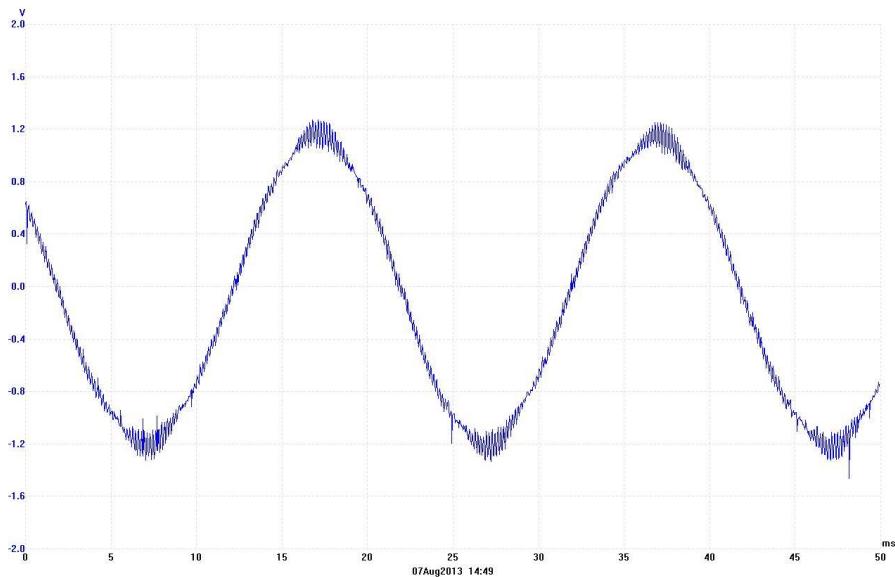


Figure 44 - Output VFD Current when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

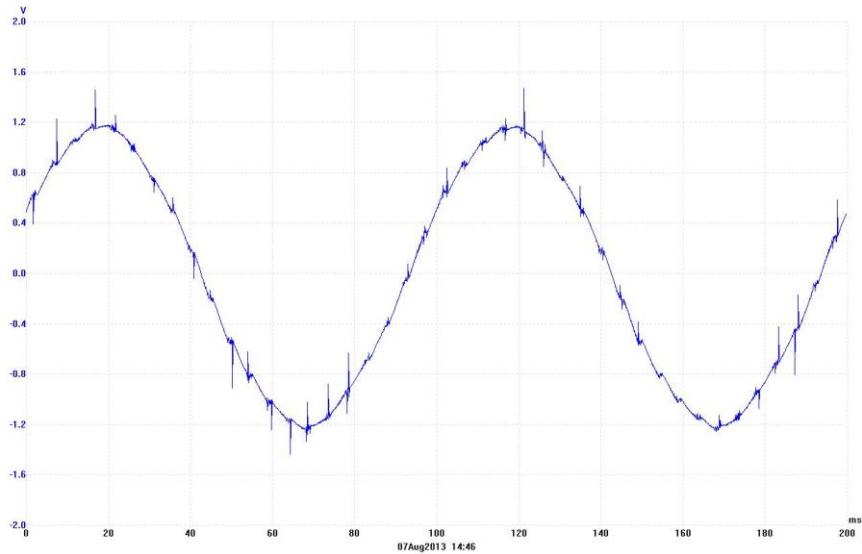


Figure 45 - Output VFD Current when Carrier Frequency is 6 kHz and Duty Frequency is 10 Hz

It can be seen from Figure 44 and Figure 45 that there was significant ringing that occurred in the VFD output current, particularly at the peaks of the sinusoids, at the higher duty frequency. One possible theory that was derived to explain why this happened was that the overall inductive reactance of the motor, which is dependent on frequency, increased as the duty frequency increased. A higher inductance may have then caused the resonance issues.

Also, it appeared that the ringing effects in the current waveform were exacerbated at points where the pulses widths in the voltage waveforms were larger. This can be seen in Figure 44 where the ringing effects are more significant at the peaks of the current waveform (where the pulses for the voltage waveform would be larger). Furthermore, there was less ringing in the 10 Hz current waveform (Figure 45) which maintained constant smaller width pulses. Therefore, a theory was deduced that formulated a correlation between larger width pulses and less frequent pulses in the voltage waveform causing more significant ringing effects in the current waveforms. However, this theory needs to be proved before it can be validated.

4.3 Effects of Changing Carrier Frequency

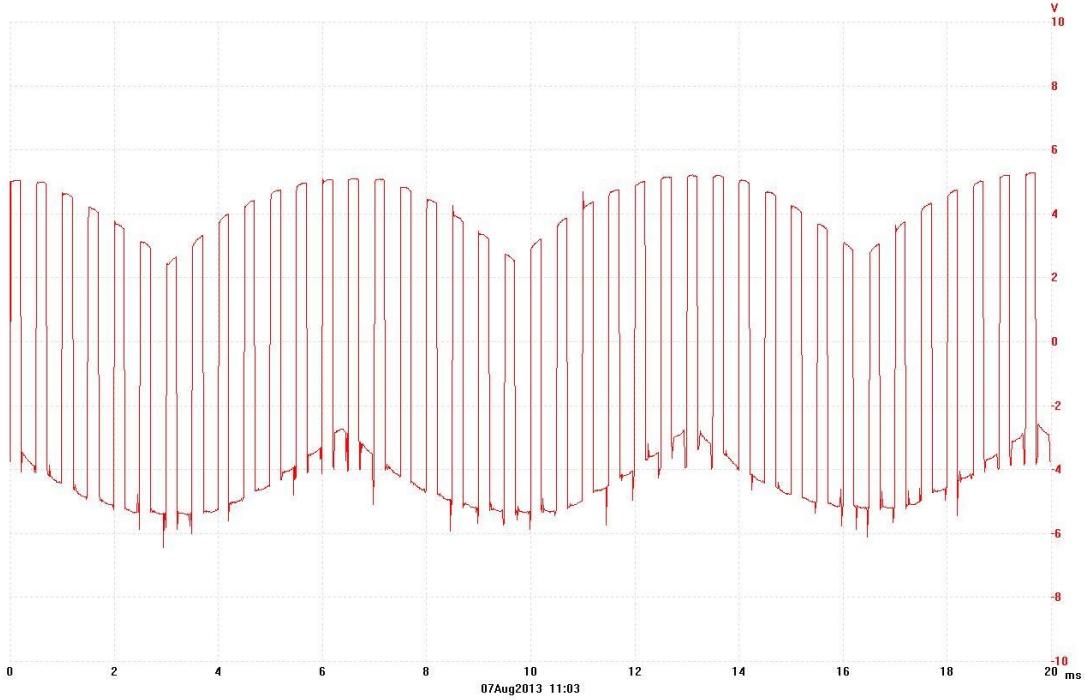


Figure 46 - Node Voltage at Output of VFD when Carrier Frequency is 2 kHz and Duty Frequency is 10 Hz

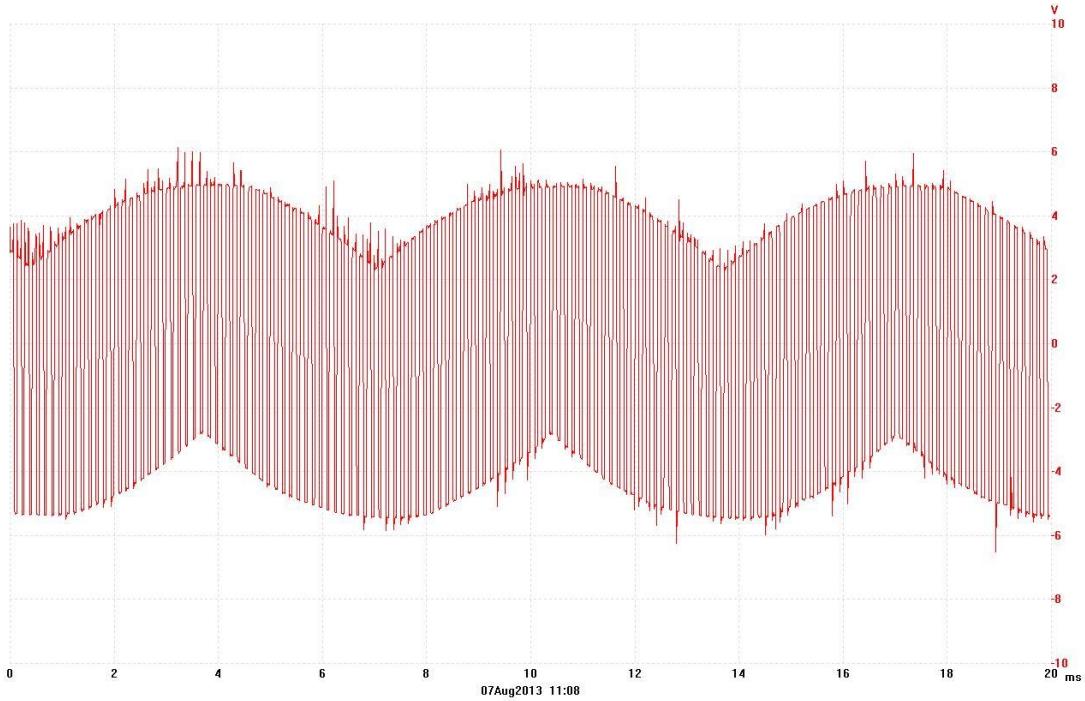


Figure 47 - Node Voltage at Output of VFD with Carrier Frequency of 15 kHz and Duty Frequency of 10 Hz

When Figure 46 and Figure 47 were compared (VFD output voltage), it was seen that increasing the carrier frequency decreased the period of the switching and therefore added more pulses to increase the resolution of the effective sinusoidal representation. This has the combined effect of causing more transients (faster switching) and maintaining higher drive losses as the carrier frequency is increased. Also, the more rapid switching will cause higher

capacitance currents as $I = C \cdot dv/dt$. Therefore, it can be surmised that a low duty frequency and high carrier frequency will typically result in more sizeable earth leakage currents.

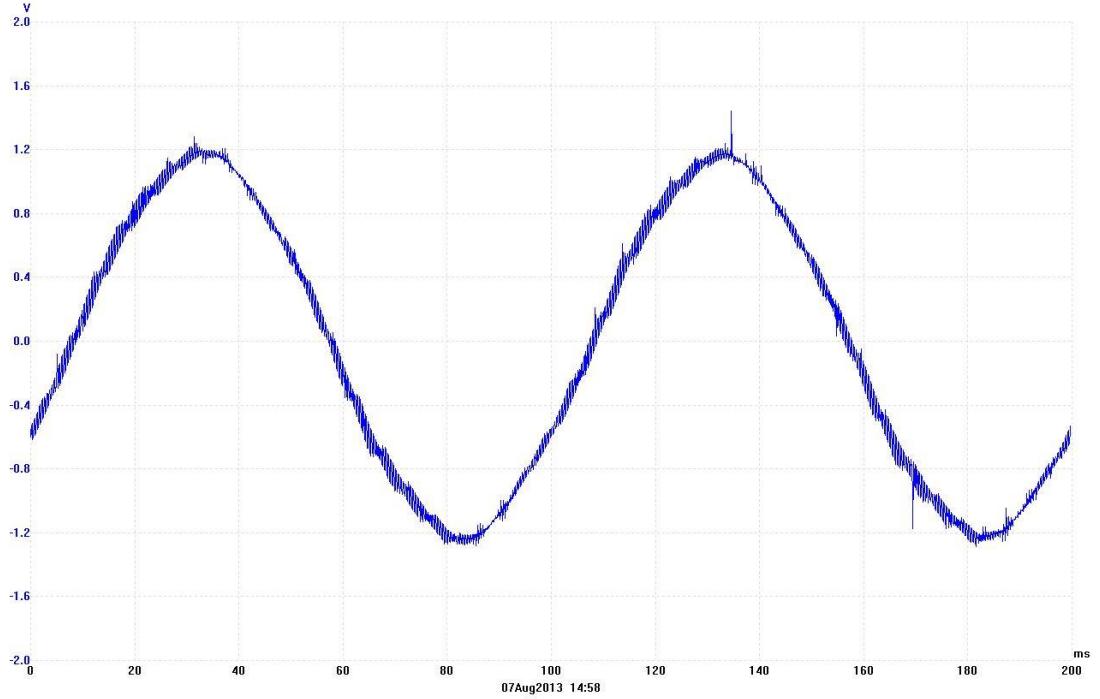


Figure 48 - Output VFD Current when Carrier Frequency is 2 kHz and Duty Frequency is 10 Hz

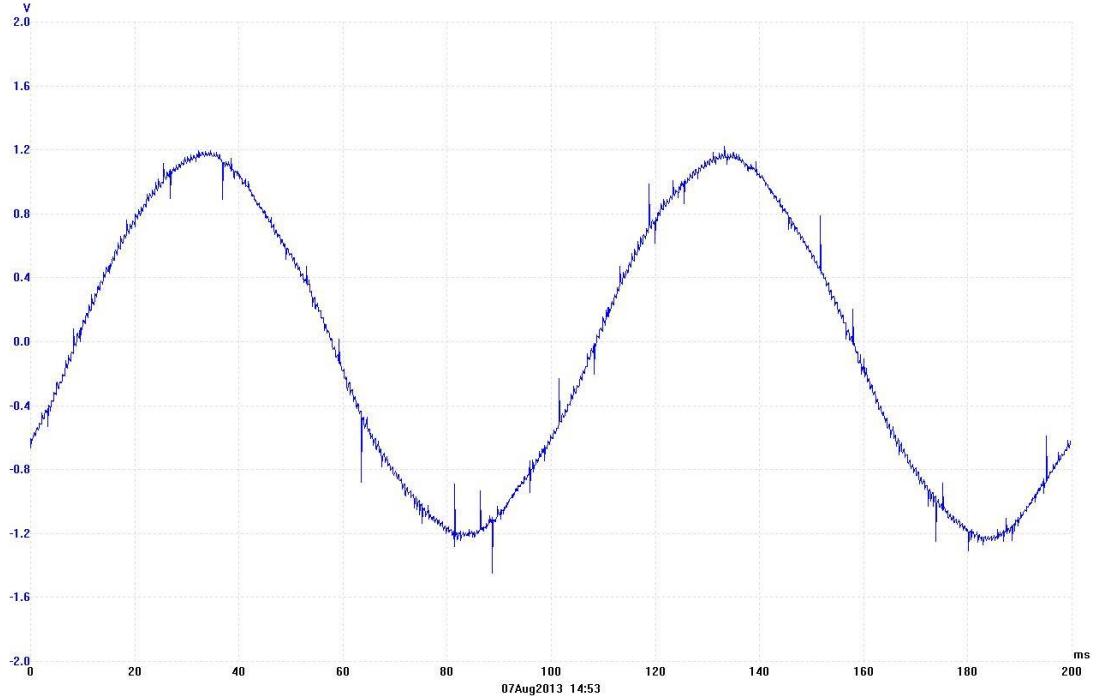


Figure 49 - Output VFD Current when Carrier Frequency is 15 kHz and Duty Frequency is 10 Hz

When comparing Figure 48 and Figure 49 (VFD output current), it was seen that the smaller carrier frequency waveform (2 kHz) maintained more ringing. Also, the smaller carrier frequency maintained larger width pulses and less frequent pulses as can be seen in Figure

46. This reinforced the theory suggesting that larger width pulses and less frequent pulses in the voltage waveform would cause more significant ringing effects in the current waveforms.

4.4 Effects of the Harmonic Filter

4.4.1 Effect on the Output VFD Voltage

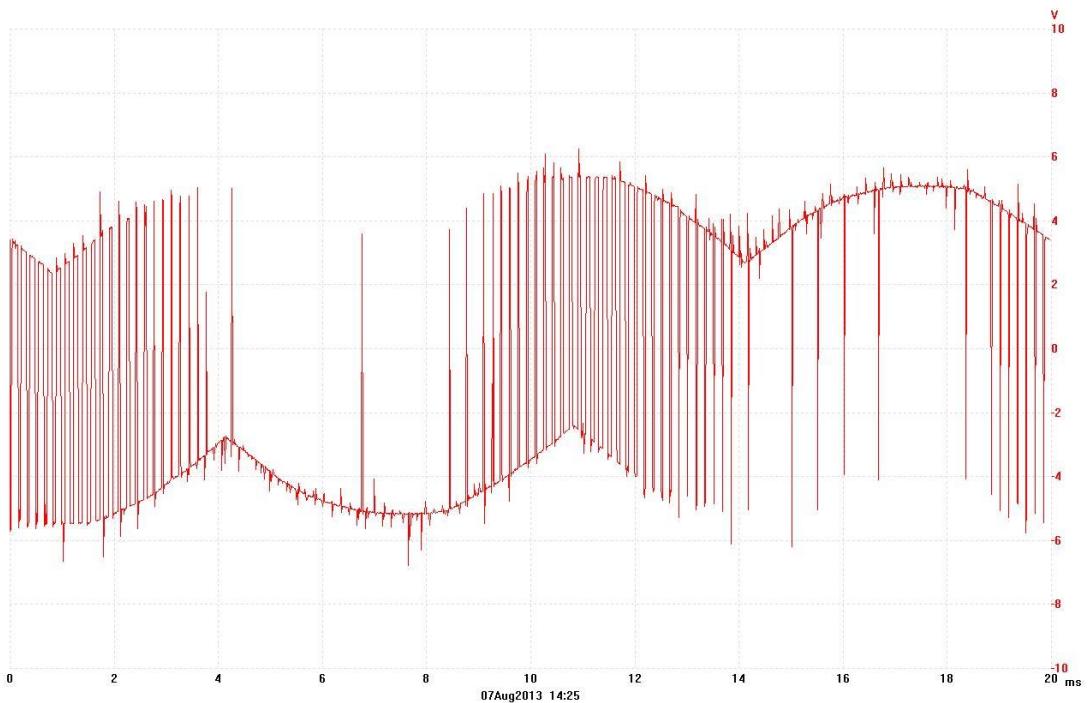


Figure 50 - Node Voltage at Output of VFD with Carrier Frequency of 6 kHz and Duty Frequency of 50 Hz

When Figure 50 (without harmonic filter) and Figure 41 (with harmonic filter) were compared, it was seen that the harmonic filter did not make any difference to the output voltage. This was expected as the harmonic filter was designed to stop harmonic reflections back to the line side and therefore should not affect the output waveform much.

4.4.2 Effect on the Input VFD Voltage

It was seen from the comparison of Figure 51 (without harmonic filter) and Figure 52 (with harmonic filter) that the harmonic filter removed the ringing and transients present in Figure 51 to give a cleaner input (line side) waveform in Figure 52. Therefore, the harmonic filter does actually work to produce a cleaner voltage input waveform to the VFD and should always be used in tandem with VFDs.

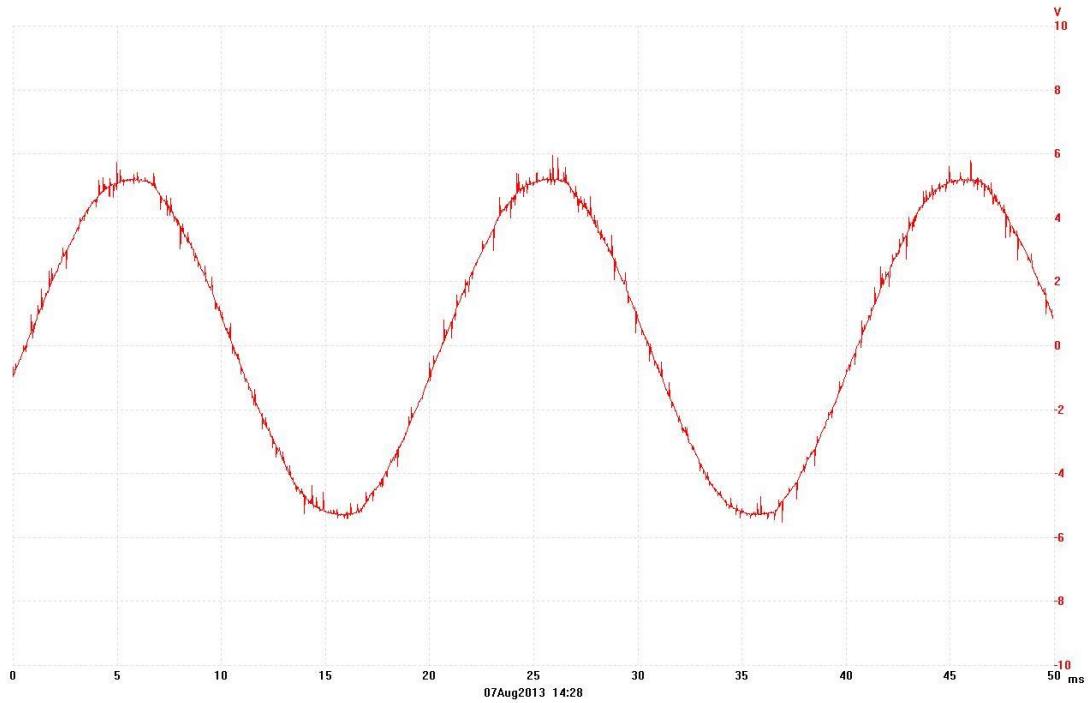


Figure 51 - Node Voltage at Input to VFD without Harmonic Filter

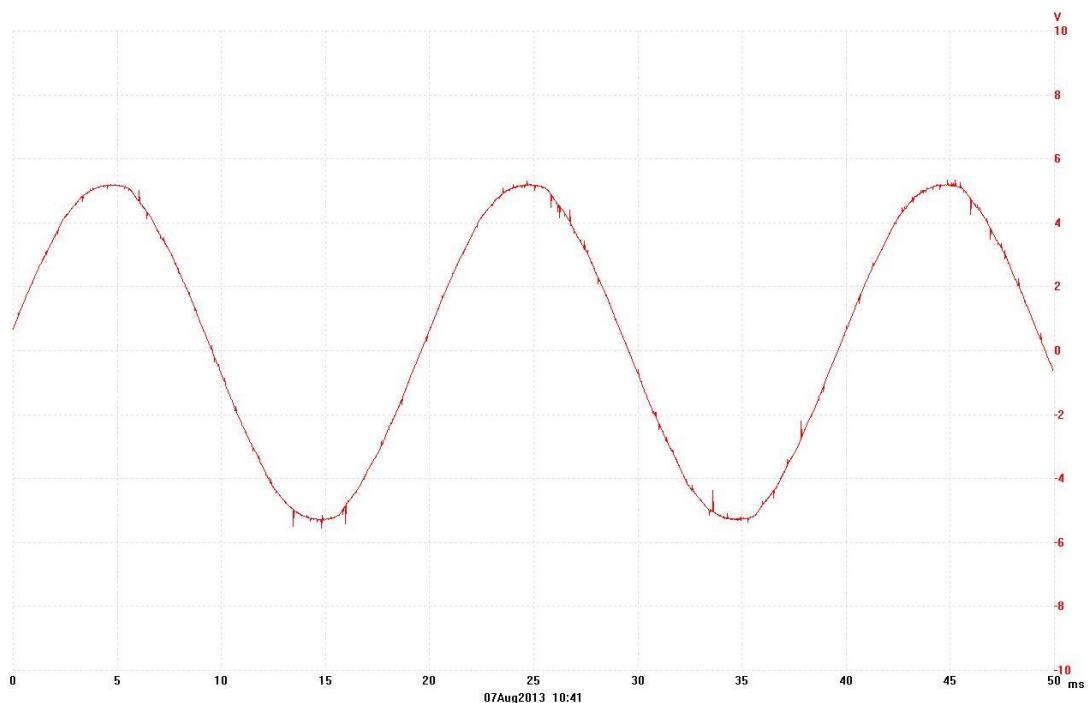


Figure 52 - Node Voltage at Input to VFD with Harmonic Filter

4.4.3 Effect on the Input VFD Current

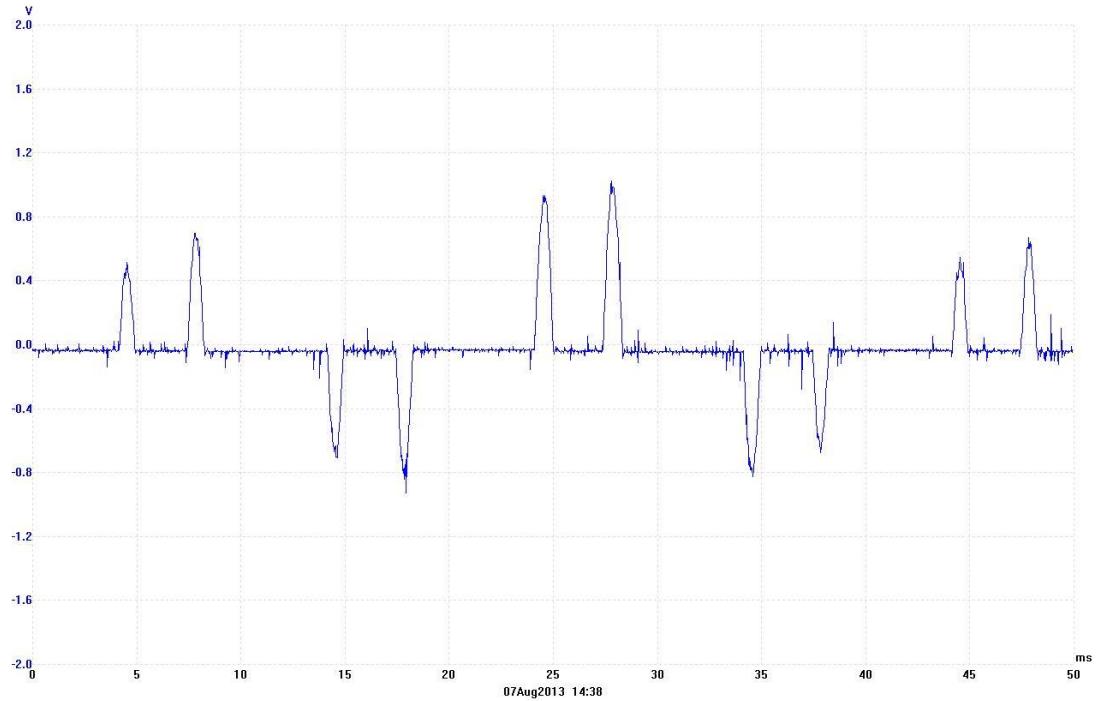


Figure 53 - Input VFD Current without Harmonic Filter when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

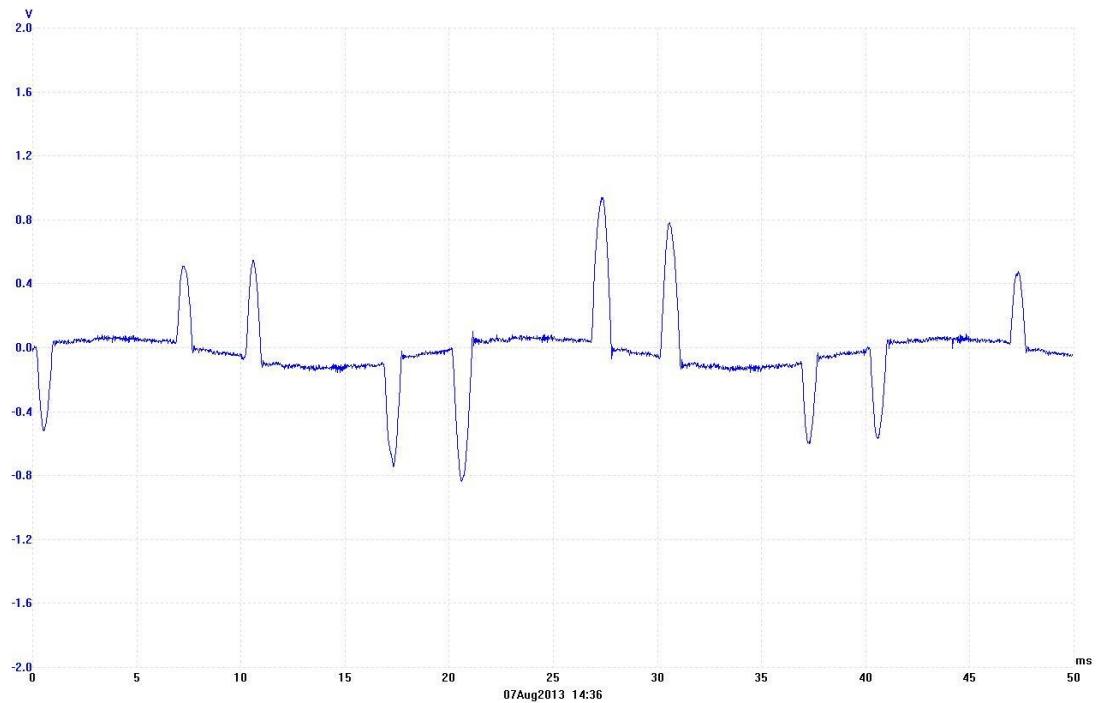


Figure 54 - Input VFD Current with Harmonic Filter when Carrier Frequency is 6 kHz and Duty Frequency is 50 Hz

When comparing Figure 53 (without harmonic filter) and Figure 54 (with harmonic filter), it was seen that the harmonic filter again removed the ringing and transients. Therefore, the harmonic filter does actually work to produce a cleaner current input waveform to the VFD and should always be used in tandem with VFDs.

4.5 Recommendations for Minimisation of Earth Leakage Current

From the results gained in the investigation, the following recommendations were produced to provide ways of minimising spurious earth leakage current and protecting other upstream equipment:

1. Use VFD rated cable to connect the VFD to the motor

Cables which are VFD rated will maintain a heavy industrial grade XLPE insulation which provides less capacitance and more stable electrical performance. The smaller capacitance value will decrease the magnitude of the capacitive earth leakage currents and therefore allows for a longer cable length in between the VFD and motor.

2. Avoid running at small duty frequencies and high carrier frequencies

A small duty frequency and high carrier frequency significantly increases the magnitude of the earth leakage currents. However, low carrier frequencies offer poorer resolution VFD output waveforms, so it is recommended that a moderate carrier frequency such as 6 kHz is used as a trade-off. Furthermore, it is recommended that other techniques, such as a gearbox, be used if motor speed is to be reduced to considerably small levels.

3. Minimise the length of the cable in between the motor and the VFD

A longer cable in between the motor and VFD will maintain a higher capacitance value in between the active and earth conductors. This higher capacitance value will increase the magnitude of the earth leakage currents.

CHAPTER FIVE

5 CONCLUSIONS AND FUTURE WORK

5.1 Summary

This thesis project maintained an industry supervisor from Orana Engineering called Dr Graham Woods and was performed in tandem with another university student named David Giardina. The aim of this thesis was to prove that the current circuit model could produce circuit characteristics with similar trends to that produced in typical industry VFD environments. To do this, a practical hardware simulation of a typical industry VFD – motor environment was constructed and used to test the accuracy of the existing VFD circuit model. The investigation also required making recommendations on how to improve the circuit model and determining which industry conditions could lead to problematic earth leakage levels.

To construct the practical environment, Orana Engineering provided a 6 kW squirrel cage motor, a rheostat to act as a fault resistance from one of the phases to ground, a current clamp and 100 m of VFD rated cable. Furthermore, CSE Uniserve donated a VFD and harmonic filter with the premise that all results and reports be submitted to them at the completion of the project.

It was decided that four nodes in the practical environment would be tested throughout the investigation. These nodes included the input harmonic filter node, the input VFD node, the output VFD motor and the earth conductor node. Furthermore, each of these nodes were tested with carrier frequencies of 2 kHz, 6 kHz and 15 kHz and duty frequencies of 10 Hz, 30 Hz and 50 Hz. This was done to see if the circuit model would remain accurate for a variety of duty and carrier frequencies. Moreover, the practical environment was tested with phase to earth fault resistances of $3.375\text{ k}\Omega$ and $761\text{ }\Omega$ to see if the model would produce accurate results under fault conditions. Lastly, the cable length in between the motor and VFD was varied from 10 m to 50m to establish the effects of having a longer cable in between motor and VFD. These tests were then performed in MicroCAP using the VFD circuit model.

To minimise project cost, it was decided to make a single test set-up which required no further electrical work to be conducted in between tests. Although, this would make the initial set-up more expensive, it was deemed cheaper than increasing electrical contractor labour time. The environment was designed with shrouded test points at each node to test the voltage and enough space to fit the cable clamp in to measure current. A voltage divider circuit was created so that a university Picoscope, with a maximum voltage of 20 V, could be used to record the node voltage waveforms. To model the cable lengths in the cable

capacitance test, two extension cables were created at 10 m and 50 m using 3-phase plugs and sockets. Also, to test the effects of the harmonic filter on the circuit, a 6-pole bypass switch was used to isolate the harmonic filter when needed. Also, the rheostat was connected from phase to earth at the motor terminals so that a fault could be simulated.

When viewing the output VFD node voltage and current responses, it was seen that the circuit model response was similar but always maintained significantly more oscillatory ringing behaviour and had considerably sized transients when compared to the test environment response. This was put down to the fact that the circuit model motor load did not include motor inductances, which would have the effect of filtering out some of the ringing. Also, it was deduced that the practical VFD internal circuitry must contain methods of limiting the oscillatory ringing behaviour which had not been encompassed in the circuit model. It was decided that the circuit model produced output VFD node voltage waveforms similar in shape to the test environment waveforms but produced unreliable output VFD node current representations (due to amount of oscillatory behaviour).

Furthermore, when viewing the earth conductor current responses, it was seen that the test and model responses were similar, though the actual measured values possessed more oscillatory and transient behaviour than the circuit model response. This discrepancy was put down to the fact that the circuit model did not account for the practical stray reactances which would be prevalent and would cause more oscillatory ringing. Therefore, it was deduced that the circuit model did approximate earth conductor waveforms both with and without the presence of a fault to ground.

Initially, it was found that the circuit model did not accurately model changes in cable length in between the motor and VFD. The circuit model cable capacitances values were then changed from a generic value to the actual VFD rated cable capacitances, which was measured with a capacitance meter. This resulted in the circuit model giving surprisingly accurate earth conductor current representations when the cable length was changed.

The test environment waveforms were then viewed to determine the effect of changing duty frequency. When viewing the output VFD node voltage waveforms, it was seen that a lower duty frequency resulted in a constant small PWM pulse width. However, a higher duty frequency resulted in larger variable pulse widths. This was put down to the fact that to keep the voltage/frequency ratio constant (to maximise torque and maintain the V/F ratio), the voltage of the smaller duty frequency waveform had to be decreased (which means smaller width pulses in PWM). It was found that lower duty frequencies resulted in greater earth leakage current issues as the larger number of rapid changes in voltages (unlike with higher duty frequencies where there are larger pulse widths) would cause higher capacitive leakage

currents ($I = C \cdot dv/dt$). Moreover, when viewing the output VFD node current waveforms, a theory was deduced that suggested a correlation between larger width pulses and less frequent pulses in the voltage waveform causing more significant ringing effects in the current waveforms. However, this theory is yet to be proved.

When viewing the output VFD node voltage waveforms, it was then seen that increasing the carrier frequency decreased the period of the switching and therefore added more PWM pulses to increase the resolution of the effective sinusoidal representation. It was seen that the more rapid switching caused higher capacitance currents as $I = C \cdot dv/dt$. Therefore, it was surmised that a low duty frequency and high carrier frequency would typically result in more sizeable earth leakage currents.

Lastly, it was seen that the harmonic filter does actually work to produce a cleaner voltage and current input waveform to the VFD and should always be used in tandem with VFDs.

In conclusion, the thesis was considered a success. It proved that the circuit model could simulate the characteristic trends of all important circuit nodes, though some responses were not accurate due to the model not taking into account all reactance effects. More importantly, it was proved that the circuit model was surprisingly accurate in modelling earth conductor currents. Lastly, it was deduced that the circuit model could definitely be used for the purposes of investigative troubleshooting or providing clients with estimated conditions that could cause earth leakage current issues.

5.2 Future Work

The following aspects of the circuit model shown in Figure 55 of Appendix 7.3 should be improved in future tests to better represent an accurate VFD/motor situation:

- The delta motor model
- Accuracy of cable resistance, inductance and capacitance values
- VFD circuitry which is used to reduce the ringing in the output waveforms

The delta motor model is highly simplistic (only maintaining resistors) and specifically does not accurately represent the inductance of the motor windings. A poorly modelled load could have severely impacted on the accuracy of the output waveforms from the VFD. Furthermore, provisions should be made in future investigations to find out specifically what circuitry is used in VFDs to reduce the ringing in the output waveform which was evident in each circuit model waveform but not evident in the experimental responses.

Also, only three factors were tested during this investigation. Subsequent investigations should investigate other conditions such as earthing types, other circuit capacitances and the usage of different types of earth leakage protection devices.

CHAPTER SIX

6 REFERENCES

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CHAPTER SEVEN

7 APPENDIX

7.1 Risk Assessment



Townsville Campus
 Townsville Qld 4811 Australia
School of Engineering & Physical Sciences

Risk Assessment

Name of Test:	Investigating Operational Characteristics of a VFD		
Purpose: Thesis			
Operator: David Giardina & Matthew Priestley	Duration: 1 week		
SDS Attached: (Tick one)	Yes	No	N/A
Major Hazard Types: (Tick at least one)			
Chemical		Mechanical	
Electrical		Thermal	
Environmental		Other:	

SUMMARY OF RISKS

Specific Task/Activity	Potential Hazards/Consequences	Assessed Risk	Risk Control Measures	Reassessed Risk
Motor/Generator in operation	Electrocution	High	Enclose all exposed live parts De-energise before making circuit changes Emergency stop Safety observer Appropriate LV PPE Have qualified electrical engineer present for any circuit changes	Medium
Motor/Generator in operation	Caught in rotating shaft	Medium	Mount shroud on motor	Low
Motor/Generator in operation	Noise	Medium	Appropriate PPE Conduct tests with environment free of other personnel	Low
Handling of jiffy box	Burns	Medium	Mount heat sink on box Frequent cooling periods Handle box with gloves	Low
Heavy lifting	Back sprains/strains	Medium	2 man lift Mechanical means eg. crane	Low
Use of test equipment	Electrocution	High	Appropriate training received Enclose all exposed live parts	Medium

SUMMARY OF REQUIREMENTS

Personal Protective Equipment	Ear plugs, long sleeve shirt, long pants, steel-toe boots, safety glasses <i>safety gloves oo</i>
Is Training Required	Yes/No
If YES, please state requirements	Lab induction on how to safely use equipment
Training Manual Location	Induction is verbal Methodology for tests is included on risk assessment VFD manual located in high voltage lab

SUMMARY OF ACTIVITY

Pre-Test:

- Elect safety observer to sit next to bench with emergency stop button
- Energise circuit at main switch
- Wearing LV gloves, open enclosure door and switch VFD into RUN mode
- Inspect circuit for any arcing or sparking

Test #1 (Recording Voltage)

- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Plug voltage recorder circuit into appropriate node test point
- Connect picoscope leads to voltage recorder (via banana plugs)
- Close enclosure door and ensure that all personnel are at a safe distance away from motor and enclosure
- Energise circuit at main switch
- Inspect circuit for any arcing or sparking
- Start pico-scope recording
- Wearing LV gloves, open enclosure door and switch VFD into RUN mode
- Stop pico-scope recording at steady state
- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Remove voltage recorder circuit

Test #1 (Recording Current)

- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Clamp around appropriate phase
- Close enclosure door and ensure that all personnel are at a safe distance away from motor and enclosure
- Energise circuit at main switch
- Inspect circuit for any arcing or sparking
- Start pico-scope recording
- Wearing LV gloves, open enclosure door and switch VFD into RUN mode
- Stop pico-scope recording at steady state
- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Remove current clamp

Test #1 (Adjusting VFD Settings)

- Energise circuit at main switch
- Wearing LV gloves, open enclosure door and switch VFD into STOP mode
- Press [PRG] → [Data Setting] → [FUNC/DATA]
- Enter function code F26 and enter appropriate carrier frequency
- Press [FUNC/DATA]
- Wearing LV gloves, open enclosure door and switch VFD into RUN mode
- Use the [^ / v] arrow buttons to adjust duty frequency
- Press [FUNC/DATA]

Test #2 (Changing Resistance Fault to Ground)

- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Close rheostat circuit using banana plug lead and turn switch on
- Adjust rheostat to appropriate resistance and verify with multimeter
- Record exact resistance

Test #2 (Remove Fault to Ground)

- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Open rheostat circuit using banana plug lead and turn switch off

Test #3 (Change Cable Length)

- De-energise circuit at main switch
- Test for dead at nodes using multimeter and wearing LV gloves
- Change cables over (plug and play)

ASSESSMENT:

OPERATOR (Student or Technician):

David Giardina

Name



Date: 5/8/13 Contact No: 0415822409

Signature

OPERATOR (Student or Technician):

Matthew Priestley

Name



Date: 5/8/13 Contact No: 0438184647

Signature

QUALIFIED ELECTRICAL ENGINEER:

Name

Signature

Date: / / Contact No: _____

QUALIFIED ELECTRICAL ENGINEER:

Graham Woods
Name


Signature

Date: 7/8/13 Contact No: 0409698170

SUPERVISOR:

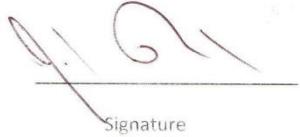
Mihay
Name


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Date: 05/08/13 Contact No: 14379.

SAFETY ADVISOR:

John Renehan
Name


Signature

Date: 05/08/13 Contact No: 14459

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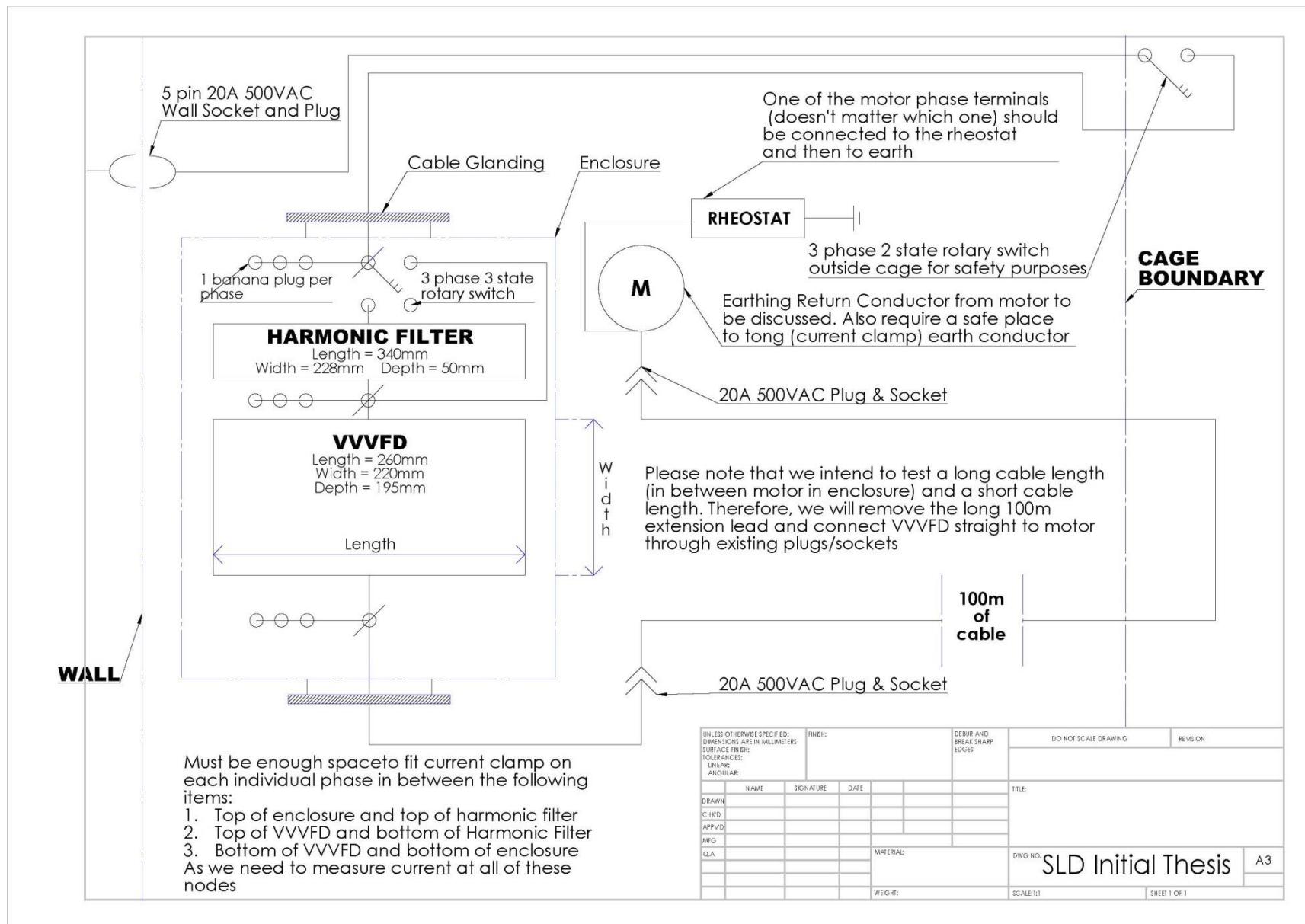
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THIS FORM IS TO BE DISPLAYED IN THE IMMEDIATE VICINITY OF THE EXPERIMENT BEING UNDERTAKEN

7.2 Experimental Set-up SLD



7.3 Current VFD Circuit Model

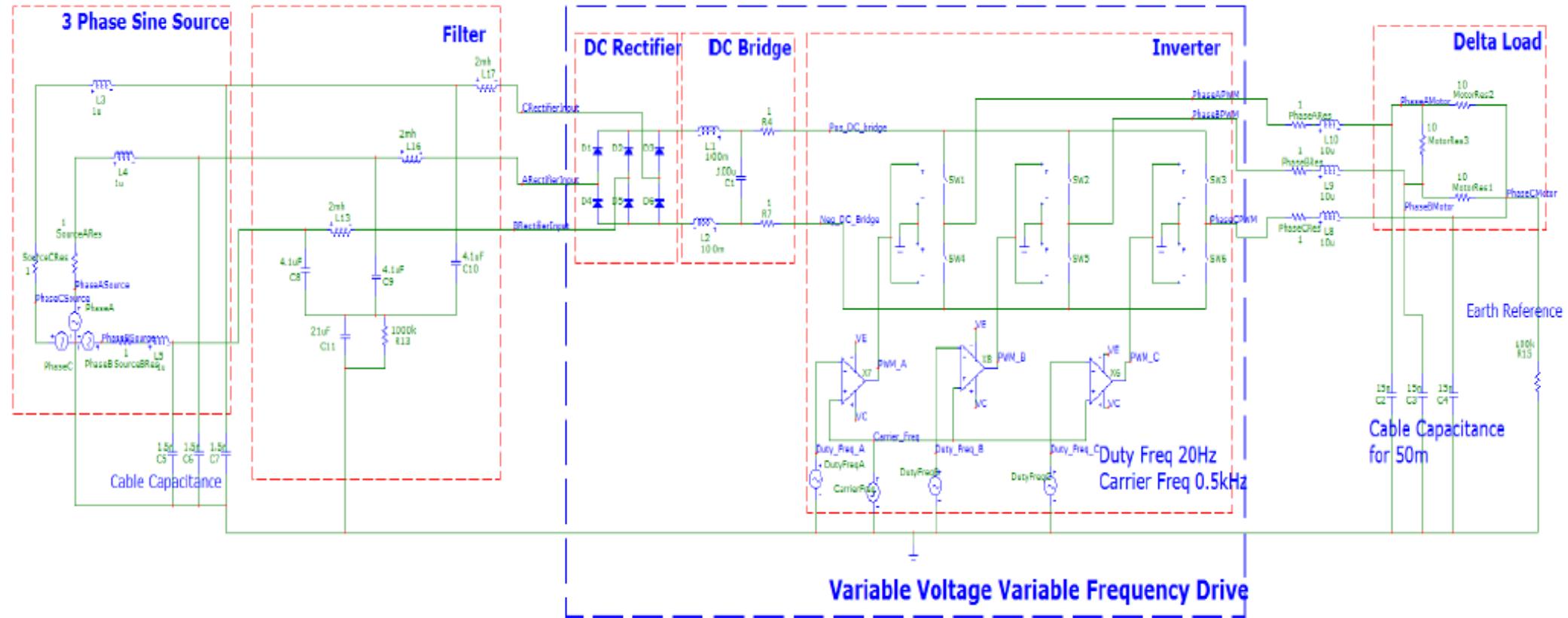


Figure 55 - Circuit Model of a VFD circuit