Lab 5 – Multipliers

CS1050 Computer Organization and Digital Design

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Index No. : **220135N**

Group : **44**

Lab Task: Implementation of Multipliers for 2-bit and 4-bit Binary Numbers

This lab focuses on the practical implementation and testing of multipliers designed for binary numbers, specifically targeting two scenarios: a 2-bit multiplier and a 4-bit multiplier. Multipliers are essential components in digital circuitry, enabling the efficient multiplication of binary numbers in electronic systems.

The 2-bit multiplier is realized through the use of two Full Adders (FAs). Full Adders are fundamental units in digital circuit design, facilitating binary addition with carry inputs. By chaining two FAs together, we create a concise yet effective circuit for multiplying 2-bit binary numbers.

To accommodate the multiplication of two 4-bit binary numbers, a more intricate circuit is employed, featuring twelve Full Adders. This design allows for the handling of carry bits, ensuring precise multiplication results for a broader range of input values.

Both implementations encompass the standard design steps, including the development of circuit diagrams and simulation of the designed circuits. These steps are integral in confirming the accuracy and efficiency of the multiplier designs.

1) 2x2 Multiplier

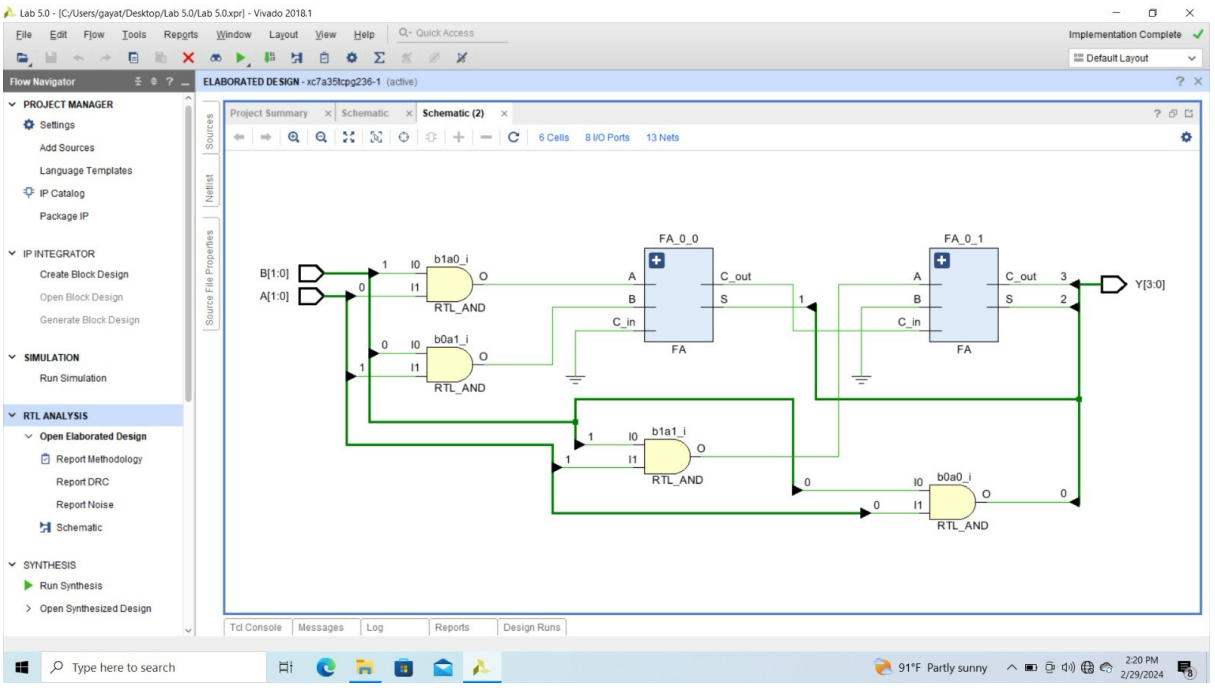
Design source file

```
----------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 02:12:22 PM
-- Design Name:
-- Module Name: Multiplier 2 - Behavioral
-- Project Name:
-- Target Devices:
```

```
-- Tool Versions:
-- Description:
-- --
Dependencies:
-- --
Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- ----------------------------------------------------------
----



library IEEE; use
IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiati -- any Xilinx leaf cells in this code.
--library UNISIM; --use
UNISIM.VComponents.all;

entity Multiplier_2 is
Port (
A : in STD_LOGIC_VECTOR (1 downto 0);
B : in STD_LOGIC_VECTOR (1 downto 0);
Y : out STD_LOGIC_VECTOR (3 downto 0));
end Multiplier_2;
architecture Behavioral of Multiplier_2 is

COMPONENT FA
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);
```

```
END COMPONENT;

signal b0a0, b0a1, b1a1, b1a0 : STD_LOGIC;
signal S_0_0, S_0_1, C_0_0, C_0_1 : STD_LOGIC;


begin

FA_0_0 : FA
Port map(
    A => b1a0,
    B => b0a1,
    C_in => '0',
    S => S_0_0,
    C_out  => C_0_0);

FA_0_1 : FA
    Port map(
        A => b1a1,
        B => '0',
        C_in => C_0_0,
        S => S_0_1,
        C_out  => C_0_1);

b0a0 <= B(0) and A(0);
b0a1 <= B(0) and A(1);
b1a0 <= B(1) and A(0);
b1a1 <= B(1) and A(1);

Y(0) <= b0a0;
Y(1) <= S_0_0;
Y(2) <= S_0_1;
Y(3) <= C_0_1;


end Behavioral;
```

Elaborated design schematic



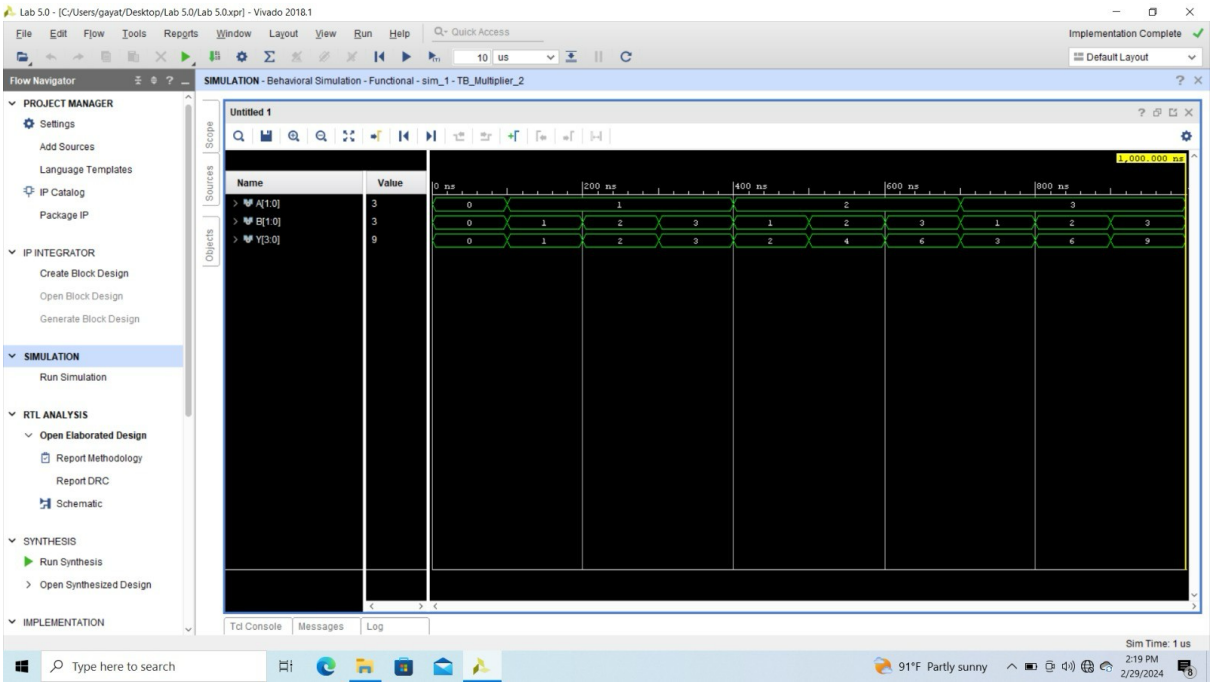
Simulation source file

```
----------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 02:41:51 PM
-- Design Name:
-- Module Name: TB_Multiplier_2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
```

```
-- Revision 0.01 - File Created
-- Additional Comments:
-- ----------------------------------------------------------
----


library IEEE; use
IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiati -- any Xilinx leaf cells in this code.
--library UNISIM; --use
UNISIM.VComponents.all;

entity TB_Multiplier_2
is --  Port ( ); end
TB_Multiplier_2;

architecture Behavioral of TB_Multiplier_2 is

COMPONENT Multiplier_2
        Port ( A : in STD_LOGIC_VECTOR (1 downto 0);
               B : in STD_LOGIC_VECTOR (1 downto 0);
               Y : out STD_LOGIC_VECTOR (3 downto 0));

END COMPONENT;

signal A, B : STD_LOGIC_VECTOR (1 downto 0);
signal Y : STD_LOGIC_VECTOR(3 downto 0);

begin UUT: Multiplier_2 PORT MAP(A,B,Y);

process
```

```
begin

        A<= "00";
        B <="00";

        WAIT FOR 100 ns;
        A<="01";
        B<="01";

        WAIT FOR 100 ns;
        B<="10";
        WAIT FOR 100 ns;
        B<="11";

        WAIT FOR 100 ns;
        A<="10";
        B<="01";

        WAIT FOR 100 ns;
        B<="10";
        WAIT FOR 100 ns;
        B<="11";
        WAIT FOR 100 ns;
        A<="11";
        B<="01";
        WAIT FOR 100 ns;
        B<="10";
        WAIT FOR 100 ns;
        B<="11";
        WAIT;

end process;
end Behavioral;
```

Timing diagram



2) 4x4 Multiplier

Design source file

```
----------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/27/2024 03:06:16 PM
-- Design Name:
-- Module Name: Multiplier_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments :
```

```
-- ----------------------------------------------------------------
---



library IEEE; use
IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiati
-- any Xilinx leaf cells in this code.
--library UNISIM; --use
UNISIM.VComponents.all;

entity Multiplier_4 is     Port ( A : in
STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC_VECTOR (7 downto 0)); end
Multiplier_4;

architecture Behavioral of Multiplier_4 is

COMPONENT FA
    Port ( A : in STD_LOGIC;
           B : in STD_LOGIC;
           C_in : in STD_LOGIC;
           S : out STD_LOGIC;
           C_out : out STD_LOGIC);

END COMPONENT;

signal b0a0, b0a1, b0a2, b0a3,b1a0, b1a1, b1a2, b1a3, b2a0, b2a1, b2a2, b2a3,
       b3a0,b3a1, b3a2, b3a3 : STD_LOGIC;
signal S_0_0, S_0_1,S_0_2, S_0_3,S_1_0, S_1_1,S_1_2, S_1_3,S_2_0, S_2_1,S_2_2,
      S_2_3,C_0_0, C_0_1,C_0_2, C_0_3,C_1_0, C_1_1,C_1_2, C_1_3,C_2_0, C_2_1,C_2_2,
      C_2_3: STD_LOGIC;

begin
```

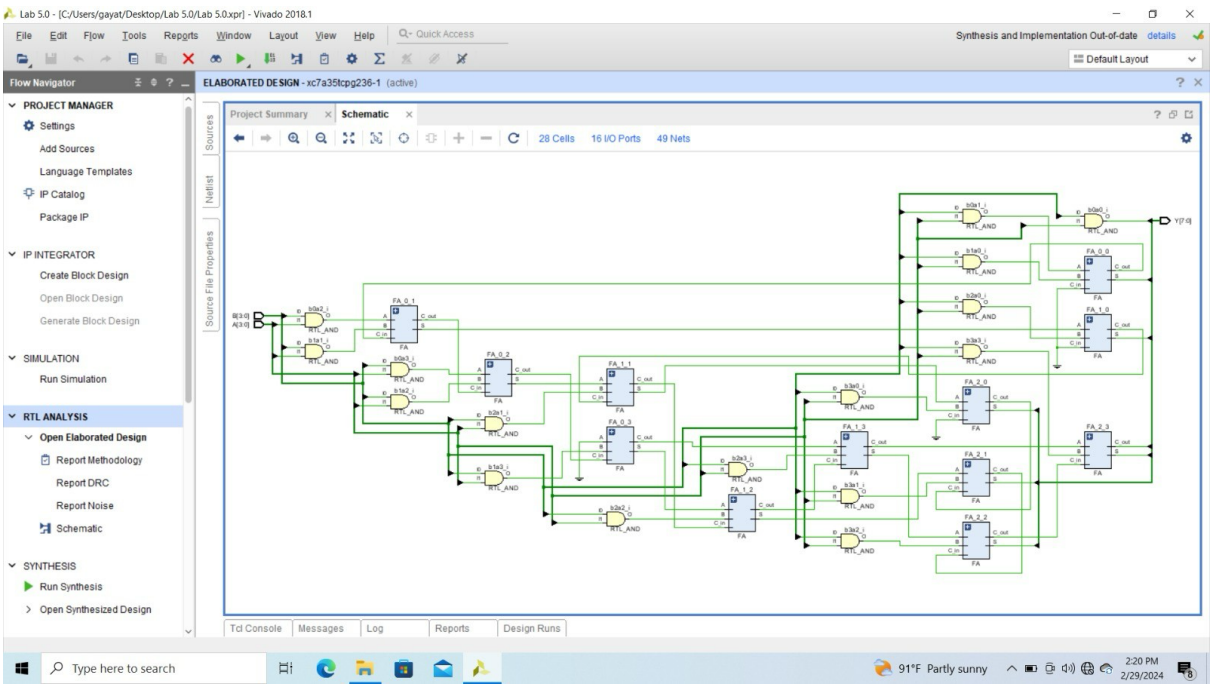
```
FA_0_0 : FA
Port map(
A => b0a1,
B => b1a0,
C_in => '0',
S => S_0_0,
C_out  => C_0_0);

FA_0_1 : FA
    Port map(
A => b0a2,
B => b1a1,
C_in => C_0_0,
S => S_0_1,
C_out  => C_0_1);

FA_0_2 : FA
        Port map(
A => b0a3,
B => b1a2,
C_in => C_0_1,
S => S_0_2,
C_out  => C_0_2);

FA_0_3 : FA
    Port map(
A => '0',
B => b1a3,
C_in => C_0_2,
S => S_0_3,
C_out  => C_0_3);

FA_1_0 : FA
        Port map(
A => S_0_1,
B => b2a0,
C_in => '0',
S => S_1_0,
```

```
C_out  => C_1_0);

FA_1_1 : FA
    Port map(
A => S_0_2,
B => b2a1,
C_in => C_1_0,
S => S_1_1,
C_out  => C_1_1);

FA_1_2 : FA
        Port map(
A => S_0_3,
B => b2a2,
C_in => C_1_1,
S => S_1_2,
C_out  => C_1_2);

FA_1_3 : FA
    Port map(
A => c_0_3,
B => b2a3,
C_in => C_1_2,
S => S_1_3,
C_out  => C_1_3);

FA_2_0 : FA
        Port map(
A => S_1_1,
B => b3a0,
C_in => '0',
S => S_2_0,
C_out  => C_2_0);

FA_2_1 : FA
    Port map(
A => S_1_2,
B => b3a1,
```

```
C_in => C_2_0,
S => S_2_1,
C_out  => C_2_1);

FA_2_2 : FA
        Port map(
A => S_1_3,
B => b3a2,
C_in => C_2_1,
S => S_2_2,
C_out  => C_2_2);

FA_2_3 : FA
    Port map(
A => c_1_3,
B => b3a3,
C_in => C_2_2,
S => S_2_3,
C_out  => C_2_3);


b0a0 <= B(0) and A(0);
b0a1 <= B(0) and A(1);
b0a2 <= B(0) and A(2);
b0a3 <= B(0) and A(3);
b1a0 <= B(1) and A(0);
b1a1 <= B(1) and A(1);
b1a2 <= B(1) and A(2);
b1a3 <= B(1) and A(3);
b2a0 <= B(2) and A(0);
b2a1 <= B(2) and A(1);
b2a2 <= B(2) and A(2);
b2a3 <= B(2) and A(3);
b3a0 <= B(3) and A(0);
b3a1 <= B(3) and A(1);
b3a2 <= B(3) and A(2);
b3a3 <= B(3) and A(3);
```

```
Y(0) <= b0a0;
Y(1) <= S_0_0;
Y(2) <= S_1_0;
Y(3) <= S_2_0;
Y(4) <= S_2_1;
Y(5) <= S_2_2;
Y(6) <= S_2_3;
Y(7) <= C_2_3;

end Behavioral;
```

Elaborated design schematic



Simulation source file

```
----------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/28/2024 04:33:35 PM
```

```
-- Design Name:
-- Module Name: TB_Multiplier_4 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
-- --
Dependencies:
-- --
Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
-- ----------------------------------------------------------
----


library IEEE; use
IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
instantiati -- any Xilinx leaf cells in this code.
--library UNISIM; --use
UNISIM.VComponents.all;

entity TB_Multiplier_4
is --  Port ( ); end
TB_Multiplier_4;

architecture Behavioral of TB_Multiplier_4 is
COMPONENT Multiplier_4
        Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
               B : in STD_LOGIC_VECTOR (3 downto 0);
               Y : out STD_LOGIC_VECTOR (7 downto 0));
```

```
END COMPONENT;

signal A, B : STD_LOGIC_VECTOR (3 downto 0);
signal Y : STD_LOGIC_VECTOR(7 downto 0);

begin
    UUT: Multiplier_4 PORT MAP(A, B, Y);

process
begin

    A <= "0111";
    B <= "1110";
    WAIT FOR 100 ns;
    A<= "1011";
    B <="0101";

    WAIT FOR 100 ns;
    A<="1101";
    B<="0110";

    WAIT FOR 100 ns;
    A<="1111";
    B<="1001";
    WAIT FOR 100 ns;
    A<="0011";
    B<="1111";
    WAIT FOR 100 ns;
    A<= "1101";
    B <="1010";
    WAIT;

end process;

end Behavioral;
```

Timing diagram