CS1050 - Computer Organization and Digital Design

Department of Computer Science and Engineering - University of Moratuwa

Multipliers

Learning Outcomes:

In this lab exercise, you will implement

- A multiplier which multiplies two 2-bit binary numbers.
- A multiplier which multiplies two 4-bit binary numbers.

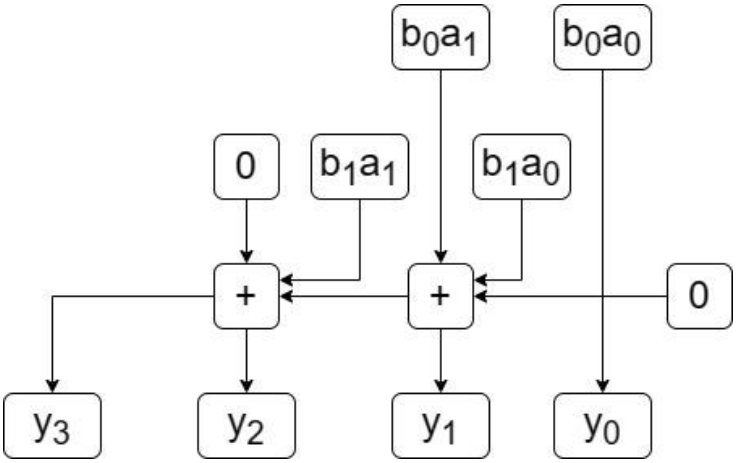
Consider the multiplication of two 2-bit numbers: a_1a_0 and b_1b_0:

		b_1	b_0
		a_1	a_0
	---	---	---
	c_1	b_1a_0	b_0a_0
	b_1a_1	b_0a_1	
	---	---	---
c_2	s_2	s_1	b_0a_0

Where

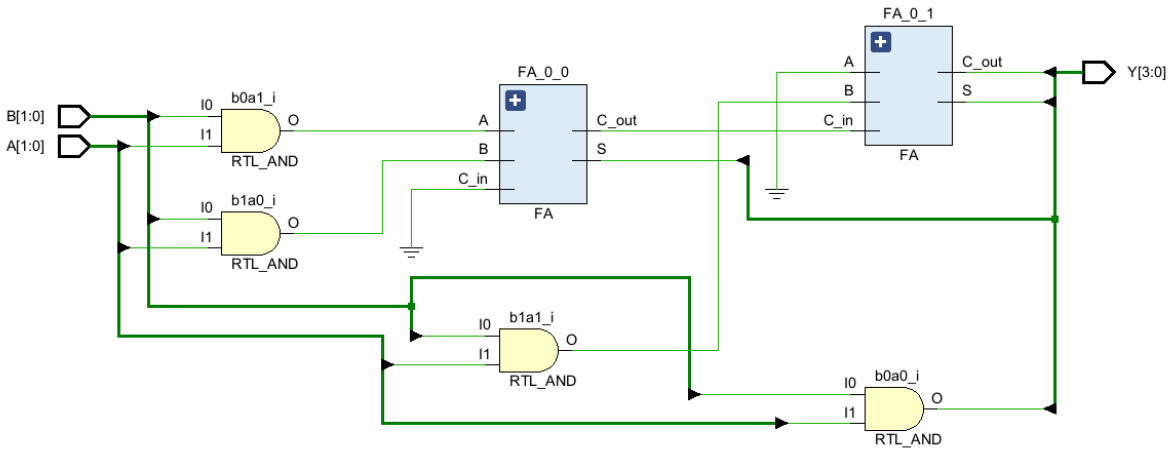
- c_1 - carry of $b_1a_0 + b_0a_1$
- s_1 - sum of $b_1a_0 + b_0a_1$
- c_2 - carry of $c_1 + b_1a_1$
- s_2 - sum of $c_1 + b_1a_1$

We can use this approach to build a multiplier combinational circuit.



Exercises:

- Build a 2x2 multiplier circuit.
  After successfully building the 2x2 multiplier, your elaborated design diagram will look like this:



- Build a 4x4 multiplier circuit.

Naming convention:

Use the following entity declaration for the full adder circuit:

```
entity FA is
    Port (
        A : in std_logic;
        B : in std_logic;
        C_in : in std_logic;
        S : out std_logic;
        C_out : out std_logic
    );
end FA;
```

Use the following entity declaration for the 2x2 multiplier circuit:

```
entity Multiplier_2 is
    Port ( A : in STD_LOGIC_VECTOR (1 downto 0);
           B : in STD_LOGIC_VECTOR (1 downto 0);
           Y : out STD_LOGIC_VECTOR (3 downto 0));
end Multiplier;
```

Use the following entity declaration for the 4x4 multiplier circuit:

```
entity Multiplier_4 is
    Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
           B : in STD_LOGIC_VECTOR (3 downto 0);
           Y : out STD_LOGIC_VECTOR (7 downto 0));
end Multiplier;
```

Name the internal signals as follows

- Multiplication between `B[x]` and `A[x]`: `bxax` (ie. `b0a0`, `b0a1`, etc.)
- i^{th} adder of j^{th} row: `FA_j_i`
- Carry of the i^{th} adder of j^{th} row: `c_j_i`
- Sum of the i^{th} adder of j^{th} row: `s_j_i`

Submission:

Submit a report with the following content

- Introduction
- 2x2 multiplier
    - Design source file
    - Elaborated design schematic
    - Simulation source file
    - Timing diagram
- 4x4 multiplier
    - Design source file
    - Elaborated design schematic
    - Simulation source file
    - Timing diagram

Name your report in the following format:

<Index_no>_Multiplier.pdf

eg:- 210001A_Multiplier.pdf

References

- J. F. Wakerly, “Combinational Multipliers” in *Digital Design - Principles and Practices, 3rd Edition*. Prentice Hall, ch 5.11, pp. 406-407.