

CPU DESIGN

Problem:

Build CPU based on following requirements:

1. Word Size of CPU = 5
2. ALU Operations = XOR, ADD, ROL
3. Register Number = 3
4. Size of RAM = 7
5. Word size of ISA and RAM = 15
6. CPU Instructions = Register Mode, Immediate Mode, JMP, JLE

Solution:

Simulator Design:

1. ALU Circuit (Top to Bottom all circuits):

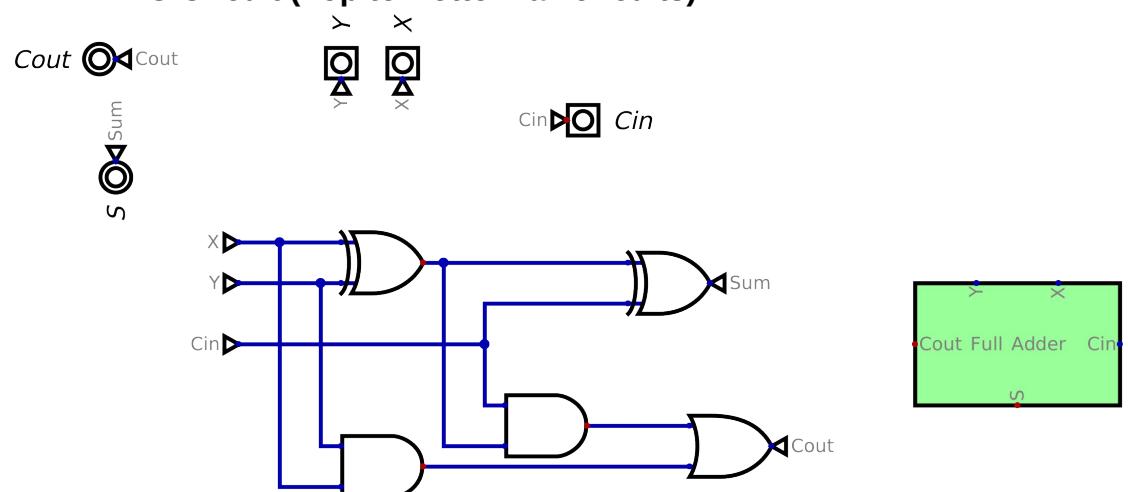


Figure: Full Adder

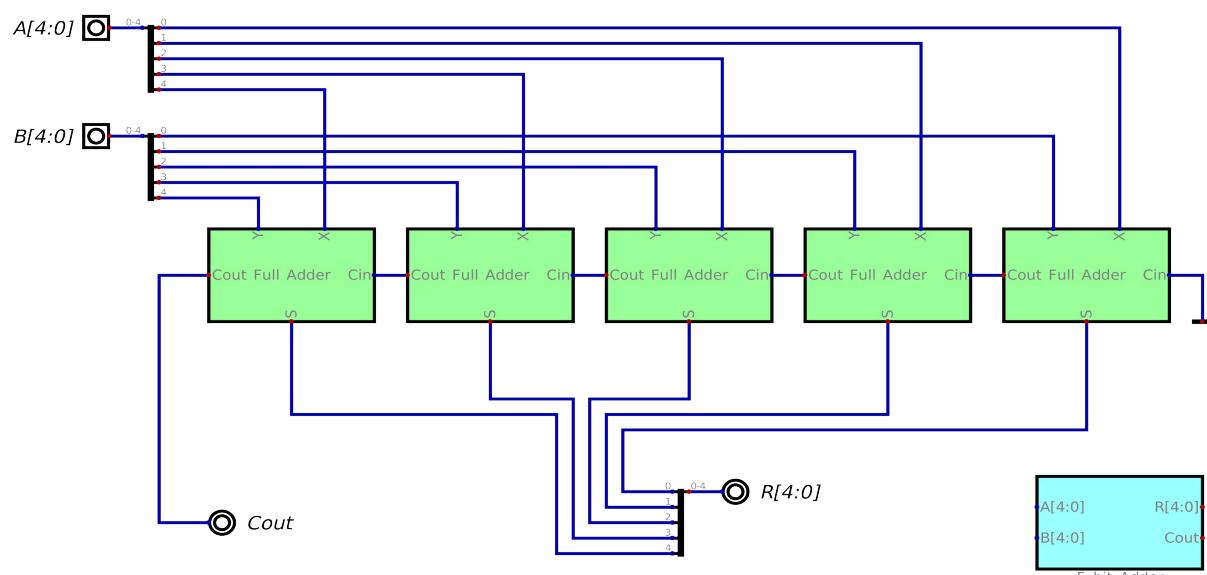


Figure: 5 bit Adder

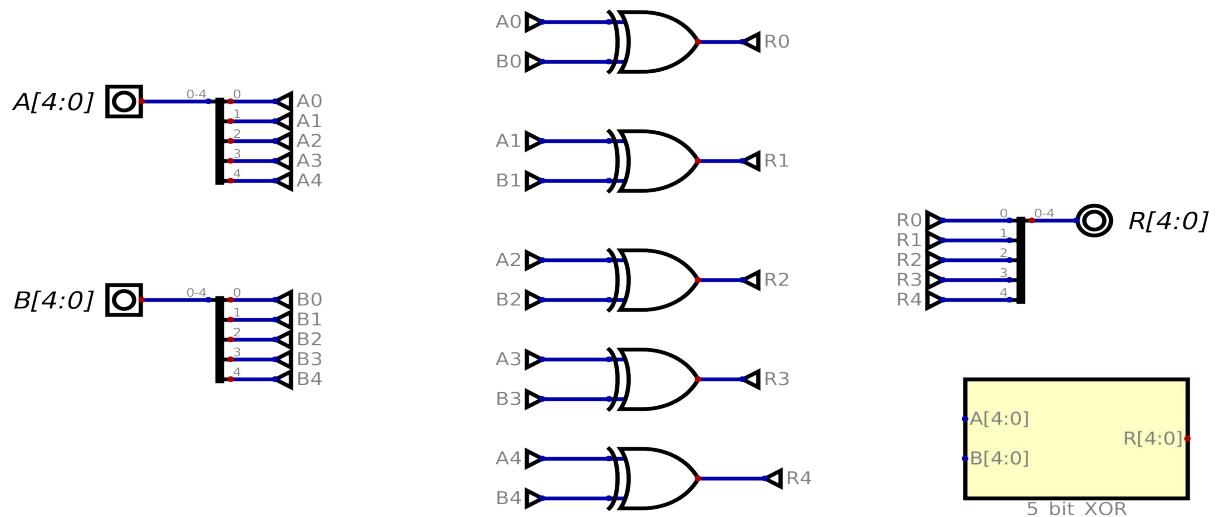


Figure: 5 bit XOR

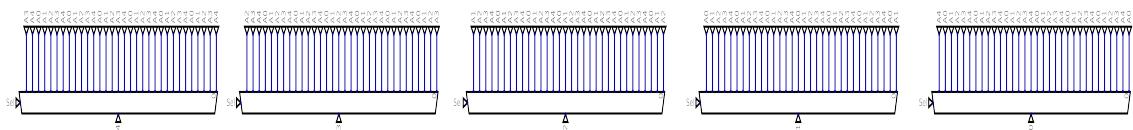
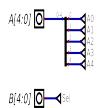


Figure: 5 bit Left Rotator

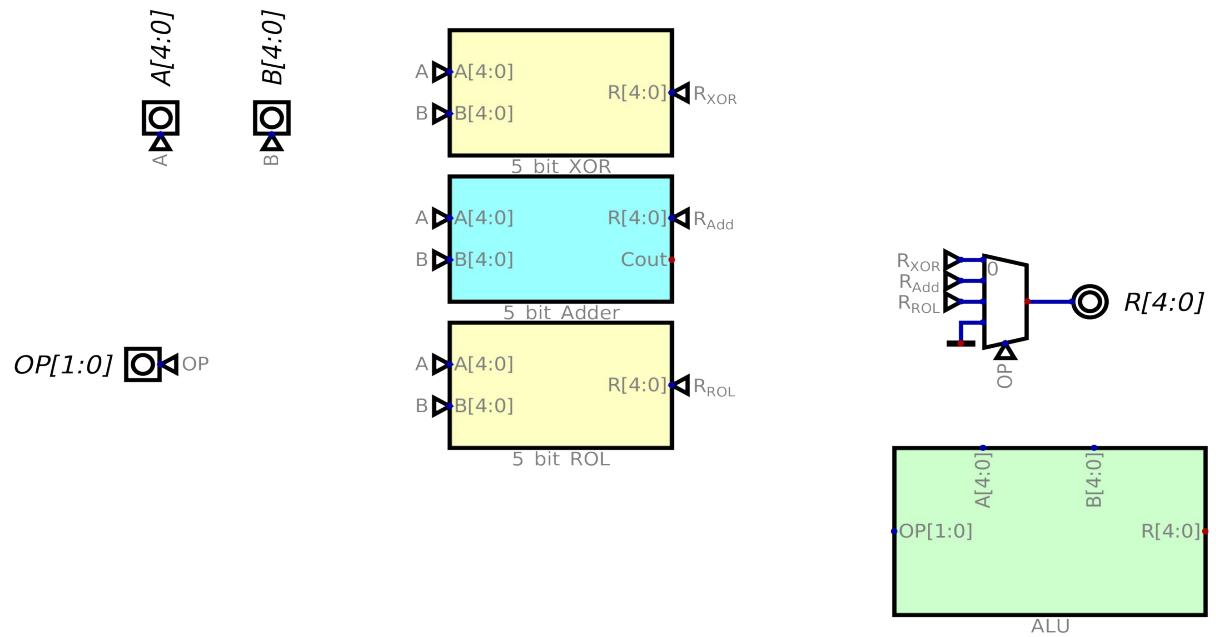


Figure: 5 bit ALU

2. Register Set Circuit (Top to Bottom all circuits):

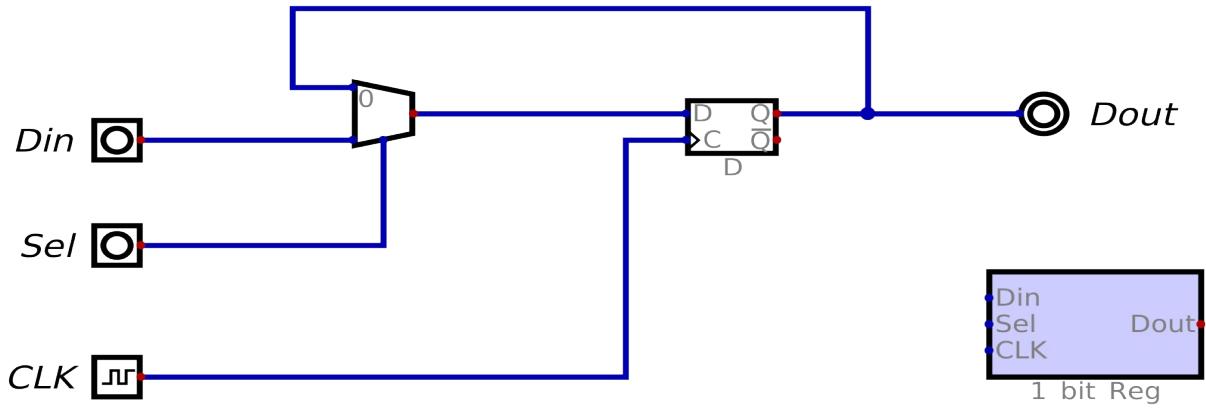


Figure: 1 bit Register

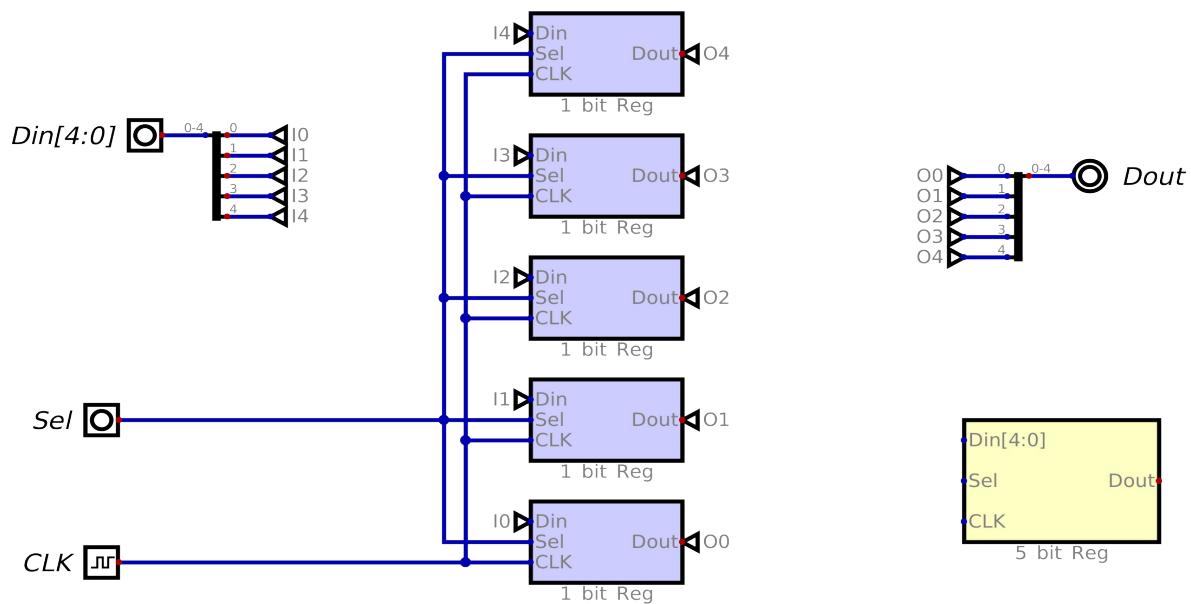


Figure: 5 bit Register

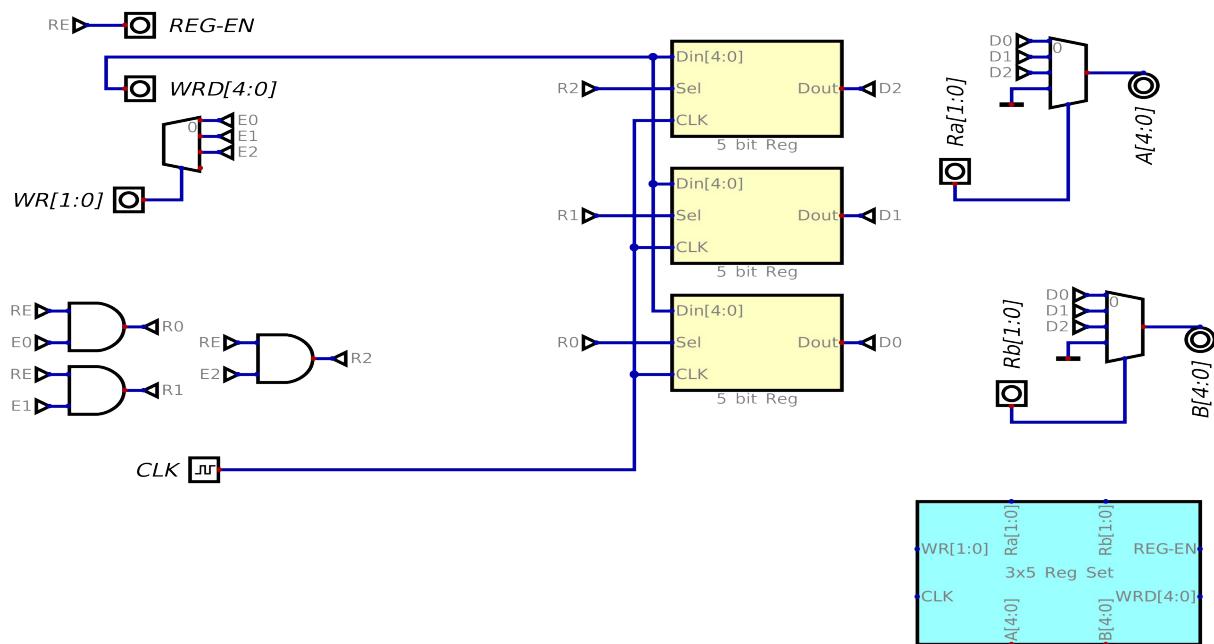


Figure: 3x5 Register Set

3. RAM Circuit (Top to Bottom all circuits):

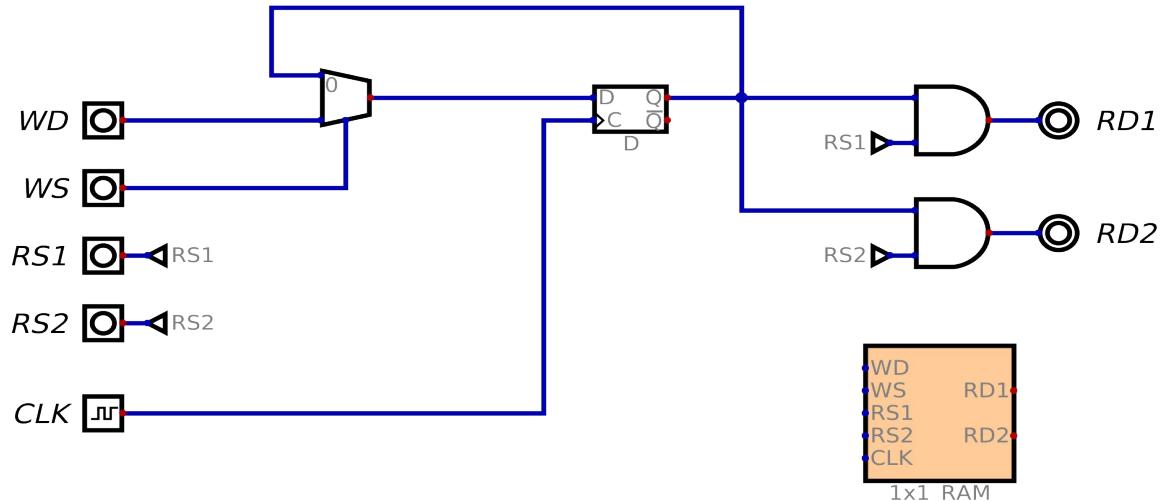


Figure: 1x1 RAM

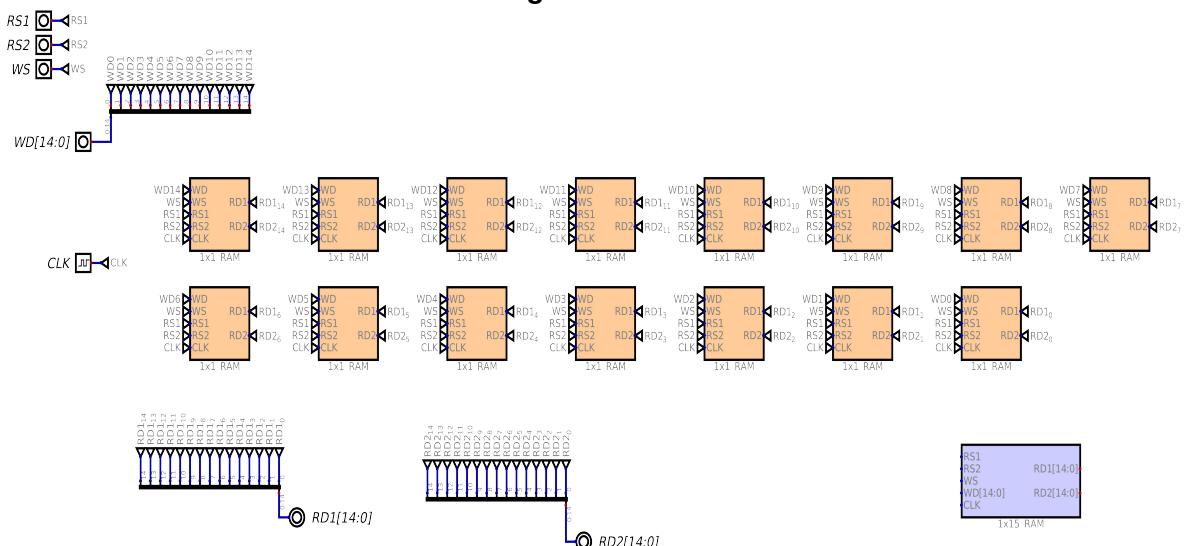


Figure: 1x15 RAM

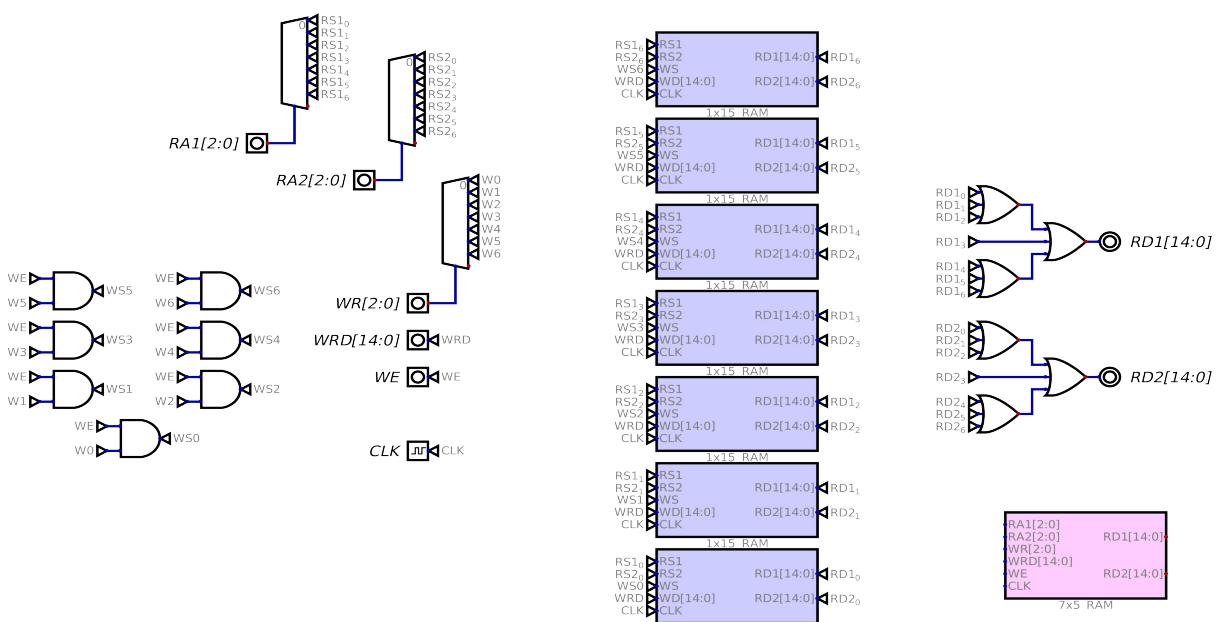


Figure: 7x15 RAM

4. ISA:

ISA of Arithmetic & Logic Instruction (Register Mode):

Opcode (4 bit)		Register 1	Register 2	Unused
2 bits	2 bits	2 bits	2 bits	7 bits
Types of Instruction	Operations (ALU selection lines)	00 - 10 (R0 - R2)	00 - 10 (R0 - R2)	xxxxxx

Opcode		Register 1	Register 2	Unused	Assembly Example
Type (2 bits)	Operations (2 bits)	2 bits	2 bits	7 bits	
00	XOR (00)	00 - 10 (R0 - R2)	00 - 10 (R0 - R2)	xxxxxxxx	XOR R1, R1
	ADD (01)	00 - 10 (R0 - R2)	00 - 10 (R0 - R2)		ADD R1, R2
	ROL (10)	00 - 10 (R0 - R2)	00 - 10 (R0 - R2)		ROL R1, R2

ISA of Arithmetic & Logic Instruction (Immediate Mode):

Opcode (4 bit)		Register 1	Constant	Unused
2 bits	2 bits	2 bits	5 bits	4 bits
Types of Instruction	Operations (ALU selection lines)	00 - 10 (R0 - R2)	00000 - 11111 (0 - 31)	xxxx

Opcode		Register 1	Constant	Unused	Assembly Example
Type (2 bits)	Operations (2 bits)	2 bits	5 bits	4 bits	
01	XOR (00)	00 - 10 (R0 - R2)	00000 - 11111 (0 - 31)	xxxx	XOR R1, 5
	ADD (01)	00 - 10 (R0 - R2)			ADD R1, 6
	ROL (10)	00 - 10 (R0 - R2)			ROL R1, 3

ISA of Branching Mode:

Opcode (4 bit)		Address	Unused
2 bits	2 bits	3 bits	8 bits
Types of Instruction	Operations (ALU selection lines)	000 - 110 (0 - 6)	xxxxxxxx

Opcode		Address	Unused	Assembly Example
Type (2 bits)	Operations (2 bits)	3 bits	8 bits	
10	JMP (00)	000 - 110 (0 - 6)	xxxxxxxx	JMP 5
	JLE (01)	000 - 110 (0 - 6)		JMP 6

5. CPU (Top to Bottom all circuits):

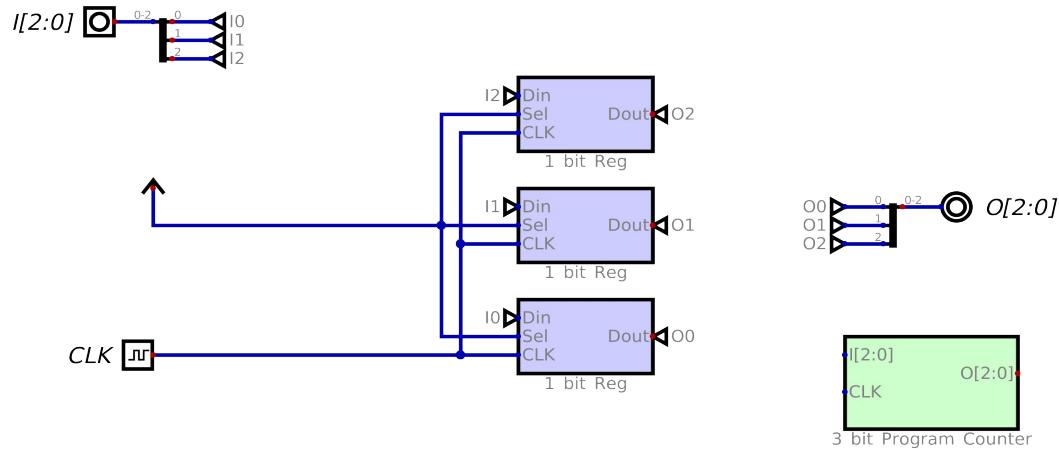


Figure: 3 bit Program Counter

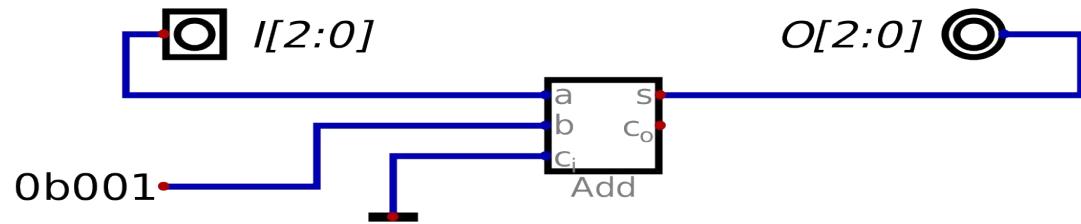


Figure: 3 bit PC Adder

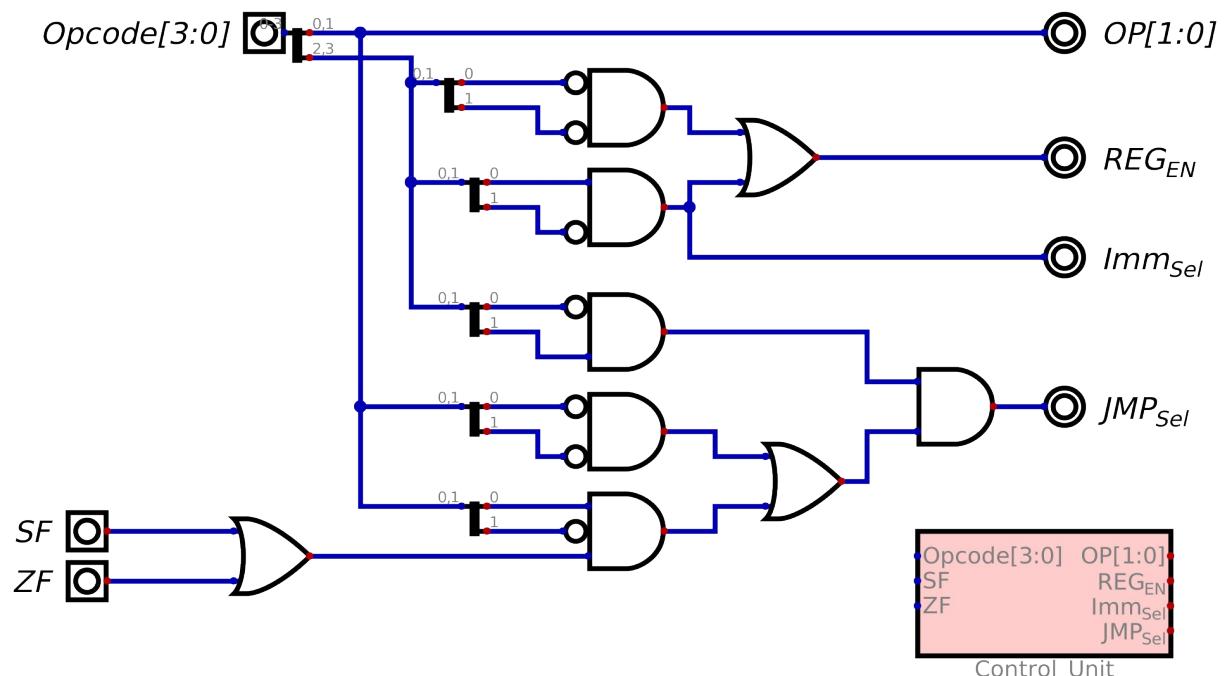


Figure: Control Unit

Register Mode: 2 bit (op type=00) + 2 bit(op) + 2 bit (reg1) + 2 bit (reg2) + 7 bit (x)
 Immediate Mode: 2 bit (op type=01) + 2 bit(op) + 2 bit (reg1) + 5 bit (value) + 4 bit (x)
 Branching Mode: 2 bit (op type=10) + 2 bit(op) + 3 bit (addr) + 8 bit (x)

XOR (op = 00), ADD (op = 01), ROL (op = 10)
 JMP (op = 00), JLE (op = 01)

START:
 XOR R1, R1 --> 0000010100000000
 JLE 0 --> 1001000000000000
 LABEL:
 ADD R1, 2 --> 0101010001000000
 JMP LABEL --> 1000010000000000

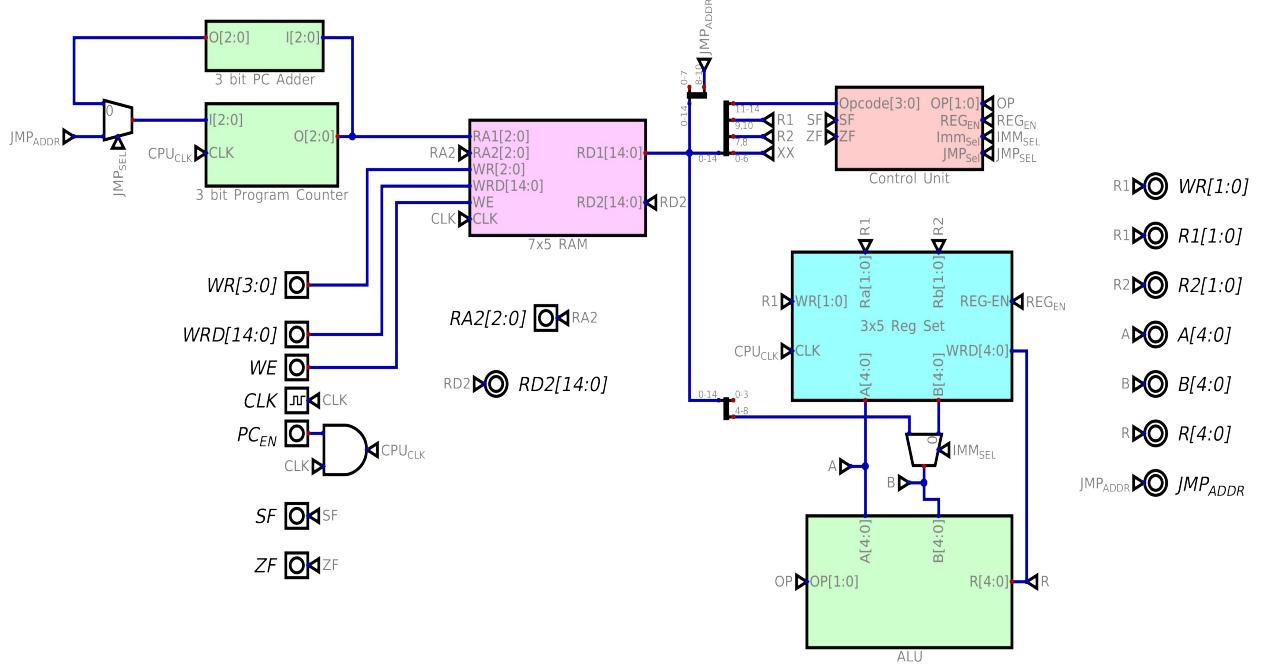


Figure: 5 bit CPU