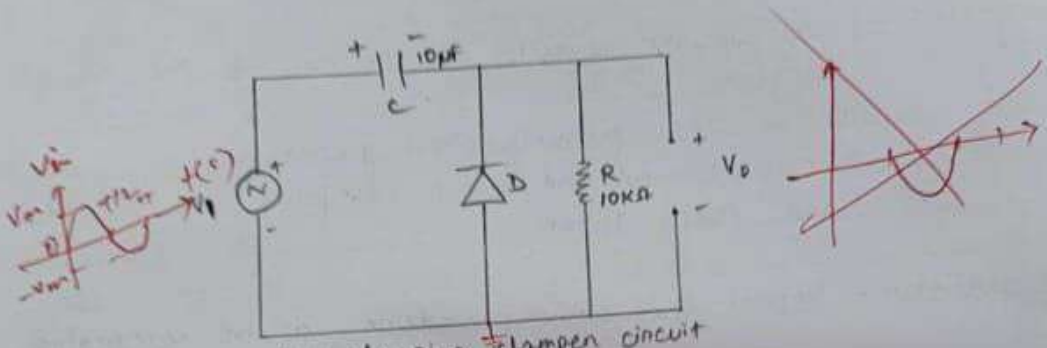
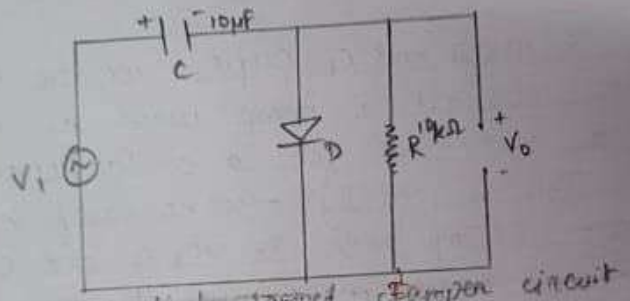
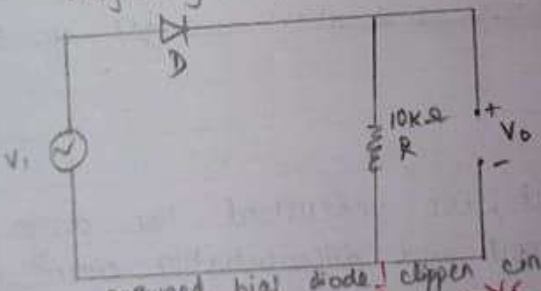


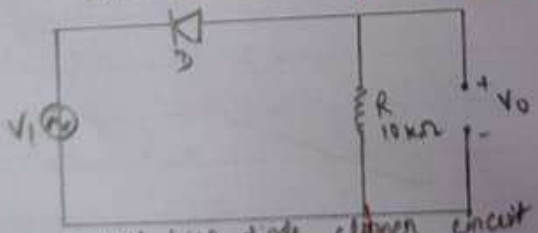
Positive clamping clamper circuit



Negatively clamped clamper circuit



Forward bias diode clipper circuit -ve clipper



Reverse bias diode clipper circuit

+ve clipper

Date .....

Expt. No. .....

Page No. 4 .....

AIM:- Designing a +ve -ve clamper and a clipper circuit.

APPARATUS REQUIRED:- Capacitor, p-n junction, resistor

THEORY:-

Clamping is a function which must be frequently performed with a periodic waveform in the establishment of the recurrent positive or negative extremity at some constant reference level. Clamping circuits are also referred to as DC restorer or DC inserter.

POSITIVE CLAMPER CIRCUIT :-

When a negative back of a signal is a clamped above to when a negative is zero, then the signal is said to be positively clamped and the circuit is called positive clamper circuit.

Initially, the capacitor is not charged in +ve half cycle, and the cycle of diode is in off state. As the capacitor change to on, in negative half cycle the diode is in 'ON' state.

In the ~~consecutive~~ consecutive half cycle (+ve), the capacitor is now charged to $+V_n$ and the diode is in off state and gets open circuited. The output of the circuit at this moment will be $V_o = V_i + V_n$. Hence, the signal is +ve clamped as shown. The V_o changes according to the changes in the V_i, but shifts the level according to the charge on the capacitor, as it adds the input V_i, the input and output signal is shown in graph.

NEGATIVE CLAMPER CIRCUIT:-

When a +ve pack of the signal is clamped below to the zero, then the signal is said to be negatively clamped

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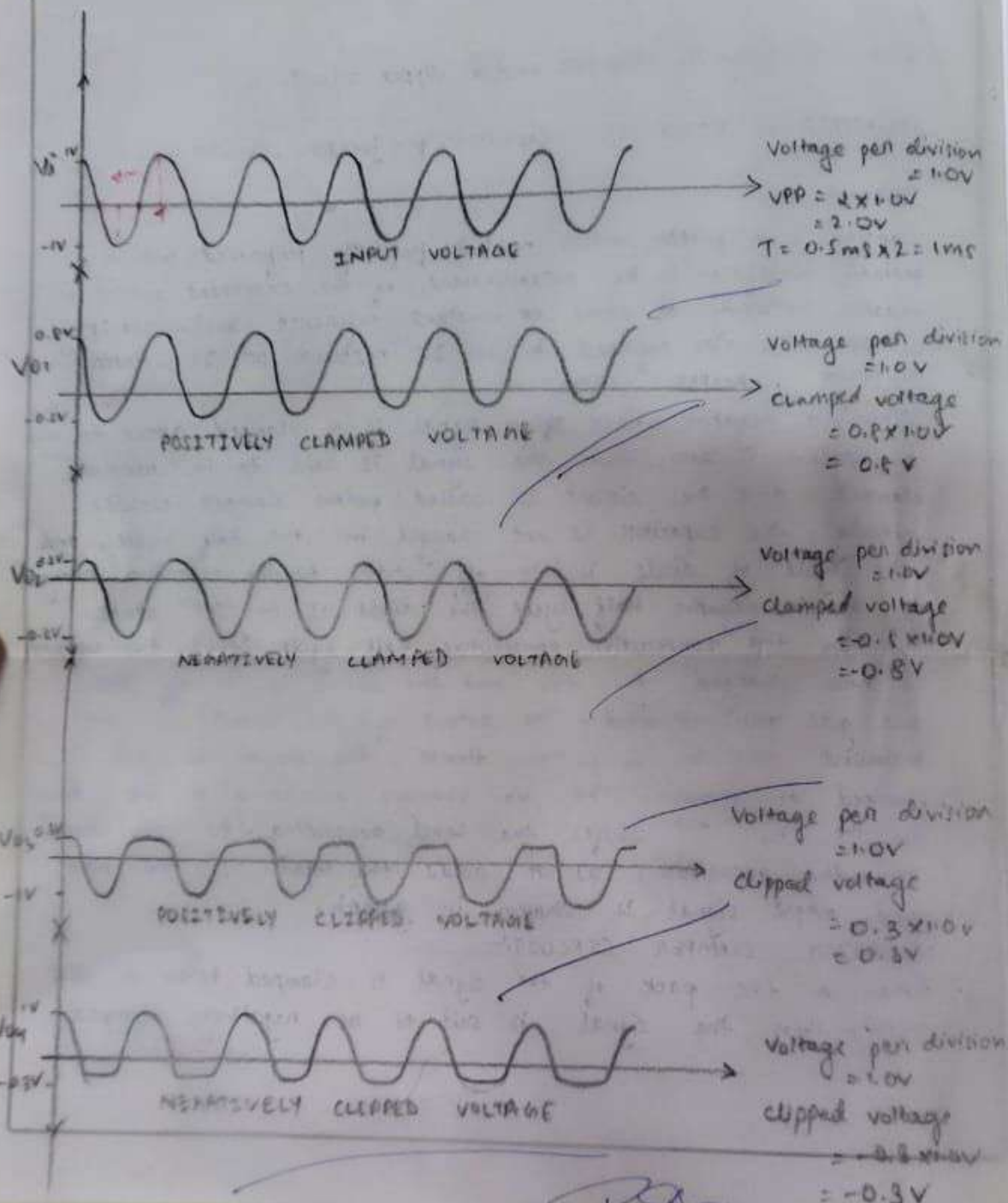
INPUT VOLTAGE
Voltage per division = 1.0V
VPP = 2 x 1.0V = 2.0V
T = 0.5ms x 2 = 1ms
POSITIVELY CLAMPED VOLTAGE
Voltage per division = 1.0 V
Clamped voltage = 0.8 x 1.0V = 0.8 V
NEGATIVELY CLAMPED VOLTAGE
Voltage per division = 1.0V
Clamped voltage = -0.8 x 1.0V = -0.8V
POSITIVELY CLIPPED VOLTAGE
Voltage per division = 1.0V
Clipped voltage = 0.3 x 1.0 V = 0.3V
NEGATIVELY CLIPPED VOLTAGE
Voltage per division = 1.0V
clipped voltage = -0.3 x 1.0V = -0.3V

19/02/24

Date .....

Expt. No. .....

Reverse biased: If $V_i < V_n$, than the diode D is in reverse bias means 'OFF' state. The output voltage $v_o = v_i$, the transfer curve has one breaks at $V_o = V_i = V_n$ and has the following characteristics (assuming $V_a \gg V_f$ and $R_f \ll R$).

Input (V_i)	Output (V_o)	Diode state
$V_i < V_n$ (=0)	$V_o = V_i$	Diode : ON
$V_i \geq V_n$ (=0)	$V_o = V_n$	Diode : OFF

Clipper circuit with forward bias diode in series:-

1. Observe the circuit diagram of the clipper.
2. Click on the power on button.
3. Select the amplitude (A) of the input sine wave signal (V_i).
4. Select the frequency of the signal (f) for the input signal (V_f).
5. Select the battery voltage (V_m).
6. Observe the input signal and clipped output signal (V_o) in the graph.
7. Change the values of A, f and V_n to observe the variation in the output signal.
8. Oven on the graph to observe the value of the V_i and V_o at that instant of time T.
9. Save the graph if you are done with experiment.

Clipper circuit with reverse bias diode in series:-

1. Observe the circuit diagram of the clipper.
2. Click on the power button.
3. Select amplitude of input sine wave signal (V_i)
4. Select the frequency (f) for the input signal.

Teacher's Signature : _____

Date .....

Expt. No. ..... Page No. 5

And the circuit is called negative clamper circuit.

CLAMPER CIRCUIT WITH POSITIVE CLAMPING :-

1. Observe the circuits diagram of full wave rectifier.
2. Click on the power button.
3. Select the amplitude (A) of the input sine wave signal (V_i)
4. Select the frequency (f) of the signal for the input signal (V_i).
5. Select the channel-1 to observe the input signal on graph.
6. Select the channel-2 to observe the output signal on graph
7. Change the value of A, f to observe the variation in the input and output signal.
8. Hover on the graph to observe the value of the V_i and V_o at the instant of time 'T.

CLAMPER CIRCUIT WITH NEGATIVE CLAMPING :-

Proceed with same steps in positive clamping.

CLIPPER CIRCUIT :-

Clipper circuit with diode in series :-

Forward biased: If $V_i > V_n$ then the diode D is in forward bias means 'ON' state. The output voltage $V_o = V_i$, the transfer curve has one break at $V_o = V_i = V_n$ and has the following characteristics (assuming $V_n \gg V_f$) and $R_i \ll R$.

Input (V_i)	Output (V_o)	Diode state
$V_i > V_n (=0)$	$V_i = V_o$	Diode = ON
$V_i < V_n (=0)$	$V_o = V_n (=0)$	Diode = OFF

Teacher's Signature : _____

Date .....

Expt. No. .....

Page No. 7

5. And proceed the same as in earlier experiment.

Conclusion :-

From the above experiment, we are able to design clamper and clipper circuit. We observe the graph and understand the working of these circuits.

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