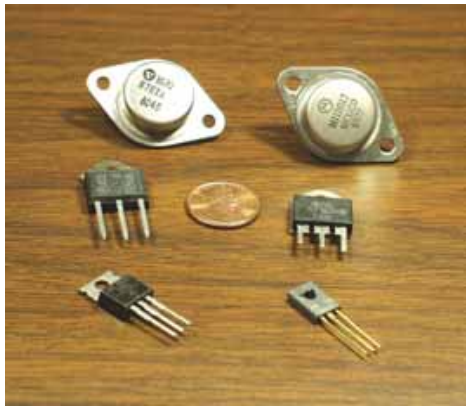
Contents

19

Field Effect Transistors

19.1 Types of Field Effect Transistors
19.3 Principle and Working of JFET
19.5 Importance of JFET
19.7 JFET as an Amplifier
19.9 Salient Features of JFET
19.11 Expression for Drain Current (I_D)
19.13 Parameters of JFET
19.15 Variation of Transconductance (g_m or g_{fs}) of JFET
19.17 JFET Biasing by Bias Battery
19.19 JFET with Voltage-Divider Bias
19.21 Practical JFET Amplifier
19.23 D.C. Load Line Analysis
19.25 Voltage Gain of JFET Amplifier (With Source Resistance R_s)
19.27 Metal Oxide Semiconductor FET (MOSFET)
19.29 Symbols for D-MOSFET
19.31 D-MOSFET Transfer Characteristic
19.33 D-MOSFET Biasing
19.35 D-MOSFETs Versus JFETs
19.37 E-MOSFET Biasing Circuits



INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor market-

ing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

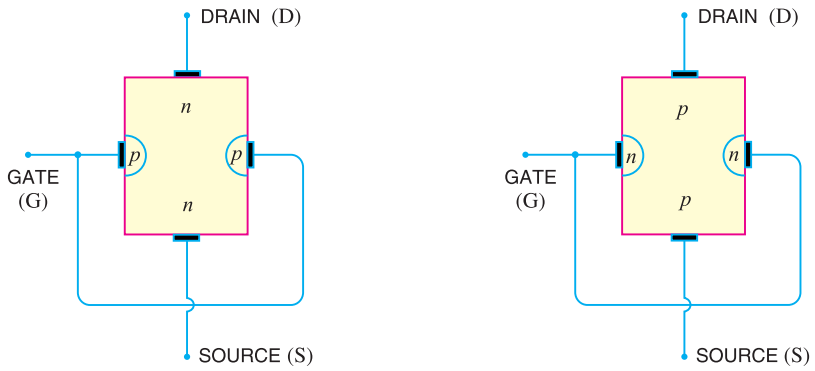
To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET*.

19.2 Junction Field Effect Transistor (JFET)

A **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig.19.1. The bar forms the conducting channel for the charge carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 19.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 19.1 (*ii*). The two *pn* junctions forming diodes are connected *internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz*., *gate* (*G*), *source* (*S*) and *drain* (*D*).



n-Channel JFET (*i*) *p-Channel JFET* (*ii*)

Fig. 19.1

* It would seem from Fig. 19.1 that there are three doped material regions. However, this is not the case. The gate material *surrounds* the channel in the same manner as a belt surrounding your waist.

JFET polarities. Fig. 19.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 19.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain.

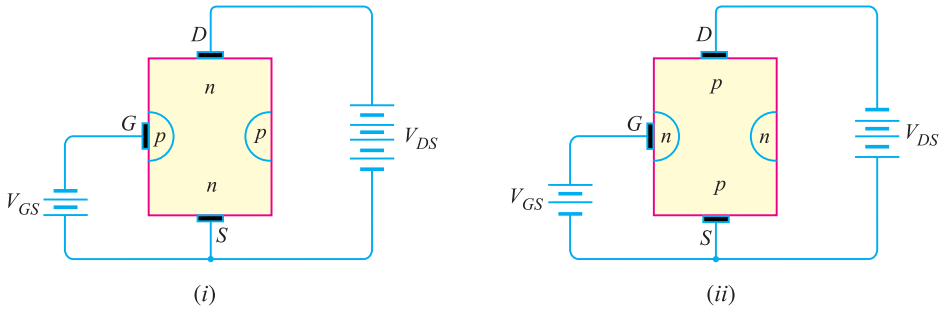


Fig. 19.2

The following points may be noted :

(*i*) The input circuit (*i.e.* gate to source) of a *JFET* is reverse biased. This means that the device has high input impedance.

(*ii*) The drain is so biased w.r.t. source that drain current I_D flows from the source to drain.

(*iii*) In all *JFETs*, source current I_S is equal to the drain current *i.e.* $I_S = I_D$.

19.3 Principle and Working of JFET

Fig. 19.3 shows the circuit of *n*-channel *JFET* with normal polarities. Note that the gate is reverse biased.

Principle. The two *pn* junctions at the sides form two depletion layers. The current conduction by charge carriers (*i.e.* free electrons in this case) is through the channel between the two depletion layers and out of the drain. The width and hence *resistance of this channel can be controlled by changing the input voltage V_{GS}. The greater the reverse voltage V_{GS}, the wider will be the depletion layers and narrower will be the conducting channel. The narrower channel means greater resistance and hence source to drain current decreases. Reverse will happen should V_{GS} decrease. *Thus JFET operates on the principle that width and hence resistance of the conducting channel can be varied by changing the reverse voltage V_{GS}.* In other words, the magnitude of drain current (I_D) can be changed by altering V_{GS}.

Working. The working of *JFET* is as under :

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 19.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 19.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

* The resistance of the channel depends upon its area of X-section. The greater the X-sectional area of this channel, the lower will be its resistance and the greater will be the current flow through it.

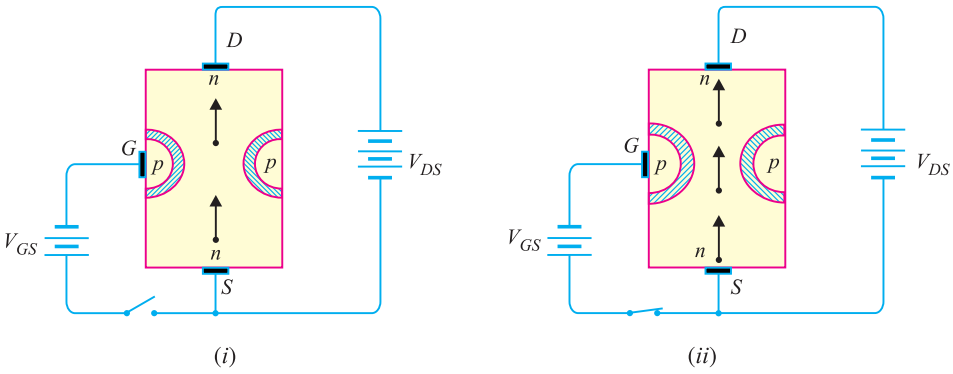
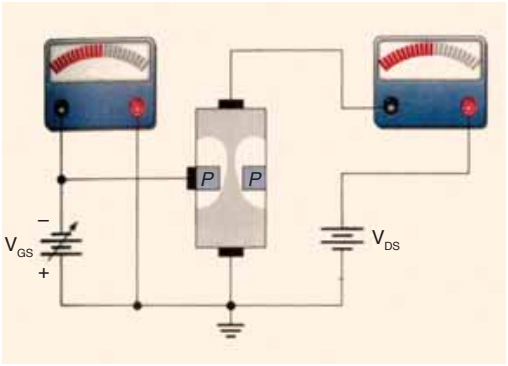


Fig. 19.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

Note. If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel becomes a non-conductor.



JFET biased for Conduction

19.4 Schematic Symbol of JFET

Fig. 19.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought

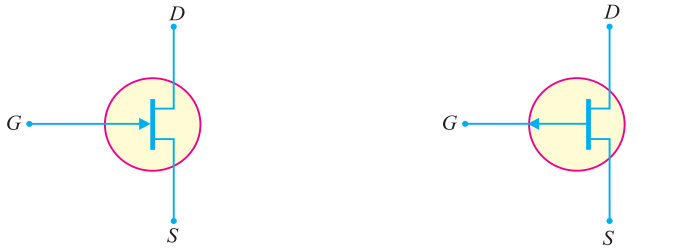
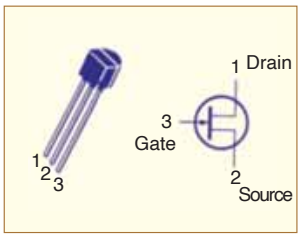


Fig. 19.4

as channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 19.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 19.4 (*ii*)].



19.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

19.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) The primary functional difference between the *JFET* and the *BJT* is that no current (actually, a very, very small current) enters the gate of *JFET* (*i.e.* $I_G = 0$A). However, typical *BJT* base current might be a few μA while *JFET* gate current a thousand times smaller [See Fig. 19.5].

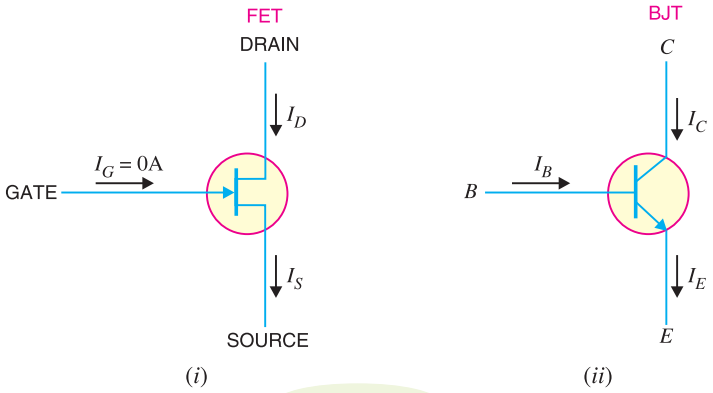


Fig. 19.5

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

(iv) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(v) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

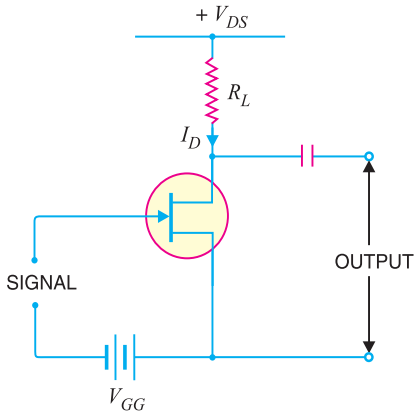


Fig. 19.6

19.7 JFET as an Amplifier

Fig. 19.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

19.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 19.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 19.8 shows a family of output characteristics.

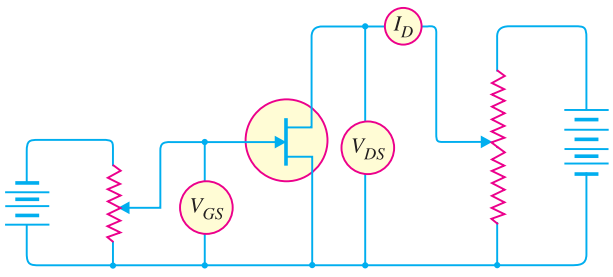


Fig. 19.7

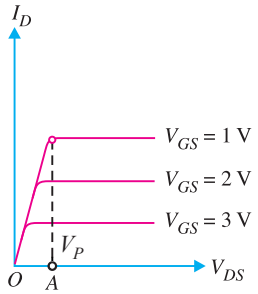


Fig. 19.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 19.8, *OA* is the *pinch off voltage* V_P.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

19.9 Salient Features of JFET

The following are some salient features of *JFET* :

(*i*) A *JFET* is a three-terminal *voltage-controlled* semiconductor device *i.e.* input voltage controls the output characteristics of *JFET*.

(*ii*) The *JFET* is *always* operated with gate-source *pn* junction *reverse biased.

(*iii*) In a *JFET*, the gate current is zero *i.e.* $I_G = 0$A.

(*iv*) Since there is no gate current, $I_D = I_S$.

(*v*) The *JFET* must be operated between V_{GS} and $V_{GS\,(off)}$. For this range of gate-to-source voltages, I_D will vary from a maximum of I_{DSS} to a minimum of almost zero.

(*vi*) Because the two gates are at the same potential, both depletion layers widen or narrow down by an equal amount.

(*vii*) The *JFET* is not subjected to thermal runaway when the temperature of the device increases.

(*viii*) The drain current I_D is controlled by changing the channel width.

(*ix*) Since *JFET* has no gate current, there is no β rating of the device. We can find drain current I_D by using the eq. mentioned in Art. 19.11.

19.10 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS\,(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current*.

Fig 19.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 19.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and **holds drain current constant at I_{DSS}.

* Forward biasing gate-source *pn* junction may destroy the device.

** When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

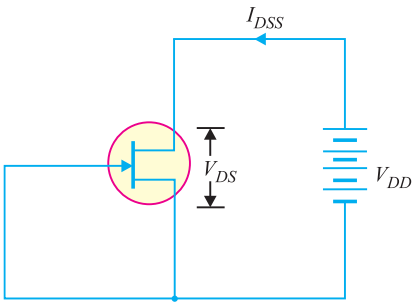


Fig. 19.9

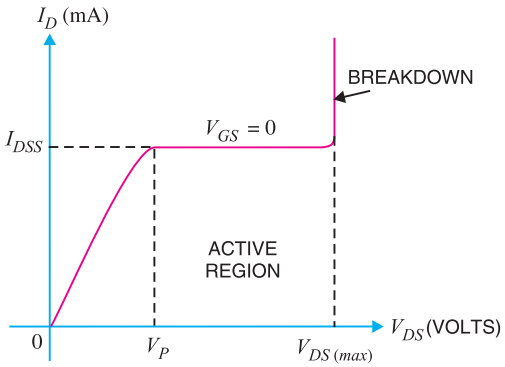


Fig. 19.10

The following points may be noted carefully :

(*i*) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 19.10.

(*iii*) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or *active region*. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

2. Pinch off Voltage (V_p). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 19.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$V, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

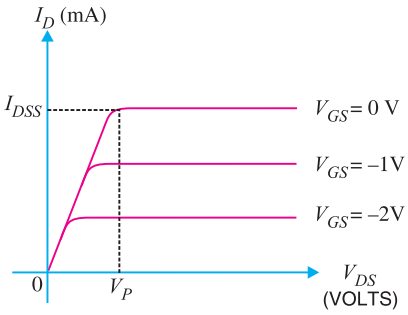


Fig . 19.11

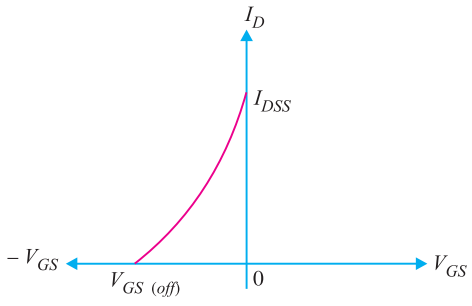


Fig . 19.12

3. Gate-source cut off voltage $V_{GS\,(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 19.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases. This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\,(off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\,(off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}. However, $V_{GS\,(off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

19.11 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 19.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS\,(off)} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 19.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where
I_D = drain current at given V_{GS}
I_{DSS} = shorted – gate drain current
V_{GS} = gate–source voltage
$V_{GS\,(off)}$ = gate–source cut off voltage

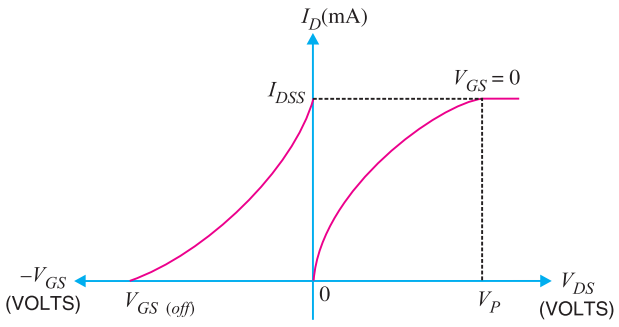


Fig. 19.13

Example 19.1. *Fig. 19.14 shows the transfer characteristic curve of a JFET. Write the equation for drain current.*

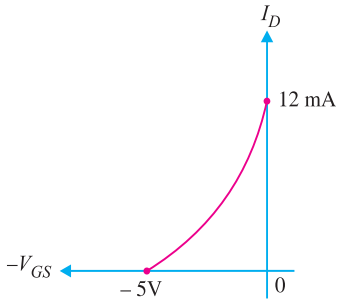


Fig. 19.14

Solution. Referring to the transfer characteristic curve in Fig. 19.14, we have,

$$I_{DSS} = 12 \text{ mA}$$
$$V_{GS\,(off)} = -5 \text{ V}$$
$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$\text{or} \quad I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA} \quad \textbf{Ans.}$$

Example 19.2. *A JFET has the following parameters: $I_{DSS} = 32$ mA ; $V_{GS\,(off)} = -8V$; $V_{GS} = -4.5$ V. Find the value of drain current.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$
$$= \textbf{6.12 mA}$$

Example 19.3. *A JFET has a drain current of 5 mA. If $I_{DSS} = 10$ mA and $V_{GS\,(off)} = -6$ V, find the value of (i) V_{GS} and (ii) V_P.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$\text{or} \quad 5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$
$$\text{or} \quad 1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$
(i) $\therefore \quad V_{GS} = \textbf{– 1.76 V}$
(ii) and $\quad V_P = -V_{GS\,(off)} = \textbf{6 V}$

Example 19.4. *For the JFET in Fig. 19.15, $V_{GS\,(off)} = -4V$ and $I_{DSS} = 12$ mA. Determine the minimum value of V_{DD} required to put the device in the constant-current region of operation.*

Solution. Since $V_{GS\,(off)} = -4$V, $V_P = 4$V. The minimum value of V_{DS} for the *JFET* to be in constant-current region is

$$V_{DS} = V_P = 4\text{V}$$

In the constant current region with $V_{GS} = 0$V,

$$I_D = I_{DSS} = 12 \text{ mA}$$

Applying Kirchhoff's voltage law around the drain circuit, we have,

$$V_{DD} = V_{DS} + V_{R_D} = V_{DS} + I_D R_D$$
$$= 4\text{V} + (12 \text{ mA})\,(560\Omega) = 4\text{V} + 6.72\text{V} = \textbf{10.72V}$$

This is the value of V_{DD} to make $V_{DS} = V_P$ and put the device in the constant-current region.

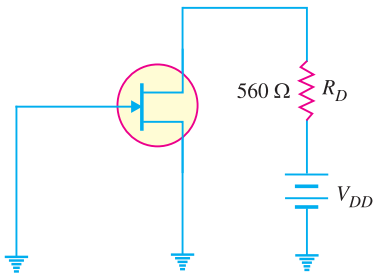


Fig. 19.15

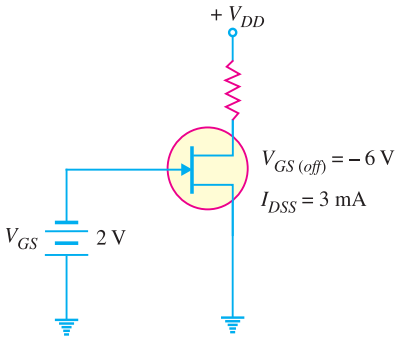


Fig. 19.16

Example 19.5. *Determine the value of drain current for the circuit shown in Fig. 19.16.*

Solution. It is clear from Fig. 19.16 that $V_{GS} = -2$V. The drain current for the circuit is given by;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 3\text{ mA}\left(1 - \frac{-2\text{V}}{-6\text{V}}\right)^2$$

$$= (3\text{ mA})\,(0.444) = \mathbf{1.33\text{ mA}}$$

Example 19.6. *A particular p-channel JFET has a* $V_{GS\,(off)} = +4V$. *What is* I_D *when* $V_{GS} = +6V$?

Solution. The *p*-channel *JFET* requires a positive gate-to-source voltage to pass drain current I_D. The more the positive voltage, the less the drain current. When $V_{GS} = 4$V, $I_D = 0$ and *JFET* is cut off. Any further increase in V_{GS} keeps the *JFET* cut off. Therefore, at $V_{GS} = +6$V, $I_D = \mathbf{0A.}$

19.12 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.

19.13 Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are (*i*) a.c. drain resistance (*ii*) transconductance (*iii*) amplification factor.

(*i*) a.c. drain resistance (r_d). Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :