19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as ***depletion-mode* operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

*A field effect transistor (FET) that can be operated in the enhancement-mode is called a **MOSFET**.*

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs viz.*

1. Depletion-type *MOSFET* or ***D-MOSFET.*** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called depletion/enhancement *MOSFET*.
2. Enhancement-type *MOSFET* or ***E-MOSFET.*** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons ($\because$ it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

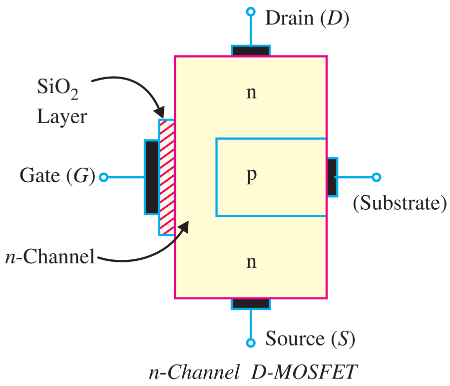
(ii) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals *viz* *source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

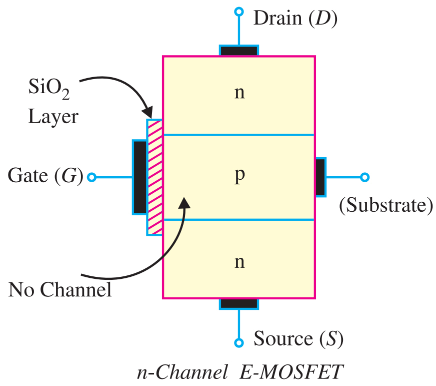
* With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.

** With gate reverse biased, the channel is depleted (*i.e.* emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.



n-Channel D-MOSFET

Fig. 19.43



n-Channel E-MOSFET

Fig. 19.44

2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel *E-MOSFET.* Its gate construction is similar to that of *D-MOSFET*. The *E-MOSFET* has no channel between source and drain unlike the *D-MOSFET*. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The *E-MOSFET* requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that *E-MOSFET* can be operated *only* in enhancement mode. In short, the construction of *E-MOSFET* is quite similar to that of the *D-MOSFET* except for the absence of a channel between the drain and source terminals.

Why the name MOSFET ? The reader may wonder why is the device called *MOSFET?* The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET.* Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET).* However, this term is rarely used in place of the term *MOSFET*.

19.29 Symbols for D-MOSFET

There are two types of *D-MOSFETs viz* (*i*) *n*-channel *D-MOSFET* and (*ii*) *p*-channel *D-MOSFET*.

(*i*) n-channel D-MOSFET. Fig. 19.45 (*i*) shows the various parts of *n*-channel *D-MOSFET*. The *p*-type substrate constricts the channel between the source and drain so that only a small passage

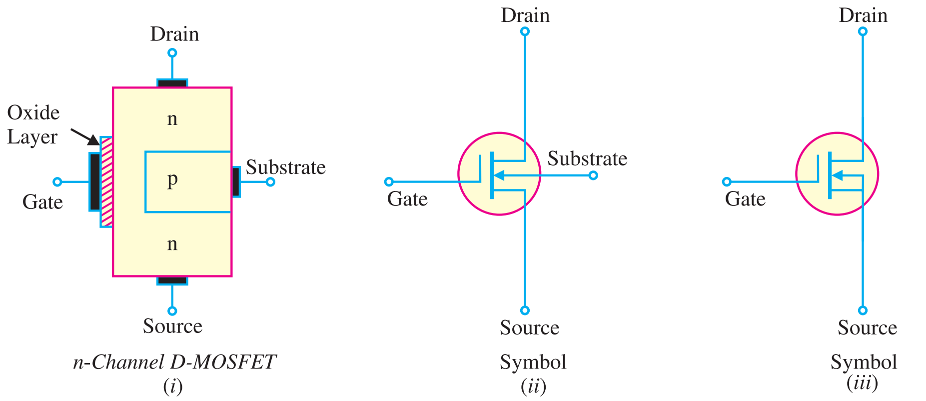


Fig. 19.45

remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel *D-MOSFET* is shown in Fig. 19.45 (*ii*). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel *D-MOSFET*. It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (*iii*). This gives rise to a three-terminal device.

(*ii*) *p*-channel D-MOSFET. Fig. 19.46 (*i*) shows the various parts of *p*-channel *D-MOSFET*. The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel *D-MOSFET* is shown in Fig. 19.46 (*ii*). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (*iii*).

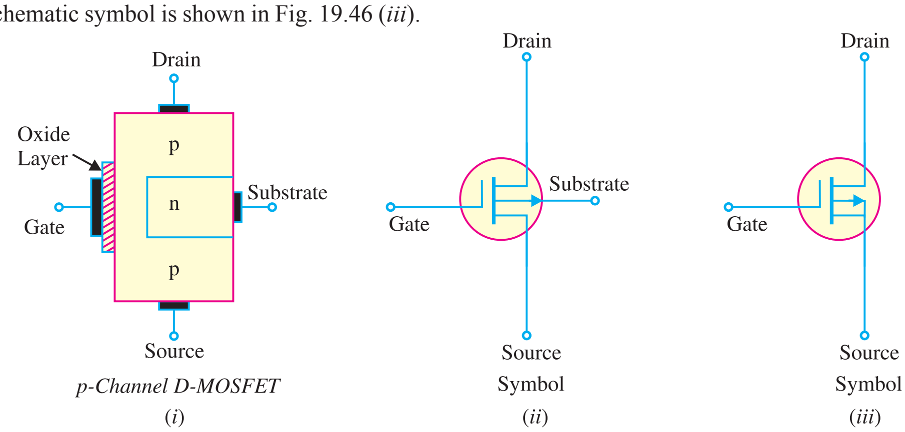


Fig. 19.46

19.30 Circuit Operation of D-MOSFET

Fig. 19.47 (*i*) shows the circuit of *n*-channel *D-MOSFET*. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the n-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive-gate operation is known as *enhancement mode.*

(*i*) Depletion mode. Fig. 19.47 (*i*) shows depletion-mode operation of *n*-channel *D-MOSFET*. Since gate is negative, it means electrons are on the gate as shown is Fig. 19.47 (*ii*). These electrons *repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (*ii*). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of *D-MOSFET* is similar to *JFET*. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode.*

* If one plate of the capacitor is negatively charged, it induces positive charge on the other plate.

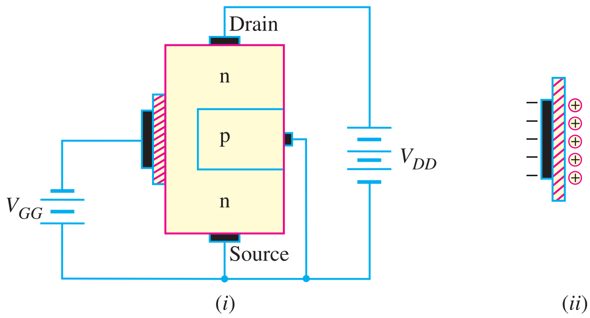


Fig. 19.47

(ii) **Enhancement mode.** Fig. 19.48 (*i*) shows enhancement-mode operation of *n*-channel *D-MOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (*ii*). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially *zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode.*

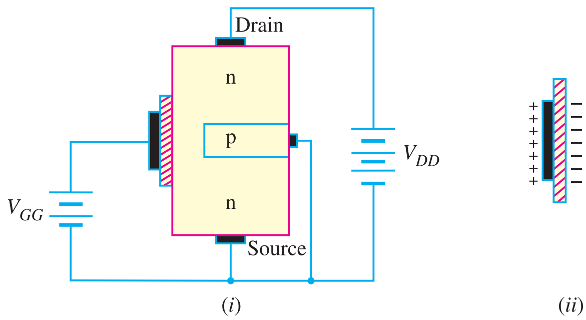


Fig. 19.48

The following points may be noted about *D-MOSFET* operation :

(i) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(ii) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(iii) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether

* Note that gate of *JFET* is always reverse biased for proper operation. However, in a *MOSFET*, because of the insulating layer, a negligible gate current flows whether we apply negative or positive voltage to gate.

positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,00 MΩ.

(iv) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(i) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted *i.e.* $V_{GS} = 0$.

(ii) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS\,(off)}$ just as with *JFET*.

(iii) When V_{GS} is *positive*, I_D increases above the value of I_{DSS}. The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

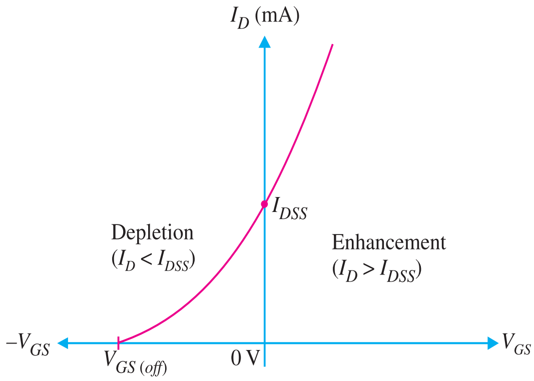


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation *viz.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

Example 19.30. *For a certain D-MOSFET, I_{DSS} = 10 mA and $V_{GS\,(off)} = -8V$.*

(*i*) *Is this an n-channel or a p-channel ?*

(*ii*) *Calculate I_D at $V_{GS} = -3V$.*

(*iii*) *Calculate I_D at $V_{GS} = +3V$.*

Solution.

(i) The device has a negative $V_{GS\,(off)}$. Therefore, it is ***n*-channel *D-MOSFET***.

(ii)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{-3}{-8}\right)^2 = \mathbf{3.91\ mA}$$