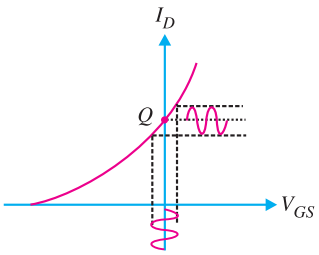


Fig. 19.50

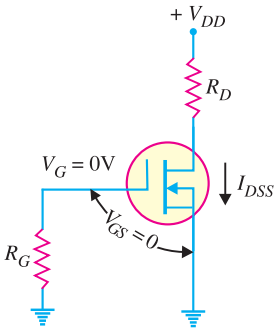


Fig. 19.51

We can use the simple circuit of Fig. 19.51 to provide zero bias. This circuit has $V_{GS} = 0$V and $I_D = I_{DSS}$. We can find V_{DS} as under :

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Note that for the *D-MOSFET* zero bias circuit, the source resistor (R_S) is not necessary. With no source resistor, the value of V_S is 0V. This gives us a value of $V_{GS} = 0$V. This biases the circuit at $I_D = I_{DSS}$ and $V_{GS} = 0$V. For mid-point biasing, the value of R_D is so selected that $V_{DS} = V_{DD}/2$.

Example 19.32. *Determine the drain-to-source voltage (V_{DS}) in the circuit shown in Fig. 19.51 above if $V_{DD} = +18V$ and $R_D = 620\Omega$. The MOSFET data sheet gives $V_{GS(off)} = -8V$ and $I_{DSS} = 12$ mA.*

Solution. Since $I_D = I_{DSS} = 12$ mA, the V_{DS} is given by;

$$V_{DS} = V_{DD} - I_{DSS} R_D$$
$$= 18\text{V} - (12\text{ mA})\,(0.62\text{ k}\Omega) = \mathbf{10.6V}$$

19.34 Common-Source D-MOSFET Amplifier

Fig. 19.52 shows a common-source amplifier using *n*-channel *D-MOSFET*. Since the source terminal is common to the input and output terminals, the circuit is called *common-source amplifier. The circuit is zero biased with an a.c. source coupled to the gate through the coupling capacitor C_1. The gate is at approximately 0V d.c. and the source terminal is grounded, thus making $V_{GS} = 0$V.

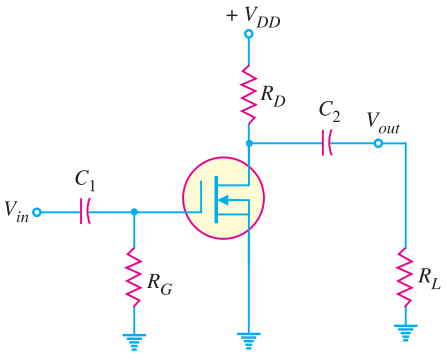


Fig. 19.52

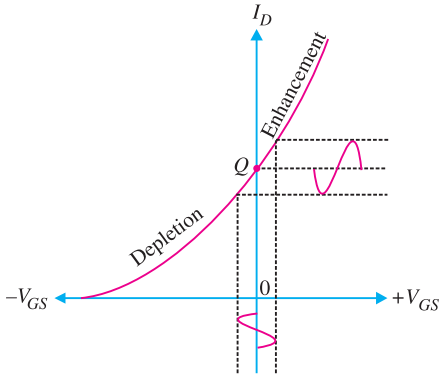


Fig. 19.53

* It is comparable to common-emitter transistor amplifier.

Operation. The input signal (V_{in}) is capacitively coupled to the gate terminal. In the absence of the signal, d.c. value of $V_{GS} = 0$V. When signal (V_{in}) is applied, V_{gs} swings above and below its zero value (Q d.c. value of $V_{GS} = 0$V), producing a swing in drain current I_d.

(i) A small change in gate voltage produces a large change in drain current as in a *JFET*. This fact makes *MOSFET* capable of raising the strength of a weak signal; thus acting as an amplifier.

(ii) During the positive half-cycle of the signal, the positive voltage on the gate increases and produces the enhancement-mode. This increases the channel conductivity and hence the drain current.

(iii) During the negative half-cycle of the signal, the positive voltage on the gate decreases and produces depletion-mode. This decreases the conductivity and hence the drain current.

The result of above action is that a small change in gate voltage produces a large change in the drain current. This large variation in drain current produces a large a.c. output voltage across drain resistance R_D. In this way, *D-MOSFET* acts as an amplifier. Fig. 19.53 shows the amplifying action of *D-MOSFET* on transconductance curve.

Voltage gain. The a.c. analysis of *D-MOSFET* is similar to that of the *JFET*. Therefore, voltage gain expressions derived for *JFET* are also applicable to *D-MOSFET*.

$$\text{Voltage gain, } A_v = g_m R_D \quad \text{... for unloaded } D\text{-}MOSFET \text{ amplifier}$$
$$= g_m R_{AC} \quad \text{... for loaded } D\text{-}MOSFET \text{ amplifier}$$

Note the total a.c. drain resistance $R_{AC} = R_D \parallel R_L$.

Example 19.33. *The D-MOSFET used in the amplifier of Fig. 19.54 has an $I_{DSS} = 12$ mA and $g_m = 3.2$ mS. Determine (i) d.c. drain-to-source voltage V_{DS} and (ii) a.c. output voltage. Given $v_{in} = 500$ mV.*

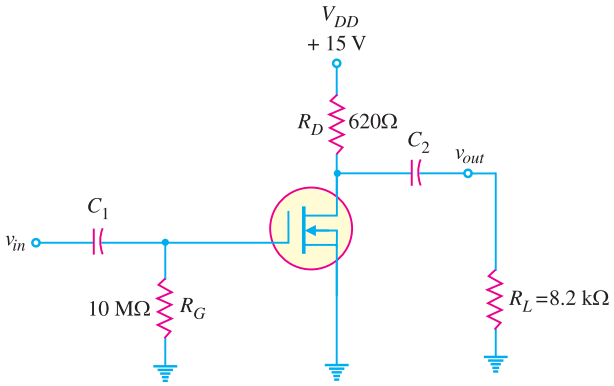


Fig. 19.54

Solution.

(i) Since the amplifier is zero biased, $I_D = I_{DSS} = 12$ mA.

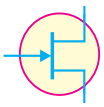
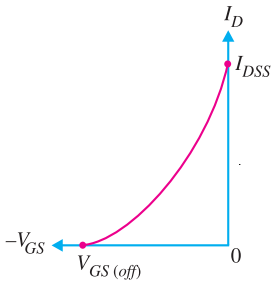
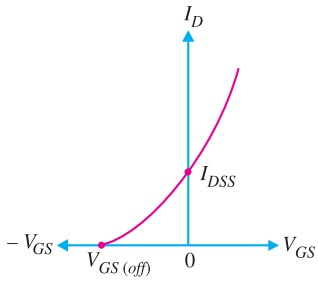
$$\therefore \quad V_{DS} = V_{DD} - I_{DSS} R_D$$
$$= 15\text{V} - (12\text{ mA})\,(0.62\text{ k}\Omega) = \mathbf{7.56V}$$

(ii) Total a.c. drain resistance R_{AC} of the circuit is

$$R_{AC} = R_D \parallel R_L = 620\Omega \parallel 8.2\text{ k}\Omega = 576\Omega$$
$$\therefore \quad v_{out} = A_v \times v_{in} = (g_m R_{AC})\,(v_{in})$$
$$= (3.2 \times 10^{-3}\ S \times 576\ \Omega)\,(500\text{ mV}) = \mathbf{922\text{ mV}}$$

19.35 D-MOSFETs Versus JFETs

Table below summarises many of the characteristics of *JFET*s and *D-MOSFET*s.

Devices:	*JFETs*	*D-MOSFETs*
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion only	Depletion and enhancement
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias	Gate bias Self bias Voltage-divider bias Zero bias
Advantages:	Extremely high input impedance.	Higher input impedance than a comparable *JFET*. Can operate in both modes (depletion and enhancement).
Disadvantages:	Bias instability. Can operate only in the depletion mode.	Bias instability. More sensitive to changes in temperature than the *JFET*.

19.36 E-MOSFET

Two things are worth noting about *E-MOSFET*. First, *E-MOSFET* operates *only* in the enhancement mode and has no depletion mode. Secondly, the *E-MOSFET* has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig. 19.55 (*i*)]. It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the *E-MOSFET* is called *Threshold voltage* [$V_{GS\,(th)}$]. The *n*-channel device requires positive V_{GS} ($\geq V_{GS\,(th)}$) and the *p*-channel device requires negative V_{GS} ($\geqslant V_{GS\,(th)}$).

Operation. Fig. 19.55 (*i*) shows the circuit of *n*-channel *E-MOSFET*. The circuit action is as under :

(*i*) When $V_{GS} = 0$V [See Fig. 19.55(*i*)], there is no channel connecting the source and drain. The *p* substrate has only a few thermally produced free electrons (minority carriers) so that drain current is essentially zero. For this reason, *E-MOSFET* is normally *OFF* when $V_{GS} = 0$ V. Note that this behaviour of *E-MOSFET* is quite different from *JFET* or *D-MOSFET*.

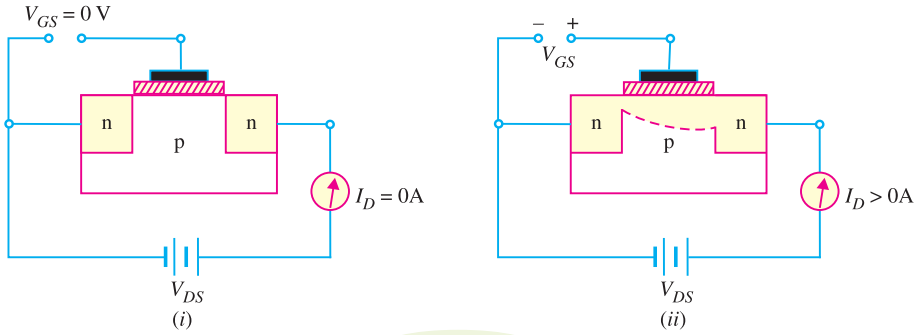


Fig. 19.55

(ii) When gate is made positive (*i.e.* V_{GS} is positive) as shown in Fig. 19.55 (*ii*), it attracts free electrons into th *p* region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is the same as creating a thin layer of *n*-type material (*i.e.* inducing a thin *n*-channel) adjacent to the SiO_2 layer. Thus the *E-MOSFET* is turned *ON* and drain current I_D starts flowing form the source to the drain.

The minimum value of V_{GS} that turns the E-MOSFET ON is called ***threshold voltage*** *[$V_{GS\,(th)}$].*

(iii) When V_{GS} is less than $V_{GS\,(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS\,(th)}$, the *E-MOSFET* is turned *ON* and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS\,(th)}$, if the value of V_{GS} is *increased*, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS\,(th)}$], the channel becomes narrower and I_D will decrease. This fact is revealed by the transconductance curve of *n*-channel *E-MOSFET* shown in Fig. 19.56. As you can see, $I_D = 0$ when $V_{GS} = 0$. Therefore, the value of I_{DSS} for the *E-MOSFET* is zero. Note also that there is no drain current until V_{GS} reaches $V_{GS\,(th)}$.

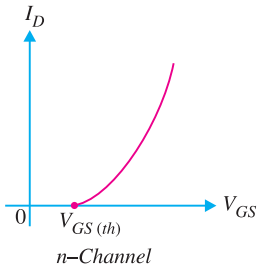


Fig. 19.56

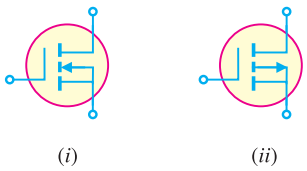


Fig. 19.57

Schematic Symbols. Fig. 19.57 (*i*) shows the schematic symbols for *n*-channel *E-MOSFET* whereas Fig. 19.57 (*ii*) shows the schematic symbol for *p*-channel *E-MOSFET*. When $V_{GS} = 0$, the *E-MOSFET* is *OFF* because there is no conducting channel between source and drain. The broken channel line in the symbols indicates the normally *OFF* condition.

Equation for Transconductance Curve. Fig. 19.58 shows the transconductance curve for *n*-channel *E-MOSFET*. Note that this curve is different from the transconductance curve for *n*-channel *JFET* or *n*-channel *D-MOSFET*. It is because it starts at $V_{GS\,(th)}$ rather than $V_{GS\,(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the *E-MOSFET* transconductance curve (for $V_{GS} > V_{GS\,(th)}$) is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant K depends on the particular *E-MOSFET* and its value is determined from the following equation :

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

Any data sheet for an *E-MOSFET* will include the current $I_{D(on)}$ and the voltage $V_{GS(on)}$ for one point well above the threshold voltage as shown in Fig. 19.58.

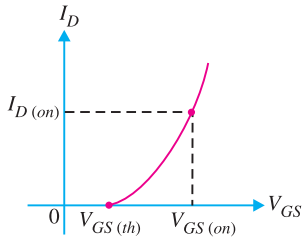


Fig. 19.58

Example 19.34. *The data sheet for an E-MOSFET gives $I_{D(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS(th)}$ = 1V. Determine the drain current for V_{GS} = 5V.*

Solution. Here $V_{GS(on)} = 10$ V.

$$I_D = K(V_{GS} - V_{GS(th)})^2 \quad \ldots (i)$$

Here $$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2} = \frac{500 \text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17 \text{ mA/V}^2$$

Putting the various values in eq. (*i*), we have,

$$I_D = 6.17 (5\text{V} - 1\text{V})^2 = \mathbf{98.7 \text{ mA}}$$

Example 19.35. *The data sheet for an E-MOSFET gives $I_{D(on)}$ = 3 mA at V_{GS} = 10V and $V_{GS(th)}$ = 3V. Determine the resulting value of K for the device. How will you plot the transconductance curve for this MOSFET ?*

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

Here $I_{D(on)} = 3$ mA ; $V_{GS(on)} = 10$V ; $V_{GS(th)} = 3$V

$$\therefore \quad K = \frac{3 \text{ mA}}{(10\text{V} - 3\text{V})^2} = \frac{3 \text{ mA}}{(7\text{V})^2} = \mathbf{0.061 \times 10^{-3} \text{ A/V}^2}$$

Now $$I_D = K(V_{GS} - V_{GS(th)})^2$$

In order to plot the transconductance curve for the device, we shall determine a few points for the curve by changing the value of V_{GS} and noting the corresponding values of I_D.

For V_{GS} = 5V ; $I_D = 0.061 \times 10^{-3} (5\text{V} - 3\text{V})^2 = 0.244$ mA

For V_{GS} = 8V ; $I_D = 0.061 \times 10^{-3} (8\text{V} - 3\text{V})^2 = 1.525$ mA

For V_{GS} = 10V ; $I_D = 0.061 \times 10^{-3} (10\text{V} - 3\text{V})^2 = 3$ mA

For V_{GS} = 12V ; $I_D = 0.061 \times 10^{-3} (12\text{V} - 3\text{V})^2 = 4.94$ mA

Thus we can plot the transconductance curve for the *E-MOSFET* from these V_{GS}/I_D points.

19.37 E-MOSFET Biasing Circuits

One of the problems with *E-MOSFET* is the fact that many of the biasing circuits used for *JFETs* and *D-MOSFETs* cannot be used with this device. For example, *E-MOSFETs* must have V_{GS} greater than the threshold value ($V_{GS(th)}$) so that zero bias cannot be used. However, there are two popular methods for *E-MOSFET* biasing *viz.*

(*i*) Drain-feedback bias

(*ii*) Voltage-divider bias

(*i*) Drain-feedback bias. This method of *E-MOSFET* bias is equivalent to collector-feedback bias in transistors. Fig. 19.59 (*i*) shows the drain-feedback bias circuit for *n*-channel *E-MOSFET*. A

high resistance R_G is connected between the drain and the gate. Since the gate resistance is superhigh, no current will flow in the gate circuit (*i.e.* $I_G = 0$). Therefore, there will be no voltage drop across R_G. Since there is no voltage drop across R_G, the gate will be at the same potential as the drain. This fact is illustrated in the d.c. equivalent circuit of drain-feedback bias as in Fig. 19.59 (*ii*).

$$\therefore \qquad V_D = V_G \quad \text{and} \quad V_{DS} = V_{GS}$$

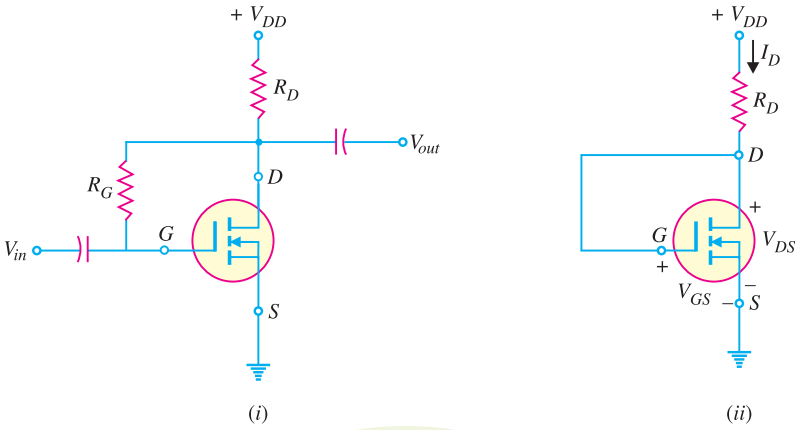


Fig. 19.59

The value of drain-source voltage V_{DS} for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D$$

Since $V_{DS} = V_{GS}$, $V_{GS} = V_{DD} - I_D R_D$

Since in this circuit $V_{DS} = V_{GS}$; $I_D = I_{D\,(on)}$.

Therefore, the *Q*-point of the circuit stands determined.

(*ii*) Voltage-divider Bias. Fig. 19.60 shows voltage divider biasing arrangement for *n*-channel *E-MOSFET*. Since $I_G = 0$, the analysis of the method is as follows :

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

and $$V_{DS} = V_{DD} - I_D R_D$$

where $$I_D = K (V_{GS} - V_{GS\,(th)})^2$$

Once I_D and V_{DS} are known, all the remaining quantities of the circuit such as V_D etc. can be determined.

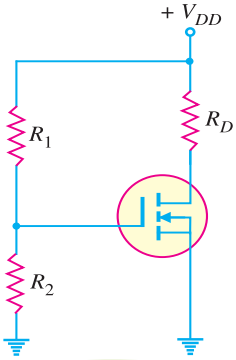


Fig. 19.60

Example 19.36. *Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Fig. 19.61. The data sheet for this particular MOSFET gives $I_{D\,(on)}$ = 500 mA at V_{GS} = 10V and $V_{GS\,(th)}$ = 1V.*

Solution. Referring to the circuit shown in Fig. 19.61, we have,

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

$$= \frac{24\text{V}}{(100 + 15)\,\text{k}\Omega} \times 15\,\text{k}\Omega = \mathbf{3.13V}$$

The value of K can be determined from the following equation :

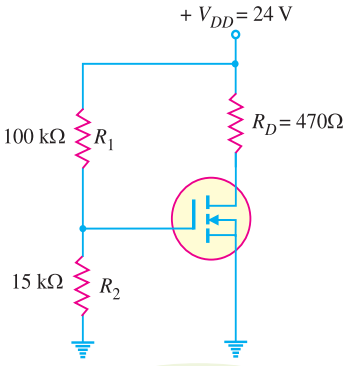


Fig. 19.61

$$K = \frac{I_{D\,(on)}}{(V_{GS\,(on)} - V_{GS\,(th)})^2}$$

$$= \frac{500\text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17\text{ mA/V}^2 \quad [\because V_{GS\,(on)} = 10\text{V}]$$

$\therefore$ $I_D = K\,(V_{GS} - V_{GS\,(th)})^2 = 6.17\text{ mA/V}^2\,(3.13\text{V} - 1\text{ V})^2 = 28\text{ mA}$

$\therefore$ $V_{DS} = V_{DD} - I_D R_D = 24\text{V} - (28\text{ mA})\,(470\Omega) = \mathbf{10.8V}$

Example 19.37. *Determine the values of I_D and V_{DS} for the circuit shown in Fig. 19.62. The data sheet for this particular MOSFET gives $I_{D\,(on)} = 10$ mA when $V_{GS} = V_{DS}$.*

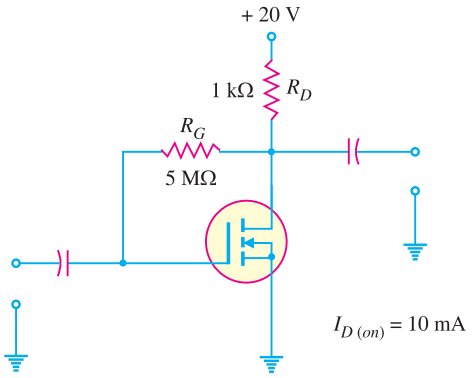


Fig. 19.62

Solution. Since in the drain-feedback circuit $V_{GS} = V_{DS}$,

$\therefore$ $I_D = I_{D\,(on)} = \mathbf{10\text{ mA}}$

The value of V_{DS} (and thus V_{GS}) is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

$$= 20\text{V} - (10\text{ mA})\,(1\text{ k}\Omega) = 20\text{V} - 10\text{V} = \mathbf{10V}$$

Example 19.38. *Determine the value of I_D for the circuit shown in Fig. 19.63. The data sheet for this particular MOSFET gives $I_{D\,(on)} = 10$ mA at $V_{GS} = 10$ V and $V_{GS\,(th)} = 1.5$ V.*

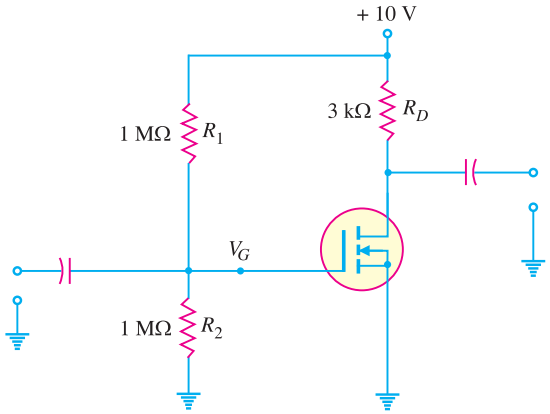


Fig. 19.63