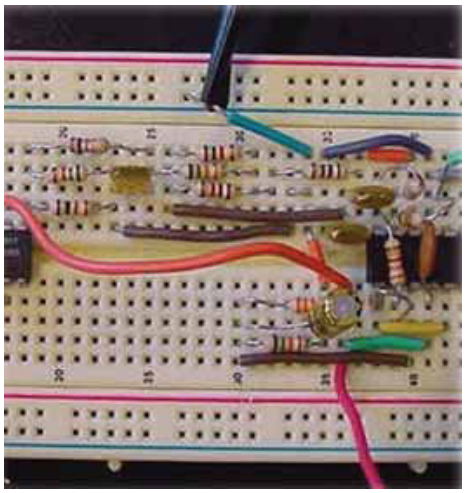
Contents

9

Transistor Biasing



INTRODUCTION

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*. In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

9.1 Faithful Amplification

The process of raising the strength of a weak signal without any change in its general shape is known as **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

(*i*) Proper zero signal collector current

(*ii*) Minimum proper base-emitter voltage (V_{BE}) at any instant

(*iii*) Minimum proper collector-emitter voltage (V_{CE}) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

(*i*) Proper zero signal collector current. Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

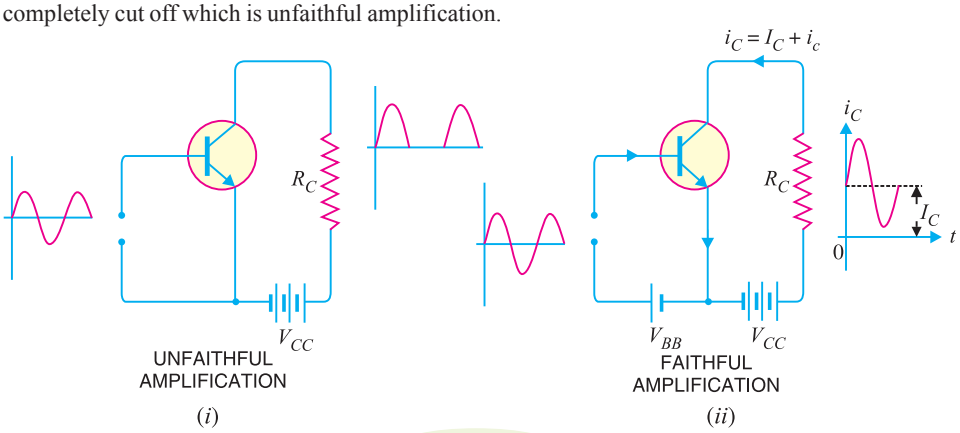


Fig. 9.1

Now, introduce a battery source V_{BB} in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current I_C will flow in the collector circuit due to V_{BB} as shown. This is known as *zero signal collector current* I_C. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

Zero signal collector current ≥ Max. collector current due to signal alone

Illustration. Suppose a signal applied to the base of a transistor gives a peak collector current of 1mA. Then zero signal collector current must be atleast equal to 1mA so that even during the peak of negative half-cycle of the signal, there is no cut off as shown in Fig. 9.2 (*i*).

If zero signal collector current is less, say 0.5 mA as shown in Fig. 9.2 (*ii*), then some part (shaded portion) of the negative half-cycle of signal will be cut off in the output.

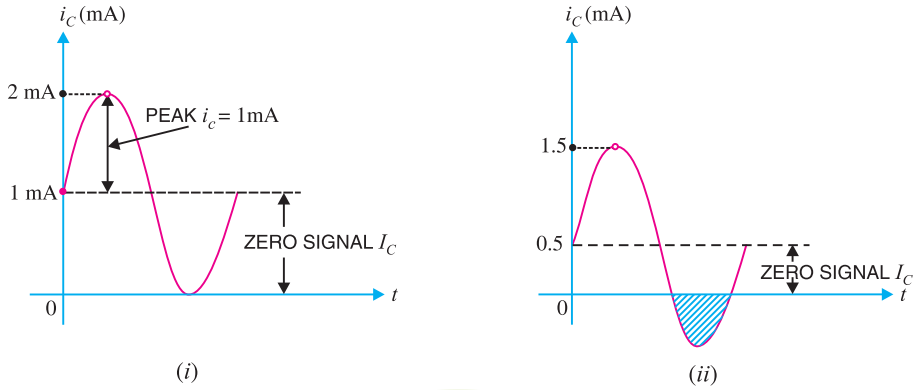


Fig. 9.2

(*ii*) Proper minimum base-emitter voltage. In order to achieve faithful amplification, the base-emitter voltage (V_{BE}) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.

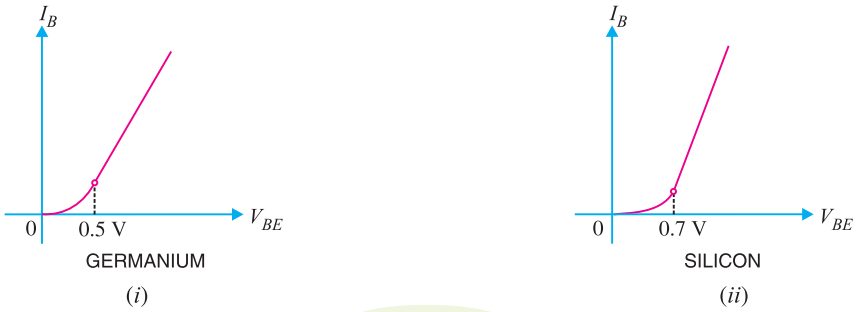


Fig. 9.3

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage V_{BE} falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

(*iii*) Proper minimum V_{CE} at any instant. For faithful amplification, the collector-emitter voltage V_{CE} should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.

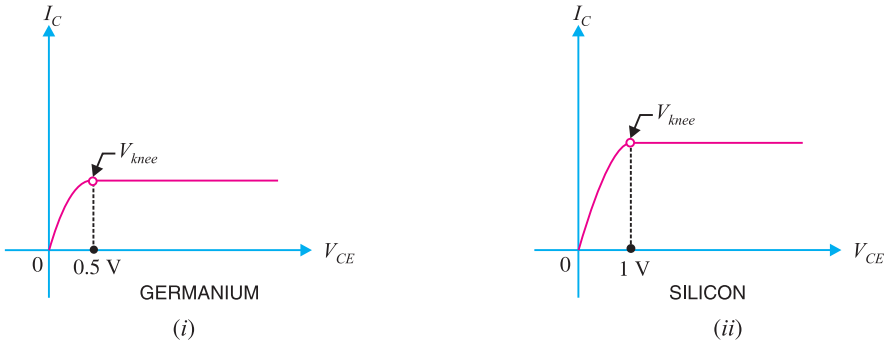


Fig. 9.4

When V_{CE} is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if V_{CE} is allowed to fall below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when V_{CE} is greater than V_{knee}, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

9.2 Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : *(i)* proper zero signal collector current, *(ii)* proper base-emitter voltage at any instant and *(iii)* proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as **transistor biasing.**

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as *biasing circuit*. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

Example 9.1. *An npn silicon transistor has V_{CC} = 6 V and the collector load R_C = 2.5 kΩ. Find :*

(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.

(ii) The minimum zero signal collector current required.

Solution. Collector supply voltage, V_{CC} = 6 V

Collector load, R_C = 2.5 kΩ

(i) We know that for faithful amplification, V_{CE} should not be less than 1V for silicon transistor.

∴ Max. voltage allowed across R_C = 6 – 1 = 5 V

∴ Max. allowed collector current = 5 V/R_C = 5 V/2.5 kΩ = **2 mA**

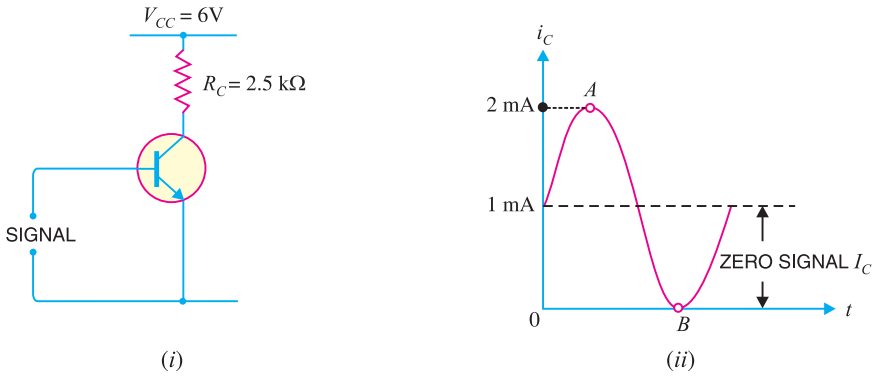


Fig. 9.5

Thus, the maximum collector current allowed during any part of the signal is 2 mA. If the collector current is allowed to rise above this value, V_{CE} will fall below 1 V. Consequently, value of β will fall, resulting in unfaithful amplification.

(ii) During the negative peak of the signal, collector current can at the most be allowed to become zero. As the negative and positive half cycles of the signal are equal, therefore, the change in collector current due to these will also be equal but in opposite direction.

∴ Minimum zero signal collector current required = 2 mA/2 = **1 mA**

During the positive peak of the signal [point *A* in Fig. 9.5 (*ii*)], $i_C = 1 + 1 = 2$mA and during the negative peak (point *B*),

$$i_C = 1 - 1 = 0 \text{ mA}$$

Example 9.2. *A transistor employs a 4 kΩ load and V_{CC} = 13V. What is the maximum input signal if β = 100 ? Given V_{knee} = 1V and a change of 1V in V_{BE} causes a change of 5mA in collector current.*

Solution.

Collector supply voltage, $V_{CC} = 13$ V

Knee voltage, $V_{knee} = 1$ V

Collector load, $R_C = 4$ kΩ

∴ Max. allowed voltage across $R_C = 13 - 1 = 12$ V

∴ Max. allowed collector current, $i_C = \dfrac{12 \text{ V}}{R_C} = \dfrac{12 \text{ V}}{4 \text{ k}\Omega} = 3$ mA

Maximum base current, $i_B = \dfrac{i_C}{\beta} = \dfrac{3 \text{ mA}}{100} = 30$ μA

Now $\dfrac{\text{Collector current}}{\text{Base voltage (signal voltage)}} = 5$ mA/V

∴ Base voltage (signal voltage) $= \dfrac{\text{Collector current}}{5 \text{ mA/V}} = \dfrac{3 \text{ mA}}{5 \text{ mA/V}} =$ **600 mV**

9.3 Inherent Variations of Transistor Parameters

In practice, the transistor parameters such as β, V_{BE} are not the same for every transistor even of the same type. To give an example, BC147 is a silicon *npn* transistor with β varying from 100 to 600 *i.e.* β for one transistor may be 100 and for the other it may be 600, although both of them are *BC*147.

This large variation in parameters is a characteristic of transistors. The major reason for these variations is that transistor is a new device and manufacturing techniques have not too much advanced. For instance, it has not been possible to control the base width and it may vary, although slightly, from one transistor to the other even of the same type. Such small variations result in large change in transistor parameters such as β, V_{BE} etc.

Transistor

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification. It is, therefore, very important that biasing network be so designed that it should be able to work with all transistors of one type whatever may be the spread in β or V_{BE}. In other words, the operating point should be independent of transistor parameters variations.

9.4 Stabilisation

The collector current in a transistor changes rapidly when

(i) the temperature changes,

(ii) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation.

The process of making operating point independent of temperature changes or variations in transistor parameters is known as **stabilisation.**

Once stabilisation is done, the zero signal I_C and V_{CE} become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(i) Temperature dependence of I_C

(ii) Individual variations

(iii) Thermal runaway

(i) **Temperature dependence of I_C.** The collector current I_C for CE circuit is given by:

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant inspite of temperature variations.

(ii) **Individual variations.** The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold I_C constant irrespective of individual variations in transistor parameters.

(iii) **Thermal runaway.** The collector current for a *CE* configuration is given by :

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad ...(i)$$

The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from exp. (*i*) that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1)\, I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out.

The self-destruction of an unstabilised transistor is known as **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e.* I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

9.5 Essentials of a Transistor Biasing Circuit

It has already been discussed that transistor biasing is required for faithful amplification. The biasing network associated with the transistor should meet the following requirements :

(i) It should ensure proper zero signal collector current.

(ii) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(iii) It should ensure the stabilisation of operating point.

9.6 Stability Factor

It is desirable and necessary to keep I_C constant in the face of variations of I_{CBO} (sometimes represented as I_{CO}). The extent to which a biasing circuit is successful in achieving this goal is measured by stability factor *S*. It is defined as under :

*The rate of change of collector current I_C w.r.t. the collector leakage current *I_{CO} at constant β and I_B is called* **stability factor** *i.e.*

$$\text{Stability factor, } S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}. Thus a stability factor 50 of a circuit means that I_C changes 50 times as much as any change in I_{CO}. In order to achieve greater thermal stability, it is desirable to have as low stability factor as possible. The ideal value of *S* is 1 but it is never possible to achieve it in practice. Experience shows that values of S exceeding 25 result in unsatisfactory performance.

The general expression of stability factor for a C.E. configuration can be obtained as under:

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

** Differentiating above expression *w.r.t.* I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

or
$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad \left[\because \frac{dI_{CO}}{dI_C} = \frac{1}{S}\right]$$

or
$$S = \frac{\beta + 1}{1 - \beta\left(\dfrac{dI_B}{dI_C}\right)}$$

* $I_{CBO} = I_{CO}$ = collector leakage current in *CB* arrangement

** Assuming β to be independent of I_C.

9.7 Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery V_{BB} which was separate from the battery V_{CC} used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* V_{CC}). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* V_{CC}) :

(i) Base resistor method

(ii) Emitter bias method

(iii) Biasing with collector-feedback resistor

(iv) Voltage-divider bias

In all these methods, the same basic principle is employed *i.e.* required value of base current (and hence I_C) is obtained from V_{CC} in the zero signal conditions. The value of collector load R_C is selected keeping in view that V_{CE} should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors.

For example, if $\beta = 100$ and the zero signal collector current I_C is to be set at 1mA, then I_B is made equal to $I_C/\beta = 1/100 = 10\ \mu A$. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

9.8 Base Resistor Method

In this method, a high resistance R_B (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig. 9.6) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by V_{CC} and it flows through R_B. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current I_B (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor R_B.

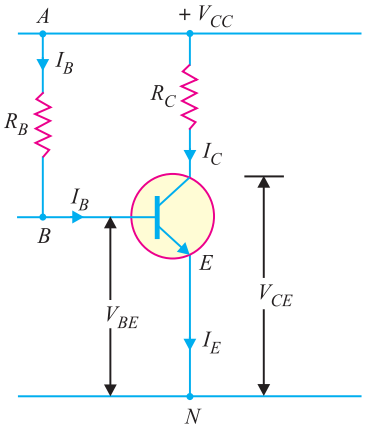


Fig. 9.6

Circuit analysis. It is required to find the value of R_B so that required collector current flows in the zero signal conditions. Let I_C be the required zero signal collector current.

$$\therefore \qquad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or $$I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \qquad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \ldots (i)$$

As V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual, therefore, value of R_B can be readily found from exp. (*i*).

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known quantity and I_B is chosen at some suitable value. Hence, R_B can always be found directly, and for this reason, this method is sometimes called *fixed-bias method.*

Stability factor. As shown in Art. 9.6,

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, I_B is independent of I_C so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that I_C changes $(\beta + 1)$ times as much as any change in I_{CO}. For instance, if $\beta = 100$, then $S = 101$ which means that I_C increases 101 times faster than I_{CO}. Due to the large value of S in a fixed bias, it has poor thermal stability.

Advantages :

(*i*) This biasing circuit is very simple as only one resistance R_B is required.

(*ii*) Biasing conditions can easily be set and the calculations are simple.

(*iii*) There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

Disadvantages :

(*i*) This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if β increases due to transistor replacement, then I_C also increases by the same factor as I_B is constant.

(*ii*) The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

Example 9.3. *Fig. 9.7 (i) shows biasing with base resistor method. (i) Determine the collector current I_C and collector-emitter voltage V_{CE}. Neglect small base-emitter voltage. Given that $\beta = 50$.*

(ii) If R_B in this circuit is changed to 50 kΩ, find the new operating point.

Solution.

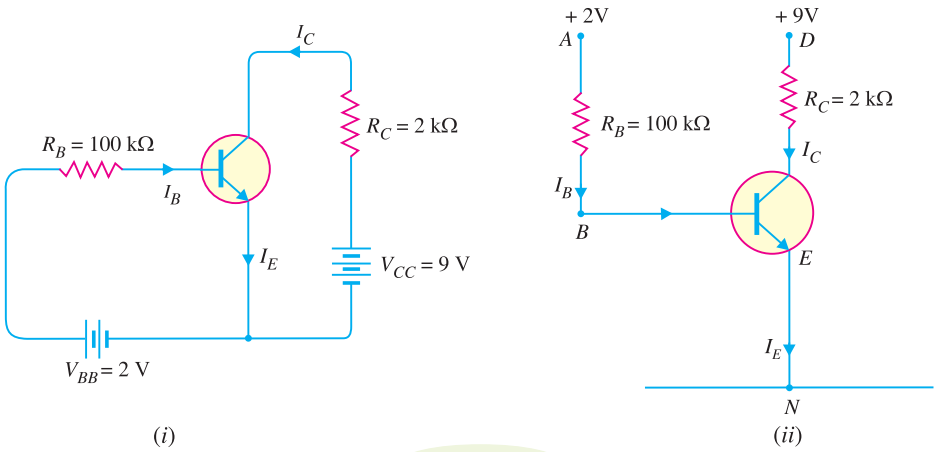


Fig. 9.7

In the circuit shown in Fig. 9.7 (*i*), biasing is provided by a battery V_{BB} (= 2V) in the base circuit which is separate from the battery V_{CC} (= 9V) used in the output circuit. The same circuit is shown in a simplified way in Fig. 9.7 (*ii*). Here, we need show only the supply voltages, + 2V and + 9V. It may be noted that negative terminals of the power supplies are grounded to get a complete path of current.

(*i*) Referring to Fig.9.7 (*ii*) and applying Kirchhoff 's voltage law to the circuit *ABEN*, we get,

$$I_B R_B + V_{BE} = 2\text{ V}$$

As V_{BE} is negligible,

$$\therefore \quad I_B = \frac{2\text{V}}{R_B} = \frac{2\text{V}}{100\text{ k}\Omega} = 20\ \mu\text{A}$$

$$\text{Collector current, } I_C = \beta I_B = 50 \times 20\ \mu\text{ A} = 1000\ \mu\text{ A} = \mathbf{1\ mA}$$

Applying Kirchhoff's voltage law to the circuit *DEN*, we get,

$$I_C R_C + V_{CE} = 9$$

or $$1\text{ mA} \times 2\text{ k}\Omega + V_{CE} = 9$$

or $$V_{CE} = 9 - 2 = \mathbf{7\ V}$$

(*ii*) When R_B is made equal to 50 kΩ, then it is easy to see that base current is doubled *i.e.* $I_B = 40\ \mu\text{A}$.

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 40 = 2000\ \mu\text{ A} = 2\text{ mA}$$

$$\text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 9 - 2\text{ mA} \times 2\text{ k}\Omega = 5\text{ V}$$

∴ New operating point is **5 V, 2 mA.**

Example 9.4. *Fig. 9.8 (i) shows that a silicon transistor with* β = *100 is biased by base resistor method. Draw the d.c. load line and determine the operating point. What is the stability factor* ?

Solution. $V_{CC} = 6\text{ V}, R_B = 530\text{ k}\Omega, R_C = 2\text{ k}\Omega$

D.C. load line. Referring to Fig. 9.8 (*i*), $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $V_{CE} = V_{CC} = 6$ V. This locates the first point B (OB = 6V) of the load line on collector-emitter voltage axis as shown in Fig. 9.8 (*ii*).

When $V_{CE} = 0$, $I_C = V_{CC}/R_C = 6\text{V}/2\text{ k}\Omega = 3$ mA. This locates the second point A (OA = 3mA) of the load line on the collector current axis. By joining points A and B, d.c. load line AB is constructed [See Fig. 9.8 (*ii*)].

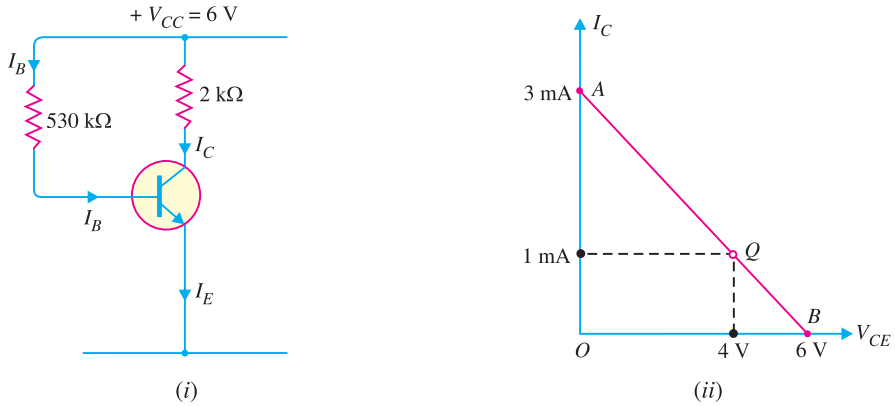


Fig. 9.8

Operating point Q. As it is a silicon transistor, therefore, $V_{BE} = 0.7$V. Referring to Fig. 9.8 (*i*), it is clear that :

$$I_B R_B + V_{BE} = V_{CC}$$

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{(6 - 0.7)\text{ V}}{530\text{ k}\Omega} = 10\ \mu\text{A}$$

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 10 = 1000\ \mu\text{A} = 1\text{ mA}$

Collector-emitter voltage, $V_{CE} = V_{CC} - I_C R_C = 6 - 1\text{ mA} \times 2\text{ k}\Omega = 6 - 2 = 4\text{ V}$

$\therefore$ Operating point is **4 V, 1 mA.**

Fig. 9.8 (*ii*) shows the operating point Q on the d.c. load line. Its co-ordinates are $I_C = 1$mA and $V_{CE} = 4$V.

Stability factor $= \beta + 1 = 100 + 1 =$ **101**

Example 9.5. *(i) A germanium transistor is to be operated at zero signal $I_C = 1$mA. If the collector supply $V_{CC} = 12$V, what is the value of R_B in the base resistor method ? Take $\beta = 100$.*

(ii) If another transistor of the same batch with $\beta = 50$ is used, what will be the new value of zero signal I_C for the same R_B ?

Solution. $V_{CC} = 12$ V, $\beta = 100$

As it is a *Ge* transistor, therefore,

$V_{BE} = 0.3$ V

(*i*) Zero signal $I_C = 1$ mA

$\therefore$ Zero signal $I_B = I_C/\beta = 1\text{ mA}/100 = 0.01$ mA

Using the relation, $V_{CC} = I_B R_B + V_{BE}$

$\therefore$ $$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.3}{0.01\text{ mA}}$$

$= 11.7\text{ V}/0.01\text{ mA} =$ **1170 kΩ**

(*ii*) Now $\beta = 50$

Again using the relation, $V_{CC} = I_B R_B + V_{BE}$

$\therefore$ $$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.3}{1170\text{ k}\Omega}$$

$= 11.7\text{ V}/1170\text{ k}\Omega = 0.01$ mA

$\therefore$ Zero signal $I_C = \beta I_B = 50 \times 0.01 =$ **0.5 mA**

Comments. It is clear from the above example that with the change in transistor parameter β, the zero signal collector current has changed from 1mA to 0.5mA. Therefore, base resistor method cannot provide stabilisation.

Example 9.6. *Calculate the values of three currents in the circuit shown in Fig. 9.9.*

Solution. Applying Kirchhoff's voltage law to the base side and taking resistances in kΩ and currents in mA, we have,

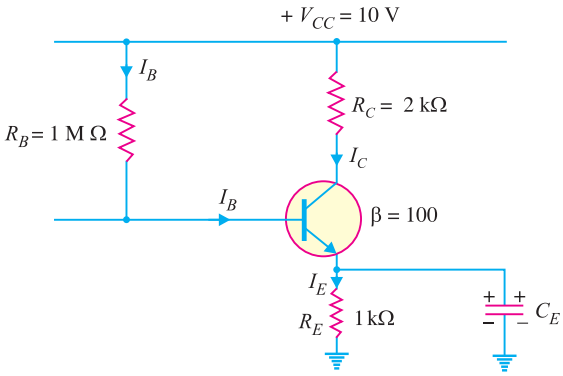


Fig. 9.9

$$V_{CC} = I_B R_B + V_{BE} + I_E \times 1$$

or $$10 = 1000\, I_B + *0 + (I_C + I_B)$$

or $$10 = 1000\, I_B + (\beta\, I_B + I_B)$$

or $$10 = 1000\, I_B + (100\, I_B + I_B)$$

or $$10 = 1101\, I_B$$

$\therefore$ $$I_B = 10/1101 = \mathbf{0.0091\ mA}$$

$$I_C = \beta\, I_B = 100 \times 0.0091 = \mathbf{0.91\ mA}$$

$$I_E = I_C + I_B = 0.91 + 0.0091 = \mathbf{0.919\ mA}$$

Example 9.7. *Design base resistor bias circuit for a CE amplifier such that operating point is V_{CE} = 8V and I_C = 2 mA. You are supplied with a fixed 15V d.c. supply and a silicon transistor with β = 100. Take base-emitter voltage V_{BE} = 0.6V. Calculate also the value of load resistance that would be employed.*

Solution. Fig. 9.10 shows *CE* amplifier using base resistor method of biasing.

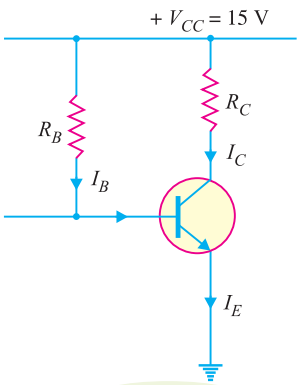


Fig. 9.10

$$V_{CC} = 15\ \text{V};\ \beta = 100;\ V_{BE} = 0.6\text{V}$$

$$V_{CE} = 8\ \text{V};\ I_C = 2\ \text{mA};\ R_C = ?;\ R_B = ?$$

$$V_{CC} = V_{CE} + I_C R_C$$

or $$15\ \text{V} = 8\ \text{V} + 2\ \text{mA} \times R_C$$

$\therefore$ $$R_C = \frac{(15 - 8)\ \text{V}}{2\text{mA}} = \mathbf{3.5\ k\Omega}$$

$$I_B = I_C/\beta = 2/100 = 0.02\ \text{mA}$$

$$V_{CC} = I_B R_B + V_{BE}$$

* Neglecting V_{BE} as it is generally very small.

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{(15 - 0.6)\ \text{V}}{0.02\ \text{mA}} = \mathbf{720\ k\Omega}$$

Example 9.8. *A *base bias circuit in Fig. 9.11 is subjected to an increase in temperature from 25°C to 75°C. If β = 100 at 25°C and 150 at 75°C, determine the percentage change in Q-point values (V_{CE} and I_C) over this temperature range. Neglect any change in V_{BE} and the effects of any leakage current.*

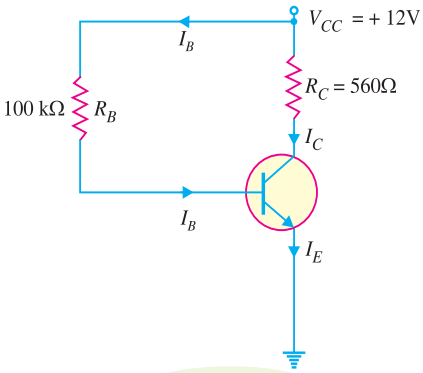


Fig. 9.11

Solution.

At 25°C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12\ V - 0.7\ V}{100\ k\Omega} = 0.113\ \text{mA}$$

$$\therefore \quad I_C = \beta I_B = 100 \times 0.113\ \text{mA} = 11.3\ \text{mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (11.3\ \text{mA})\ (560\Omega) = 5.67\text{V}$$

At 75 °C

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{100\ \text{k}\Omega} = 0.113\ \text{mA}$$

$$\therefore \quad I_C = \beta I_B = 150 \times 0.113\ \text{mA} = 17\ \text{mA}$$

and $$V_{CE} = V_{CC} - I_C R_C = 12\text{V} - (17\ \text{mA})\ (560\ \Omega) = 2.48\text{V}$$

$$\%\text{age change in } I_C = \frac{I_{C\,(75°C)} - I_{C\,(25°C)}}{I_{C\,(25°C)}} \times 100$$

$$= \frac{17\ \text{mA} - 11.3\ \text{mA}}{11.3\ \text{mA}} \times 100 = \mathbf{50\%}\ \textit{(increase)}$$

Note that I_C changes by the same percentage as β.

$$\%\text{age change in } V_{CE} = \frac{V_{CE\,(75°C)} - V_{CE\,(25°C)}}{V_{CE\,(25°C)}} \times 100$$

$$= \frac{2.48\text{V} - 5.67\text{V}}{5.67\text{V}} \times 100 = \mathbf{-56.3\%}\ \textit{(decrease)}$$

Comments. It is clear from the above example that Q-point is extremely dependent on β in a base bias circuit. Therefore, base bias circuit is very unstable. Consequently, this method is normally not used if linear operation is required. However, it can be used for switching operation.

Example 9.9. *In base bias method, how Q-point is affected by changes in V_{BE} and I_{CBO}.*

Solution. In addition to being affected by change in β, the Q-point is also affected by changes in V_{BE} and I_{CBO} in the base bias method.

(*i*) Effect of V_{BE}. The base-emitter-voltage V_{BE} decreases with the increase in temperature (and vice-versa). The expression for I_B in base bias method is given by ;

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* Note that base resistor method is also called *base bias method.*

It is clear that decrease in V_{BE} increases I_B. This will shift the Q-point ($I_C = \beta I_B$ and $V_{CE} = V_{CC} - I_C R_C$). The effect of change in V_{BE} is negligible if $V_{CC} >> V_{BE}$ (V_{CC} atleast 10 times greater than V_{BE}).

(ii) Effect of I_{CBO}. The reverse leakage current I_{CBO} has the effect of decreasing the net base current and thus increasing the base voltage. It is because the flow of I_{CBO} creates a voltage drop across R_B that adds to the base voltage as shown in Fig. 9.12. Therefore, change in I_{CBO} shifts the Q-point of the base bias circuit. However, in modern transistors, I_{CBO} is usually less than 100 nA and its effect on the bias is negligible if $V_{BB} >> I_{CBO} R_B$.

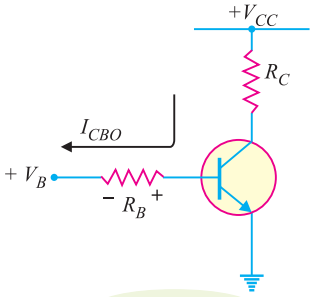


Fig. 9.12

Example 9.10. *Fig. 9.13 (i) shows the base resistor transistor circuit. The device (i.e. transistor) has the characteristics shown in Fig. 9.13 (ii). Determine V_{CC}, R_C and R_B.*

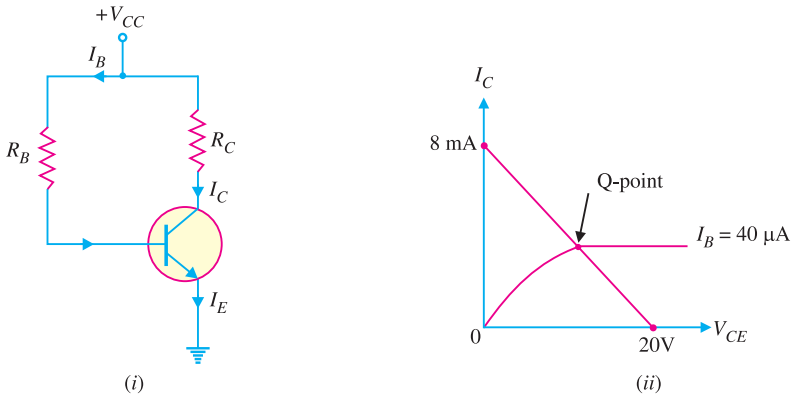


Fig. 9.13

Solution. From the d.c load line, $V_{CC} = 20\text{V}$.

$$\text{Max. } I_C = \frac{V_{CC}}{R_C} \quad (\text{when } V_{CE} = 0\text{V})$$

$$\therefore \quad R_C = \frac{V_{CC}}{\text{Max. } I_C} = \frac{20\text{V}}{8\text{mA}} = 2.5\ \text{k}\Omega$$

$$\text{Now} \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\text{V} - 0.7\text{V}}{40\ \mu\text{A}} = \frac{19.3\text{V}}{40\ \mu\text{A}} = 482.5\ \text{k}\Omega$$

Example 9.11. *What fault is indicated in (i) Fig. 9.14 (i) and (ii) Fig. 9.14 (ii) ?*

Solution.

(i) The obvious fault in Fig. 9.14 (*i*) is that the **base is internally open.** It is because 3V at the base and 9V at the collector mean that transistor is in cut-off state.

(ii) The obvious fault in Fig. 9.14 (*ii*) is that **collector is internally open.** The voltage at the base is correct. The voltage of 9V appears at the collector because the 'open' prevents collector current.

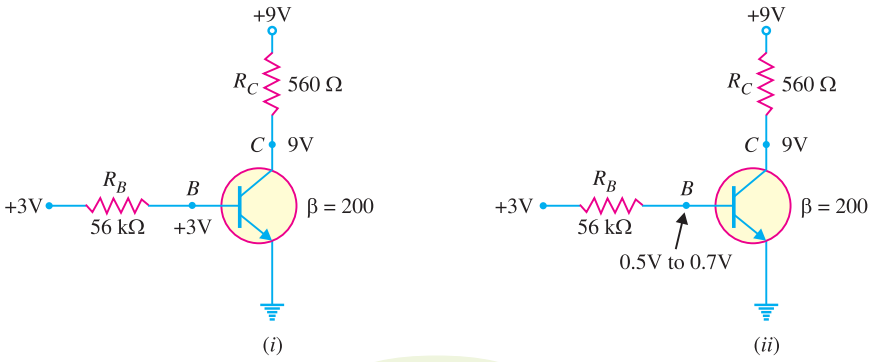


Fig. 9.14

9.9 Emitter Bias Circuit

Fig. 9.15 shows the emitter bias circuit. This circuit differs from base-bias circuit in two important respects. First, it uses two separate d.c. voltage sources ; one positive ($+V_{CC}$) and the other negative ($-V_{EE}$). Normally, the two supply voltages will be equal. For example, if $V_{CC} = +20$V (d.c.), then $V_{EE} = -20$V (d.c.). Secondly, there is a resistor R_E in the emitter circuit.

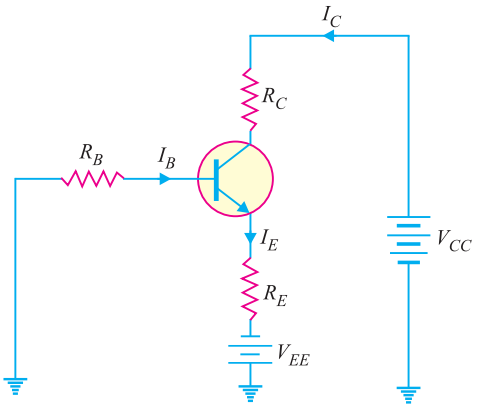


Fig. 9.15

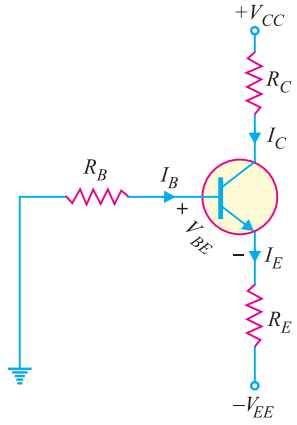


Fig. 9.16

We shall first redraw the circuit in Fig. 9.15 as it usually appears on schematic diagrams. This means deleting the battery symbols as shown in Fig. 9.16. All the information is still (See Fig. 9.16) on the diagram except that it is in condensed form. That is a negative supply voltage $-V_{EE}$ is applied to the bottom of R_E and a positive voltage of $+V_{CC}$ to the top of R_C.

9.10 Circuit Analysis of Emitter Bias

Fig. 9.16 shows the emitter bias circuit. We shall find the Q-point values (*i.e.* d.c. I_C and d.c. V_{CE}) for this circuit.

(*i*) Collector current (I_C). Applying Kirchhoff's voltage law to the base-emitter circuit in Fig. 9.16, we have,

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$\therefore \quad V_{EE} = I_B R_B + V_{BE} + I_E R_E$$

Now $I_C \simeq I_E$ and $I_C = \beta I_B \quad \therefore I_B \simeq \dfrac{I_E}{\beta}$

Putting $I_B = I_E/\beta$ in the above equation, we have,

$$V_{EE} = \left(\frac{I_E}{\beta}\right) R_B + I_E R_E + V_{BE}$$

or $$V_{EE} - V_{BE} = I_E (R_B/\beta + R_E)$$

$$\therefore \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

Since $I_C \simeq I_E$, we have,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

***(ii)* Collector-emitter voltage (V_{CE}).** Fig. 9.17 shows the various voltages of the emitter bias circuit w.r.t. ground.

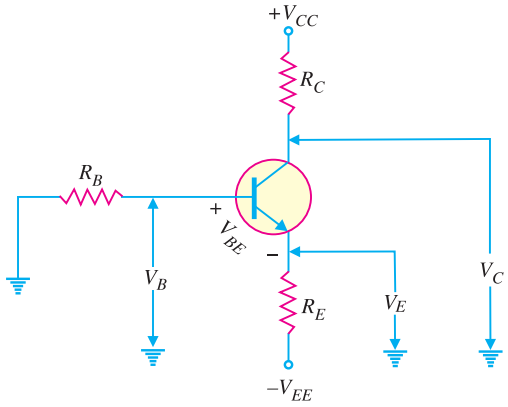


Fig. 9.17

Emitter voltage w.r.t. ground is

$$V_E = -V_{EE} + I_E R_E$$

Base voltage w.r.t. ground is

$$V_B = V_E + V_{BE}$$

Collector voltage w.r.t. ground is

$$V_C = V_{CC} - I_C R_C$$

Subtracting V_E from V_C and using the approximation $I_C \simeq I_E$, we have,

$$V_C - V_E = (V_{CC} - I_C R_C) - (-V_{EE} + I_C R_E) \qquad (\because I_E \simeq I_C)$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Alternatively. Applying Kirchhoff's voltage law to the collector side of the emitter bias circuit in Fig. 9.16 (Refer back), we have,

$$V_{CC} - I_C R_C - V_{CE} - I_C{}^{*} R_E + V_{EE} = 0$$

or $$V_{CE} = V_{CC} + V_{EE} - I_C (R_C + R_E)$$

Stability of Emitter bias. The expression for collector current I_C for the emitter bias circuit is given by ;

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

* $I_C \simeq I_E$

It is clear that I_C is dependent on V_{BE} and β, both of which change with temperature.

If $R_E >> R_B/\beta$, then expression for I_C becomes :

$$I_C = \frac{V_{EE} - V_{BE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of β.

If $V_{EE} >> V_{BE}$, then I_C becomes :

$$I_C (\simeq I_E) = \frac{V_{EE}}{R_E}$$

This condition makes $I_C (\simeq I_E)$ independent of V_{BE}.

If $I_C (\simeq I_E)$ is independent of β and V_{BE}, the Q-point is not affected appreciably by the variations in these parameters. Thus emitter bias can provide stable Q-point if properly designed.

Example 9.12. *For the emitter bias circuit shown in Fig. 9.18, find I_E, I_C, V_C and V_{CE} for $\beta = 85$ and $V_{BE} = 0.7V$.*

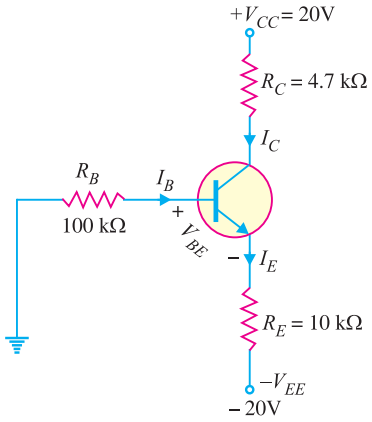


Fig. 9.18

Solution.

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.7V}{10\ k\Omega + 100\ k\Omega/85} = \mathbf{1.73\ mA}$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.73\ mA)\ (4.7\ k\Omega) = \mathbf{11.9V}$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.73\ mA)\ (10\ k\Omega) = -2.7V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.9 - (-2.7V) = \mathbf{14.6V}$$

Note that operating point (or Q – point) of the circuit is 14.6V, 1.73 mA.

Example 9.13. *Determine how much the Q-point in Fig. 9.18 (above) will change over a temperature range where β increases from 85 to 100 and V_{BE} decreases from 0.7V to 0.6V.*

Solution.

For β = 85 and $V_{BE} = 0.7V$

As calculated in the above example, $I_C = 1.73$ mA and $V_{CE} = 14.6V$.

For β = 100 and $V_{BE} = 0.6V$

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta} = \frac{20V - 0.6V}{10\ k\Omega + 100\ k\Omega/100} = \frac{19.4V}{11\ k\Omega} = 1.76\ mA$$

$$V_C = V_{CC} - I_C R_C = 20V - (1.76\ mA)\ (4.7\ k\Omega) = 11.7V$$

$$V_E = -V_{EE} + I_E R_E = -20V + (1.76\ mA)\ (10\ k\Omega) = -2.4V$$

$$\therefore \quad V_{CE} = V_C - V_E = 11.7 - (-2.4) = 14.1\text{V}$$

$$\text{\% age change in } I_C = \frac{1.76\text{ mA} - 1.73\text{ mA}}{1.73\text{ mA}} \times 100 = \textbf{1.7\%} \textit{ (increase)}$$

$$\text{\% age change in } V_{CE} = \frac{14.1\text{V} - 14.6\text{V}}{14.1\text{V}} \times 100 = \textbf{– 3.5\%} \textit{ (decrease)}$$

9.11 Biasing with Collector Feedback Resistor

In this method, one end of R_B is connected to the base and the other end to the collector as shown in Fig. 9.19. Here, the required zero signal base current is determined *not* by V_{CC} but by the collector-base voltage V_{CB}. It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

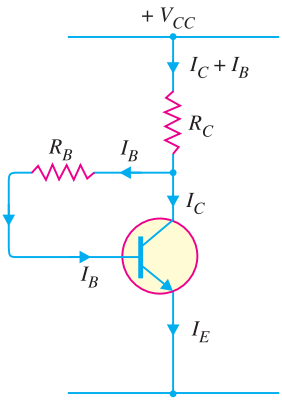


Fig. 9.19

Circuit analysis. The required value of R_B needed to give the zero signal current I_C can be determined as follows. Referring to Fig. 9.19,

$$V_{CC} = {}^*I_C R_C + I_B R_B + V_{BE}$$

or
$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta\, I_B R_C}{I_B} \quad (\because I_C = \beta\, I_B)$$

Alternatively, $V_{CE} = V_{BE} + V_{CB}$

or $V_{CB} = V_{CE} - V_{BE}$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}; \quad \text{where} \quad I_B = \frac{I_C}{\beta}$$

It can be shown mathematically that stability factor S for this method of biasing is less than $(\beta + 1)$ *i.e.*

Stability factor, $S < (\beta + 1)$

Therefore, this method provides better thermal stability than the fixed bias.

Note. It can be easily proved (See **example 9.17) that Q-point values (I_C and V_{CE}) for the circuit shown in Fig. 9.19 are given by ;

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C}$$

and $V_{CE} = V_{CC} - I_C R_C$

Advantages

(*i*) It is a simple method as it requires only one resistance R_B.

(*ii*) This circuit provides some stabilisation of the operating point as discussed below :

$$V_{CE} = V_{BE} + V_{CB}$$

* Actually voltage drop across $R_C = (I_B + I_C)\, R_C$.
However, $I_B << I_C$. Therefore, as a reasonable approximation, we can say that drop across $R_C = I_C R_C$.

** Put $R_E = 0$ for the expression of I_C in exmaple 9.17. It is because in the present circuit (Fig. 9.19), there is no R_E.

Suppose the temperature increases. This will increase collector leakage current and hence the total collector current. But as soon as collector current increases, V_{CE} decreases due to greater drop across R_C. The result is that V_{CB} decreases *i.e.* lesser voltage is available across R_B. Hence the base current I_B decreases. The smaller I_B tends to decrease the collector current to original value.

Disadvantages

(*i*) The circuit does not provide good stabilisation because stability factor is fairly high, though it is lesser than that of fixed bias. Therefore, the operating point does change, although to lesser extent, due to temperature variations and other effects.

(*ii*) This circuit provides a negative feedback which reduces the gain of the amplifier as explained hereafter. During the positive half-cycle of the signal, the collector current increases. The increased collector current would result in greater voltage drop across R_C. This will reduce the base current and hence collector current.

Example 9.14. *Fig. 9.20 shows a silicon transistor biased by collector feedback resistor method. Determine the operating point. Given that* $\beta = 100$.

Solution. $V_{CC} = 20\text{V}, R_B = 100\ \text{k}\Omega, R_C = 1\text{k}\Omega$

Since it is a silicon transistor, $V_{BE} = 0.7$ V.

Assuming I_B to be in mA and using the relation,

$$R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

or $100 \times I_B = 20 - 0.7 - 100 \times I_B \times 1$

or $200\ I_B = 19.3$

or $I_B = \frac{19.3}{200} = 0.096$ mA

$\therefore$ Collector current, $I_C = \beta I_B = 100 \times 0.096 = 9.6$ mA

Collector-emitter voltage is

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 20 - 9.6\ \text{mA} \times 1\ \text{k}\Omega$$
$$= 10.4\ \text{V}$$

$\therefore$ Operating point is **10.4 V, 9.6 mA.**

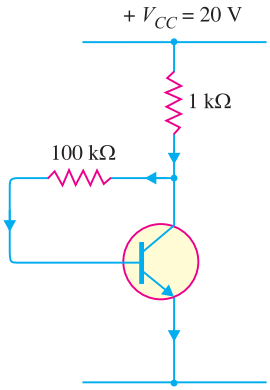


Fig. 9.20

Alternatively

$$I_C = \frac{V_{CC} - V_{BE}}{R_B/\beta + R_C} = \frac{20\text{V} - 0.7\text{V}}{100\ \text{k}\Omega/100 + 1\ \text{k}\Omega} = \frac{19.3\text{V}}{2\ \text{k}\Omega} = \mathbf{9.65\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{V} - 9.65\ \text{mA} \times 1\ \text{k}\Omega = \mathbf{10.35V}$$

A very slight difference in the values is due to manipulation of calculations.

Example 9.15. *(i) It is required to set the operating point by biasing with collector feedback resistor at* $I_C = 1$*mA,* $V_{CE} = 8$*V. If* $\beta = 100$*,* $V_{CC} = 12$*V,* $V_{BE} = 0.3$*V, how will you do it ?*

(*ii*) *What will be the new operating point if* $\beta = 50$*, all other circuit values remaining the same ?*

Solution. $V_{CC} = 12\text{V}, V_{CE} = 8\text{V}, I_C = 1\text{mA}$

$\beta = 100, V_{BE} = 0.3\text{V}$

(*i*) To obtain the required operating point, we should find the value of R_B.

Now, collector load is

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{(12 - 8)\text{ V}}{1\text{ mA}} = 4\text{ k}\Omega$$

$$\text{Also } I_B = \frac{I_C}{\beta} = \frac{1\text{ mA}}{100} = 0.01\text{ mA}$$

$$\text{Using the relation, } R_B = \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

$$= \frac{12 - 0.3 - 100 \times 0.01 \times 4}{0.01} = \mathbf{770\ k\Omega}$$

(ii) Now $\beta = 50$, and other circuit values remain the same.

$$\therefore \quad V_{CC} = V_{BE} + I_B R_B + \beta I_B R_C$$

$$\text{or} \quad 12 = 0.3 + I_B (R_B + \beta R_C)$$

$$\text{or} \quad 11.7 = I_B (770 + 50 \times 4)$$

$$\text{or} \quad I_B = \frac{11.7\text{ V}}{970\text{ k}\Omega} = 0.012\text{ mA}$$

$$\therefore \quad \text{Collector current, } I_C = \beta I_B = 50 \times 0.012 = 0.6\text{ mA}$$

$$\therefore \quad \text{Collector-emitter voltage, } V_{CE} = V_{CC} - I_C R_C = 12 - 0.6\text{ mA} \times 4\text{ k}\Omega = 9.6\text{ V}$$

$\therefore$ New operating point is **9.6 V, 0.6 mA.**

Comments. It may be seen that operating point is changed when a new transistor with lesser β is used. Therefore, biasing with collector feedback resistor does not provide very good stabilisation. It may be noted, however, that change in operating point is less than that of base resistor method.

Example 9.16. *It is desired to set the operating point at 2V, 1mA by biasing a silicon transistor with collector feedback resistor R_B. If $\beta = 100$, find the value of R_B.*

Solution.

For a silicon transistor,

$$V_{BE} = 0.7\text{ V}$$

$$I_B = \frac{I_C}{\beta} = 1/100 = 0.01\text{ mA}$$

$$\text{Now} \quad V_{CE} = V_{BE} + V_{CB}$$

$$\text{or} \quad 2 = 0.7 + V_{CB}$$

$$\therefore \quad V_{CB} = 2 - 0.7 = 1.3\text{ V}$$

$$\therefore \quad R_B = \frac{V_{CB}}{I_B} = \frac{1.3\text{V}}{0.01\text{ mA}} = \mathbf{130\ k\Omega}$$

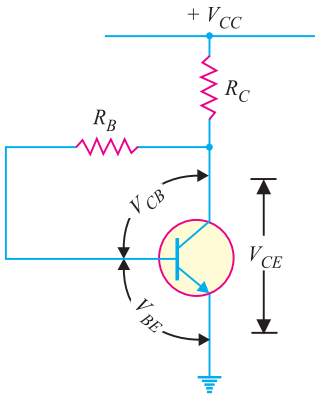


Fig. 9.21

Example 9.17. *Find the Q-point values (I_C and V_{CE}) for the collector feedback bias circuit shown in Fig. 9.22.*

Solution. Fig. 9.22 shows the currents in the three resistors (R_C, R_B and R_E) in the circuit. By following the path through V_{CC}, R_C, R_B, V_{BE} and R_E and applying Kirchhoff's voltage law, we have,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Now $I_B + I_C \simeq I_C$; $I_E \simeq I_C$ and $I_B = \dfrac{I_C}{\beta}$

$\therefore$ $V_{CC} - I_C R_C - \dfrac{I_C}{\beta} R_B - V_{BE} - I_C R_E = 0$

or $I_C \left(R_E + \dfrac{R_B}{\beta} + R_C\right) = V_{CC} - V_{BE}$

$\therefore$ $I_C = \dfrac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$

Putting the given circuit values, we have,

$$I_C = \frac{12\text{V} - 0.7\text{V}}{1\ \text{k}\Omega + 400\ \text{k}\Omega/100 + 4\ \text{k}\Omega}$$

$$= \frac{11.3\text{V}}{9\ \text{k}\Omega} = 1.26\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 12\text{V} - 1.26\ \text{mA}\ (4\text{k}\Omega + 1\ \text{k}\Omega)$$

$$= 12\text{V} - 6.3\text{V} = 5.7\text{V}$$

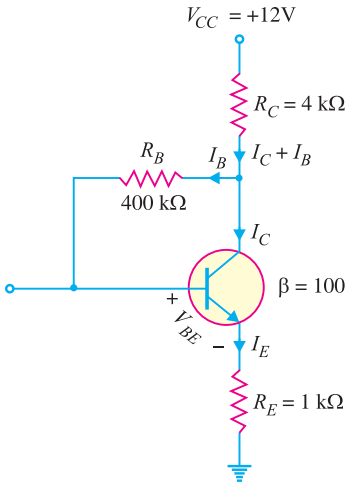


Fig. 9.22

$\therefore$ The operating point is **5.7V, 1.26 mA.**

Example 9.18. *Find the d.c. bias values for the collector-feedback biasing circuit shown in Fig. 9.23. How does the circuit maintain a stable Q point against temperature variations ?*

Solution. The collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{0 + 100\ \text{k}\Omega/100 + 10\ \text{k}\Omega}$$

$$= \frac{9.3\text{V}}{11\ \text{k}\Omega} = 0.845\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10\text{V} - 0.845\ \text{mA} \times 10\ \text{k}\Omega$$

$$= 10\text{V} - 8.45\ \text{V} = 1.55\text{V}$$

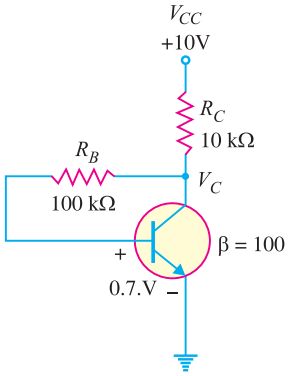


Fig. 9.23

$\therefore$ Operating point is **1.55V, 0.845 mA.**

Stability of Q-point. We know that β varies directly with temperature and V_{BE} varies inversely with temperature. As the temperature goes up, β goes up and V_{BE} goes down. The increase in β increases I_C (= βI_B). The decrease in V_{BE} increases I_B which in turn increases I_C. As I_C tries to increase, the voltage drop across R_C (= $I_C R_C$) also tries to increases. This tends to reduce collector voltage V_C (See Fig. 9.23) and, therefore, the voltage across R_B. The reduced voltage across R_B reduces I_B and offsets the attempted increase in I_C and attempted decrease in V_C. The result is that the collector-feedback circuit maintains a stable Q-point. The reverse action occurs when the temperature decreases.

9.12 Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances R_1 and R_2 are connected across the supply voltage V_{CC} (See Fig. 9.24) and provide biasing. The emitter resistance R_E provides stabilisation. The name "voltage divider" comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-

emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

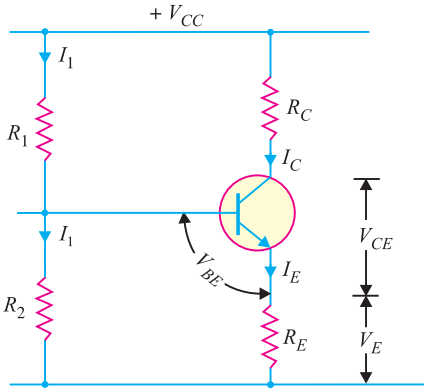


Fig. 9.24

Circuit analysis. Suppose that the current flowing through resistance R_1 is I_1. As base current I_B is very small, therefore, it can be assumed with reasonable accuracy that current flowing through R_2 is also I_1.

(*i*) Collector current I_C :

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$\therefore$ Voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig. 9.24,

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \simeq I_C$

$\therefore$ $$I_C = \frac{V_2 - V_{BE}}{R_E} \quad ...(i)$$

It is clear from exp. (*i*) above that I_C does not at all depend upon β. Though I_C depends upon V_{BE} but in practice $V_2 >> V_{BE}$ so that I_C is practically independent of V_{BE}. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

(*ii*) Collector-emitter voltage V_{CE}. Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Stabilisation. In this circuit, excellent stabilisation is provided by R_E. Consideration of eq. (*i*) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current I_C increases due to rise in temperature. This will cause the voltage drop across emitter resistance R_E to increase. As voltage drop across R_2 (*i.e.* V_2) is *independent of I_C, therefore, V_{BE} decreases. This in turn causes I_B to decrease. The reduced value of I_B tends to restore I_C to the original value.

Stability factor. It can be shown mathematically (See Art. 9.13) that stability factor of the circuit is given by :

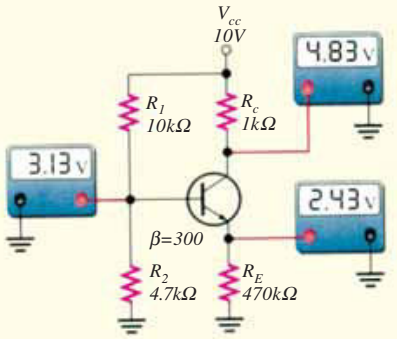
$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \frac{R_0}{R_E}}{\beta + 1 + \frac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio R_0/R_E is very small, then R_0/R_E can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$



A voltage divider biased transistor with correct voltages

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, R_0 / R_E has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

Example 9.19. *Fig. 9.25 (i) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*

Solution.

d.c. load line. The collector-emitter voltage V_{CE} is given by :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15$V. This locates the first point B ($OB = 15$V) of the load line on the collector-emitter voltage axis.

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{(1 + 2)\text{ k}\Omega} = 5 \text{ mA}$$

This locates the second point A ($OA = 5$ mA) of the load line on the collector current axis. By joining points A and B, the d.c. load line AB is constructed as shown in Fig. 9.25 (*ii*).

* Voltage drop across $R_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$

** Low value of R_0 can be obtained by making R_2 very small. But with low value of R_2, current drawn from V_{CC} will be large. This puts restrictions on the choice of R_0. Increasing the value of R_E requires greater V_{CC} in order to maintain the same value of zero signal collector current. Therefore, the ratio R_0/R_E cannot be made very small from design point of view.