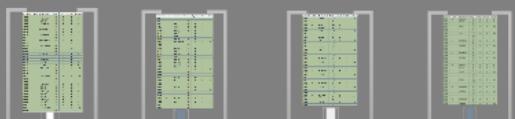


Objective

Digital simulation of the card predictor trick.

Description

Card Predictor as the name says predicts the fifth card out of a set of randomly chosen five cards. Four of these cards are given to the 8085 microprocessor. It computes and outputs both the value as well as the suit of the fifth card.



Indian Institute of Technology, Guwahati



EE 202 Digital Circuits Laboratory
July-Nov 2013

Project report
Lab Group 41

Rahul Ghosh
Ashima Jain

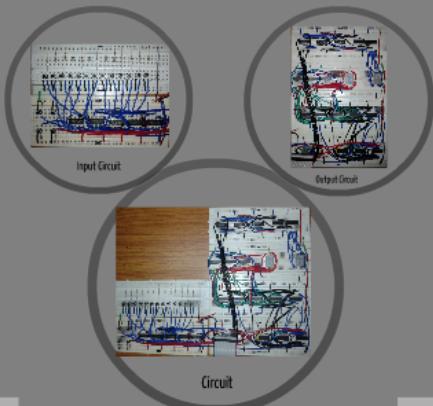
120108027
120108051

Outcome

The circuit worked and the value of the fifth card was predicted correctly.

<http://prezi.com/zcwnabpcmq4/card-predictor/>

Gallery



Indian Institute of Technology, Guwahati



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Address	Label	OpCode	R/M	Reg	Suit
0000	MAIN	00			
0006	MOV PL	66	1	A	2
0008	DEC H	20	1	C	6
000A	MOV A,B	90	2	B	7
000C	OUT CWR	00	2	L	4
000E	DEC H	20	1	C	6
0010	MOV AL,B	90	2	D	7
0012	CALL DELAY	31	3		
0014	MOV PL	66	1	A	2
0016	CALL DELAY	31	3		
0018	MOV AL,C	90	2	D	7
001A	CALL DELAY	31	3		
001C	MOV AL,D	90	2	E	7
001E	CALL DELAY	31	3		
0020	MOV AL,E	90	2	F	7
0022	CALL EXIT	31	3		
0024	END	00			

Address	Label	OpCode	R/M	Reg	Suit
0000	MAIN	00			
0006	MOV PL	66	1	A	2
0008	DEC H	20	1	C	6
000A	MOV A,B	90	2	B	7
000C	MOV AL,B	90	2	D	7
000E	MOV AL,C	90	2	E	7
0010	MOV AL,D	90	2	F	7
0012	MOV AL,E	90	2	G	7
0014	CALL EXIT	31	3		
0016	END	00			

Address	Label	OpCode	R/M	Reg	Suit
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0006	MOV PL	66	1	A	2
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000E	MOV AL,C	90	2	E	7
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000E	MOV AL,C	90	2	E	7
0010	MOV AL,D	90	2	F	7
0012	MOV AL,E	90	2	G	7
0014	CALL EXIT	31	3		
0016	END	00			

Description of Input Circuit

The input circuit consists of two parts :

Suits: Four switches have been provided to input the suit viz. Club, Diamond, Spade and Heart, of the corresponding card.

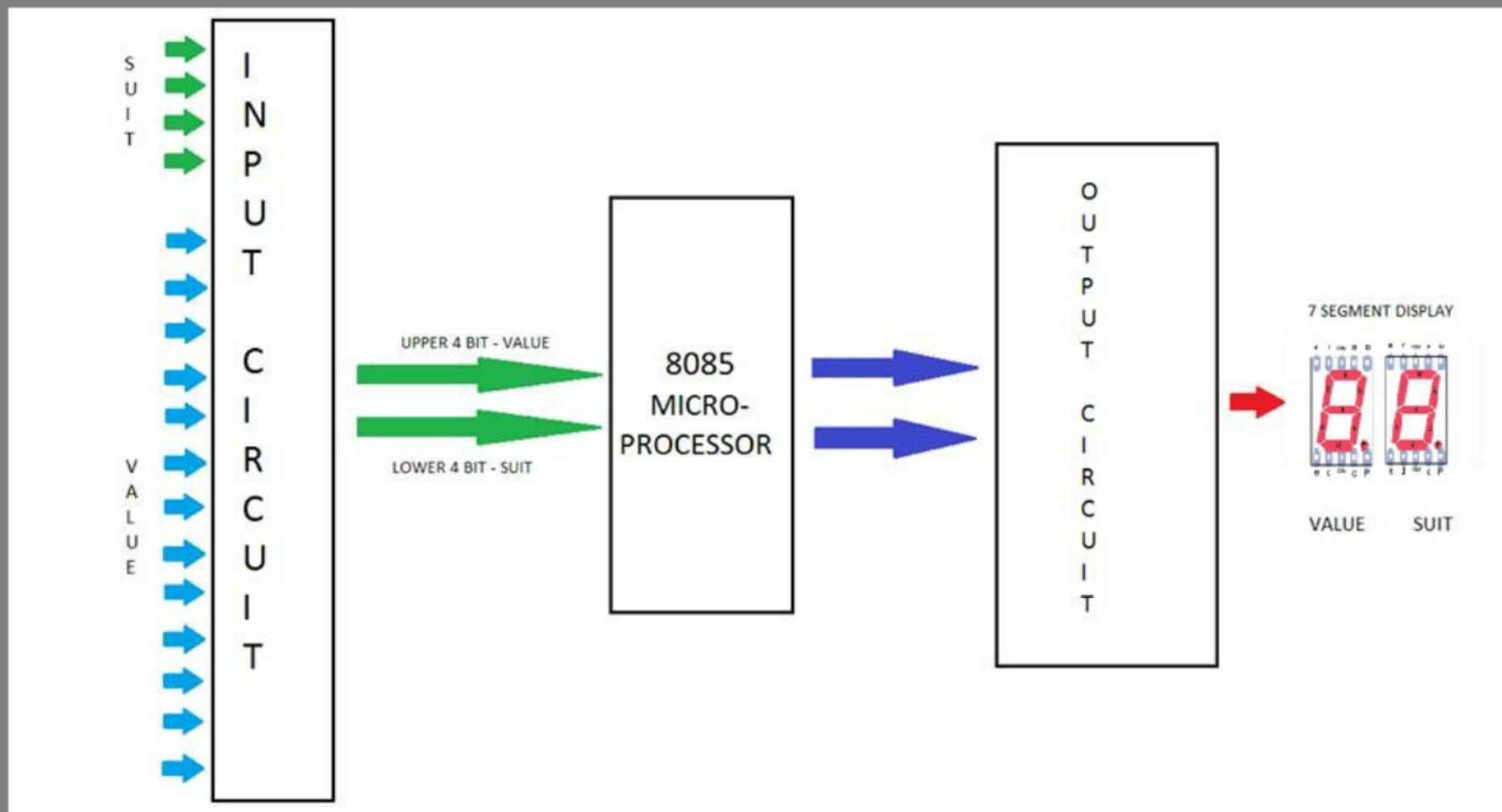
Suits	Hex value
Club	01
Diamond	02
Spade	03
Heart	04

Card Value: For each suit, there are thirteen different possible values(from 2 to 9 and then jack to ace) of a card. So, there are thirteen switches for taking the input of the value of the cards.

Card Value	Hex value
Ace	01
2	02
3	03
4	04
5	05
6	06
7	07
8	08
9	09
10	0A
Jack	0B
Queen	0C
King	0D

Description of Output Circuit

The output to be displayed comprises of both the value as well as the suit of the fifth card. 8085 gives 8 bit input where the upper 4 bits correspond to the value while the lower four to the suit. Two 7-segment displays have been used for displaying the first letter of the suit and the hex value of the card value.



Block Diagram of the circuit

8085 Assembly Code

The upper and lower C ports of 8255 are used as input ports for taking the input of the card value and the suit respectively. Port A is configured as output port. The 8085 code is as follows.

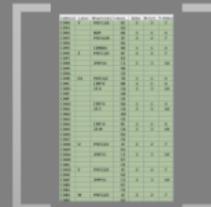
Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C000	DELAY	MVI B,32	06	2	2	7
C001			32			
C002		MVI C,64	0E	2	2	7
C003			64			
C004		MVI D,C8	16	2	2	7
C005			C8			
C006		DCR D	15	1	1	4
C007		JNZ C006	C2	3	3	10
C008			06			
C009			C0			
C00A		DCR C	0D	1	1	4
C00B		JNZ C004	C2	3	3	10
C00C			04			
C00D			C0			
C00E		DCR B	05	1	1	4
C00F		JNZ C002	C2	3	3	10
C010			02			
C011			C0			
C012		RET	C9	1	3	10
C013		MVI E,04	1E	2	2	7
C014			04			
C015		LXI H,D000	21	3	3	10
C016			00			
C017			D0			
C018		MVI A,81	3E	2	2	7
C019			81			
C01A		OUT CWR	D3	1	1	4
C01B			13	1	1	6
C01C		MVI A,FF	3E	2	2	7
C01D			FF			
C01E		OUT PORTB	D3	1	1	4
C01F			11	1	2	7
C020		CALL DELAY	CD	3	5	18
C021			00			
C022			C0			
C023		IN PORTC	DB	1	1	4

Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C024			12	1	1	6
C025		MOV M,A	77	1	2	7
C026		INX H	23	1	1	6
C027		MVI A,88	3E	2	2	7
C028			88			
C029		OUT CWR	D3	1	1	4
C02A			13	1	1	6
C02B		MVI A,00	3E	2	2	7
C02C			00			
C02D		OUT PORTB	D3	1	1	4
C02E			11	2	2	7
C02F		CALL DELAY	CD			
C030			00	2	2	7
C031			C0			
C032		IN PORTC	DB	1	1	4
C033			12	1	2	7
C034		MOV M,A	77	1	2	7
C035		INX H	23	1	1	6
C036		DCR E	1D	1	1	4
C037		JNZ C018	C2	3	3	10
C038			18			
C039			C0			
C03A		LXI H,D002	21	3	3	10
C03B			02			
C03C			D0			
C03D		MOV B,M	46	1	2	7
C03E		INX H	23	1	1	6
C03F		INX H	23	1	1	6
C040		MOV C,M	4E	1	2	7
C041		INX H	23	1	1	6
C042		INX H	23	1	1	6
C043		MOV D,M	56	1	2	7
C044		INX H	23	1	1	6
C045		INX H	23	1	1	6
C046		LXI H,D008	21	3	3	10
C047			08			



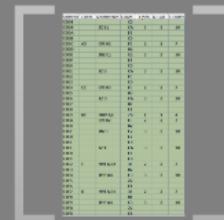
Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C048			D0			
C049		MOV M,B	70	1	2	7
C04A		INX H	23	1	1	6
C04B		MOV M,C	71	1	2	7
C04C		INX H	23	1	1	6
C04D		MOV M,D	72	1	2	7
C04E		MVI B,03	06	2	2	7
C04F			03			
C050	START	LXI H,D008	21	3	3	10
C051			08			
C052			D0			
C053		MVI C,02	0E	2	2	7
C054			02			
C055	BACK	MOV A,M	7E	1	2	7
C056		INX H	23	1	1	6
C057		CMP M	BE	1	2	7
C058		JC SKIP	DA	3	3	10
C059			63			
C05A			C0			
C05B		JZ SKIP	CA	3	3	10
C05C			63			
C05D			C0			
C05E		MOV D,M	56	1	2	7
C05F		MOV M,A	77	1	2	7
C060		DCX H	2B	1	1	6
C061		MOV M,D	72	1	2	7
C062		INX H	23	1	1	6
C063	SKIP	DCR C	0D	1	1	4
C064		JNZ BACK	C2	3	3	10
C065			55			
C066			C0			
C067		DCR B	05	1	1	4
C068		JNZ START	C2	3	3	10
C069			50			
C06A			C0			
C06B		LXI H,D002	21	3	3	10

Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C06C			02			
C06D			D0			
C06E		MOV C,M	4E	1	2	7
C06F		INX H	23	1	1	6
C070		INX H	23	1	1	6
C071		MOV E,M	5E	1	2	7
C072		INX H	23	1	1	6
C073		INX H	23	1	1	6
C074		MOV A,M	7E	1	2	7
C075		LXI H,D008	21	3	3	10
C076			08			
C077			D0			
C078		MOV B,M	46	1	2	7
C079		INX H	23	1	1	6
C07A		MOV D,M	56	1	2	7
C07B		INX H	23	1	1	6
C07C		MOV H,M	66	1	2	7
C07D		MOV L,A	6F	1	1	4
C07E		MOV A,C	79	1	1	4
C07F		CMP B	B8	1	1	4
C080		JZ X	CA	3	3	10
C081			8B			
C082			C0			
C083		CMP D	BA	1	1	4
C084		JZ Y	CA	3	3	10
C085			90			
C086			C0			
C087		CMP H	BC	1	1	4
C088		JZ Z	CA	3	3	10
C089			96			
C08A			C0			
C08B	X	MVI C,01	0E	2	2	7
C08C			01			
C08D		JMP D1	C3	3	3	10
C08E			9B			
C08F			C0			



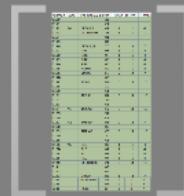
Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C090	Y	MVI C,02	0E	2	2	7
C091			02			
C092		NOP	00	1	1	4
C093		MVI A,06	3E	2	2	7
C094			06			
C095		C09BD1	00	1	1	4
C096	Z	MVI C,03	0E	2	2	7
C097			03			
C098		JMP D1	C3	3	3	10
C099			9B			
C09A			C0			
C09B	D1	MOV A,E	7B	1	1	4
C09C		CMP B	B8	1	1	4
C09D		JZ U	CA	3	3	10
C09E			A8			
C09F			C0			
COA0		CMP D	BA	1	1	4
COA1		JZ V	CA	3	3	10
COA2			AD			
COA3			C0			
COA4		CMP H	BC	1	1	4
COA5		JZ W	CA	3	3	10
COA6			B2			
COA7			C0			
COA8	U	MVI E,01	1E	2	2	7
COA9			01			
COAA		JMP E1	C3	3	3	10
COAB			B7			
COAC			C0			
COAD	V	MVI E,02	1E	2	2	7
COAE			02			
COAF		JMP E1	C3	3	3	10
COBO			B7			
COB1			C0			
COB2	W	MVI E,03	1E	2	2	7
COB3			03			

Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C0B4		JMP E1	C3	3	3	10
C0B5			B7			
C0B6			C0			
C0B7	E1	MOV A,L	7D	1	1	4
C0B8		CMP B	B8	1	1	4
C0B9		JZ P	CA	3	3	10
COBA			C4			
COBB			C0			
COBC		CMP D	BA	1	1	4
COBD		JZ Q	CA	3	3	10
COBE			C9			
COBF			C0			
COC0		CMP H	BC	1	1	4
COC1		JZ R	CA	3	3	10
COC2			CE			
COC3			C0			
COC4	P	MVI L,01	2E	2	2	7
COC5			01			
COC6		JMP F1	C3	3	3	10
COC7			D3			
COC8			C0			
COC9	Q	MVI L,02	2E	2	2	7
COCA			02			
COCB		JMP F1	C3	3	3	10
COCC			D3			
COCD			C0			
COCE	R	MVI L,03	2E	2	2	7
COCF			03			
COD0		JMP F1	C3	3	3	10
COD1			D3			
COD2			C0			
COD3	F1	MOV A,C	79	1	1	4
COD4		CPI 01	FE	2	2	7
COD5			01			
COD6		JNZ A3	C2	3	3	10
COD7			DC			



Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C0D8			C0			
C0D9		JZ B1	CA	3	3	10
C0DA			E9			
C0DB			C0			
C0DC	A3	CPI 02	FE	2	2	7
C0DD			02			
C0DE		JNZ C1	C2	3	3	10
C0DF			E4			
C0E0			C0			
C0E1		JZ G	CA	3	3	10
C0E2			FC			
C0E3			C0			
C0E4	C1	CPI 03	FE	2	2	7
C0E5			03			
C0E6		JZ O	CA	3	3	10
C0E7			0F			
C0E8			C1			
C0E9	B1	MOV A,E	7B	1	1	4
COEA		CPI 02	FE	2	2	7
COEB			02			
COEC		JNZ I	C2	3	3	10
COED			F2			
COEE			C0			
COEF		JZ K	CA	3	3	10
COFO			F7			
COF1			C0			
COF2	I	MVI A,02	3E	2	2	7
COF3			02			
COF4		JMP A4	C3	3	3	10
COF5			22			
COF6			C1			
COF7	K	MVI A,01	3E	2	2	7
COF8			01			
COF9		JMP A4	C3	3	3	10
COFA			22			
COFB			C1			

Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C0FC	G	MOV A,E	7B	1	1	4
C0FD		CPI 01	FE	2	2	7
C0FE			01			
C0FF		JNZ J	C2	3	3	10
C100			05			
C101			C1			
C102		JZ L1	CA	3	3	10
C103			0A			
C104			C1			
C105	J	MVI A,04	3E	2	2	7
C106			04			
C107		JMP A4	C3	3	3	10
C108			22			
C109			C1			
C10A	L1	MVI A,03	3E	2	2	7
C10B			03			
C10C		JMP A4	C3	3	3	10
C10D			22			
C10E			C1			
C10F	O	MOV A,E	7B	1	1	4
C110		CPI 01	FE	2	2	7
C111			01			
C112		JNZ N	C2	3	3	10
C113			18			
C114			C1			
C115		JZ N1	CA	3	3	10
C116			1D			
C117			C1			
C118	N	MVI A,06	3E	2	2	7
C119			06			
C11A		JMP A4	C3	3	3	10
C11B			22			
C11C			C1			
C11D	N1	MVI A,05	3E	2	2	7
C11E			05			
C11F		JMP A4	C3	3	3	10



Address	Label	Mnemonics	Hexco...	Bytes	M-Cycl...	T-States
C120			22			
C121			C1			
C122	A4	MOV B,A	47	1	1	4
C123		LXI H,D001	21	3	3	10
C124			01			
C125			D0			
C126		MOV A,M	7E	1	2	7
C127		RRC	0F	1	1	4
C128		RRC	0F	1	1	4
C129		RRC	0F	1	1	4
C12A		RRC	0F	1	1	4
C12B		ADD B	80	1	1	4
C12C		CPI 0D	FE	2	2	7
C12D			0D			
C12E		JCA5	DA	3	3	10
C12F			3C			
C130			C1			
C131		JNC A1	D2	3	3	10
C132			34			
C133			C1			
C134	A1	JNZ A2	C2	3	3	10
C135			37			
C136			C1			
C137	A2	SUI 0D	D6	2	2	7
C138			0D			
C139		JMP A5	C3	3	3	10
C13A			3C			
C13B			C1			
C13C	A5	RLC	07	1	1	4
C13D		RLC	07	1	1	4
C13E		RLC	07	1	1	4
C13F		RLC	07	1	1	4
C140		LXI H,D000	21	3	3	10
C141			00			
C142			D0			
C143		ORAM	B6	1	2	7
C144		OUT PORTA	D3	1	1	4
C145			10	1	1	4
C146		RST1	CF	1	1	4

Outcome

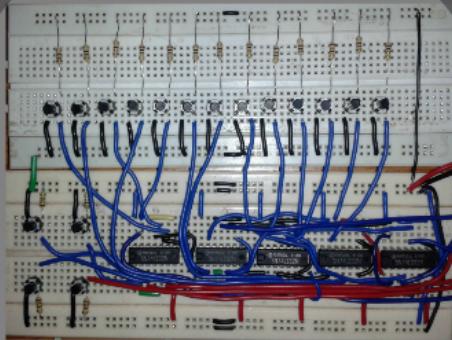
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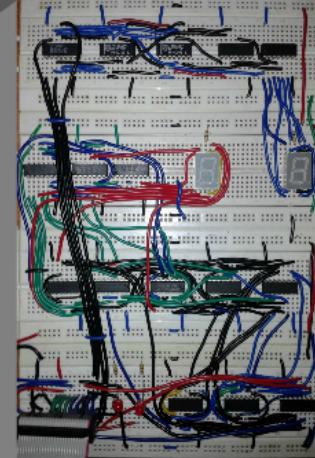
Discussion

- As per the present code, we can have a maximum of 3 cards having the same suit. This can be further improved so that it works with more than 3 cards having the same suit.
- By introducing certain changes in the code, we can also simulate other card games using the same logic circuit.

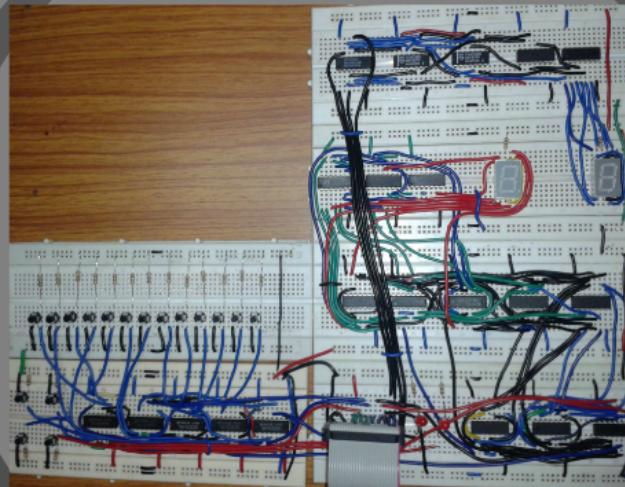
Gallery



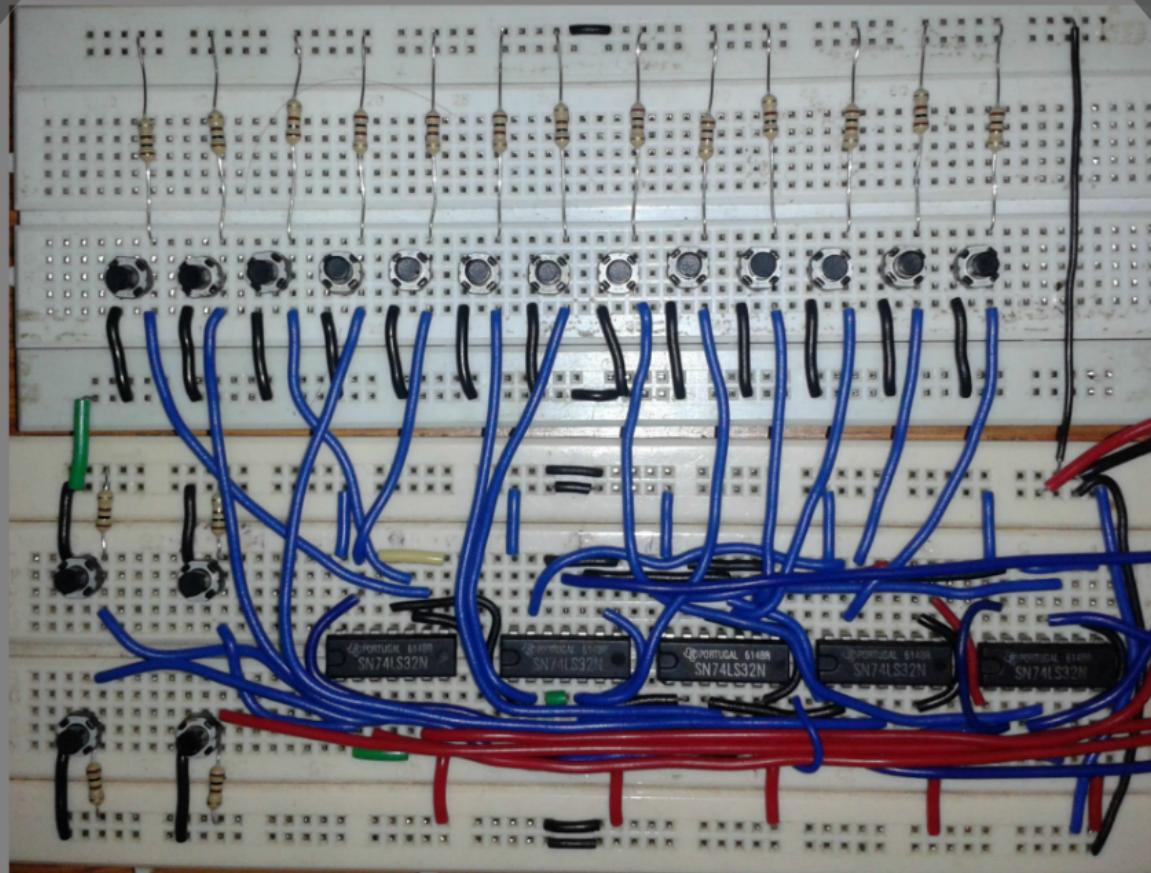
Input Circuit



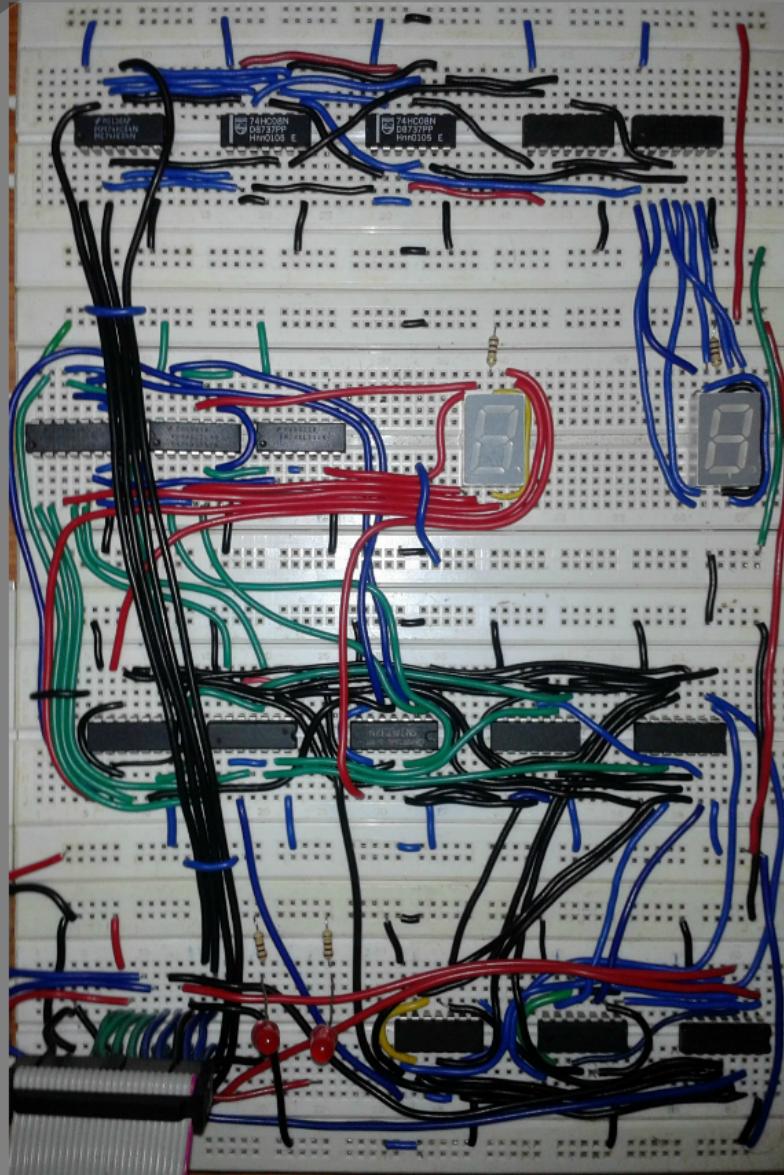
Output Circuit



Circuit



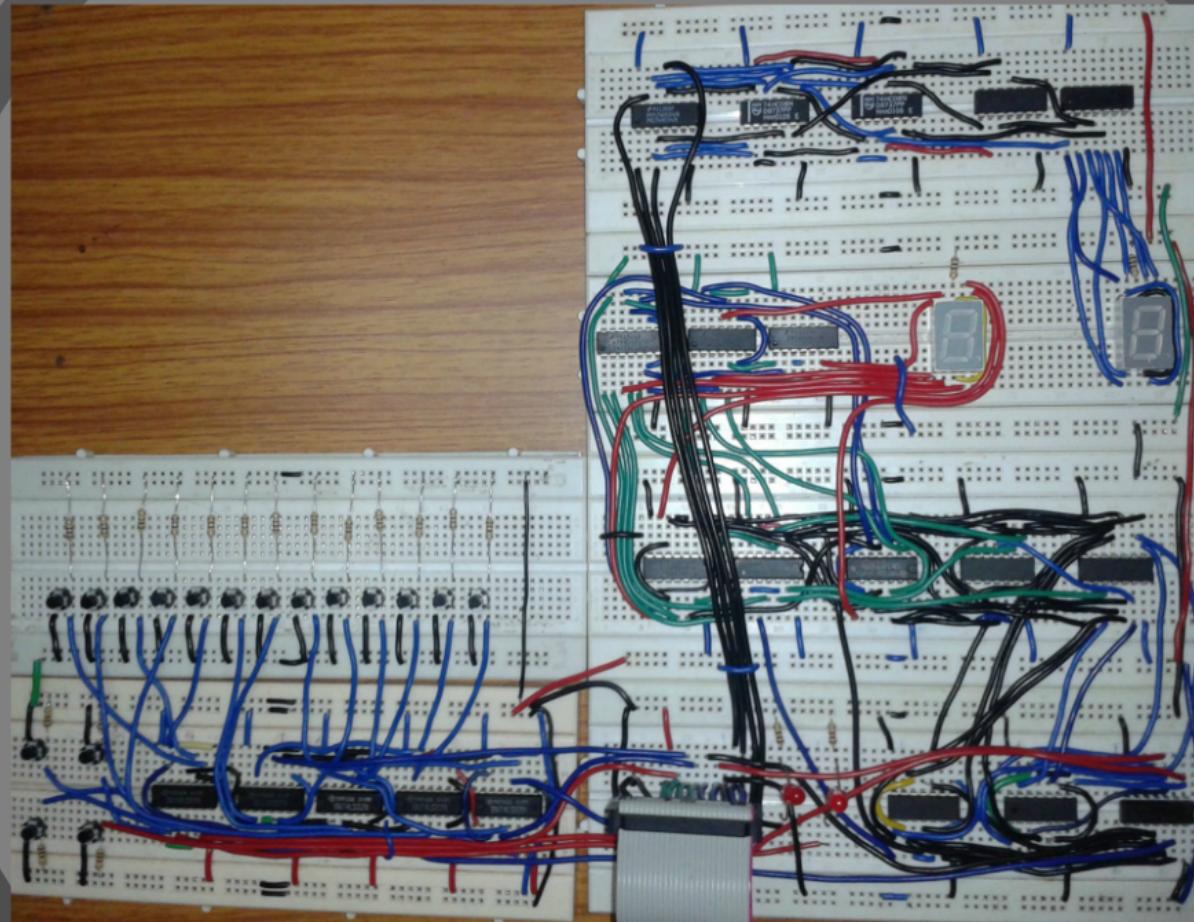
Input Circuit



Output Circuit

Input Circuit

Output Circuit



Circuit