Computer Organization and Architecture
Lab Experiments

PART I

Q 1. Write assembly language programs to perform the following arithmetic operations-

(a) 8-bit addition and subtraction.
(b) 16-bit addition and subtraction.
(c) One's complement and two's complement of a number.
(d) [Optional] Perform left and right rotation operations.
(e) [Optional] Perform binary to BCD conversion.

Q 2. Study the concept of flags and write the following assembly language programs-

(a) Check if two given 8-bit numbers are equal with and without CMP instruction.
(b) Determine the largest number from three given 8-bit numbers.
(c) [Optional] Multiply a given number by 8 without using loops and without repeated addition. (Hint: Use rotation through carry)

Q 3. Write the following assembly language programs-

(a) Find the largest number in an array of numbers.
(b) Multiply two given 8-bit numbers and store the result.
(c) Count the number of ones in a number.
(d) Find GCD of two numbers.
(e) [Optional] Sort an array of 10 numbers.

Q 4. Write the following assembly language programs-

(a) Write a subroutine that adds two 8-bit numbers. Use it to add numbers from one array to numbers from another array.
(b) Write a subroutine to perform the task of DAA instruction.
(c) Write a subroutine to generate a delay of 1 second assuming 320 ns clock cycle.
(d) [Optional] Write a subroutine to calculate Fibonacci number using recursion.

Q 5. Write the following assembly language programs-

(a) Write a program to flash an LED 4 times when a button is pressed.
(b) Write a program to accept two 4-bit/8-bit numbers by user, perform their addition and display the result on screen.

PART II

Go to the webpage of **Virtual Lab for Logic Design and Computer Organization** designed by IIT Kharagpur:

URL: http://vlabs.iitkgp.ernet.in/coa/index.html

Download simulator and its user manual from Workshop and Software sections respectively on the above link. Study the user manual to perform following experiments:

Q 7. Design and test a 4-bit carry lookahead adder circuit using half adders and full adders.

Q 8. Design and test the following circuits-

(a) A 4-bit Booth's multiplier circuit.

(b) A 4-bit shift and add multiplier.

Q 9. Design and test a 4 bit ALU comprising only the AND, OR, XOR and Add operations.

Q 10. Design and test a binary RAM cell using an S-R flip flop, AND gates, NOT gates having select, read/write, input, output.

Q 11. Design and test the following circuits-

(a) An associative cache with one word, 4 bit memory address, 2 bit data without replacement policy.

(b) A direct mapped cache with one word, 4 bit memory address, 2 bit data without replacement policy.

Q 12. Mini Project: Design a single instruction CPU. [Optional]