Implementation and Comparative Analysis of CMOS based Adders w.r.t Speed, Delay and Power Dissipation

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Abstract — Adders are key components of digital design and are necessary part of any digital signal processor (DSP) and microprocessors. Addition is representative of many arithmetic processing operations that must be carried out in portable digital systems[13,14], and the speed and power consumption trade-offs in adder hardware are of interest to portable digital system designers. Apart from the basic Addition they also perform other operations such as Subtractions, multiplication, division, address calculation[1]. Adders of various bit widths are frequently required in Very Large Scale Integration (VLSI) circuits from processors to Application Specific Integrated Circuits. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper, different type of 8-bit full adders are analyzed and compared for transistor count, power dissipation, delay and power delay products. The investigation has been carried out with simulation runs on Tanner environment using 180nm & 90nm CMOS process technology at 2V. The result shows that the carry skip adder has the lowest power-delay product.

Index Terms — Carry Select Adder, Carry Increment Adder, Carry Skip Adder, Carry Look-Ahead Adder, Area-Efficient, 8-Bit Adder, CMOS, Power Delay Product.

I. INTRODUCTION

Adders are most commonly used in various electronic applications e.g. Digital signal processing in which adders are used to perform various algorithms like FIR,IIR etc.It is one of the most important components of a CPU (central processing unit). Fast adders are necessary in ALUs, for computing memory addresses, and in floating point calculations In addition, Full-adders are important components in other applications such as digital signal processors (DSP) architectures and microprocessors. Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems[4]. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing Modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. The carry-ripple adder is composed of many cascaded single-bit full-adders. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. The other types of adder circuits such as carry look- ahead adder, carry skip adder, carry select adder and carry increment adder are more complex than the conventional carry ripple adder and consume more power but these are very fast in

operation. To quantify how effective or efficient a digital design technology is in terms of delay and power; we use the product of the propagation delay and the power dissipation. To measure system efficiency we look at the power delay product of system.

II. CMOS Based ADDER ARCHITECTURES

Multiple-bit addition can be as simple as connecting several full adders in series or it can be more complex. How the full adders are connected or the technique that is used for adding multiple bits defines the adder architecture. Architecture is the most influential property on the computation time of an adder[4]. This property can limit the overall performance. In general the computation time is proportional to the number of bits implemented in the adder. Many different adder architectures have been proposed to reduce or eliminate this proportional dependence on the number of bits. Several adder architectures are reviewed in this section.

A. Ripple Carry Adder (RCA)

An n-bit ripple carry adder consists of N full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin which is the Cout of the previous adder. Addition of k-bit numbers can be completed in k clock cycles. A N-bit ripple carry adder structures is shown in Fig. 1.

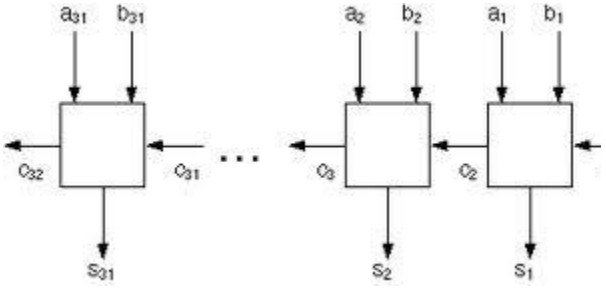

Fig. 1 N-bit Carry Ripple Adder

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The drawback of the ripple carry adder is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder. Figure 1.1 shows the CMOS based Ripple carry adder which is simulated in the EDA tool to calculate the statistics of the adder.

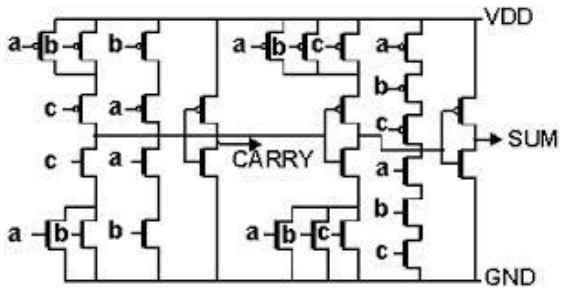

Fig 1.1 CMOS based Ripple carry adder

B. Carry Select Adder (CSA)[5]

The carry select adder comes in the category of conditional sum adder. The carry select adder is constructed by sharing the common Boolean logic term in summation generation. To share the common Boolean logic term, only one XOR gate with one INV gate is needed to generate the summation signal pair as shown in Fig. 2. As the carry-in signal is ready, we can select the correct summation output according to the logic state of carry-in signal. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. Figure 2.1 shows the CMOS based CSA which is simulated in the EDA tool to calculate the statistics of the adder.

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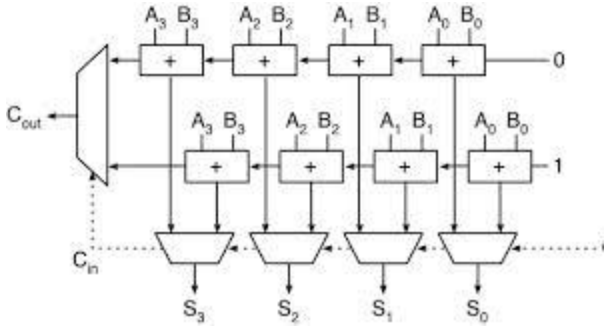

Fig. 2 Carry Select Adder

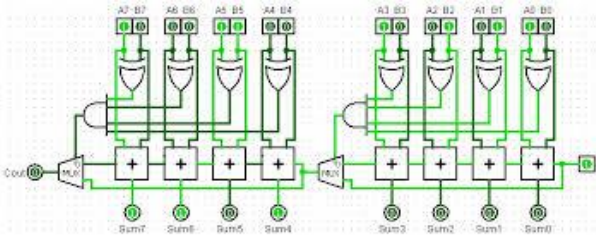

Fig 2.1 CMOS based Carry Select Adder

C. Carry Skip Adder (CSKA)

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder. The carry-skip adder is much like the RCA only it has a carry bypass path. This architecture divides the bits of the adder into an even number of stages M. Each stage M has a carry bypass path that forwards the carry-in of the Mi stage to the first carry-in of the Mi+1 stage. If the binary inputs are such that the carry would normally ripple (or propagate) from the input of the Mi stage to the input of the Mi+1 stage, then the carry takes the bypass path. The Carry Skip Adder reduces the delay

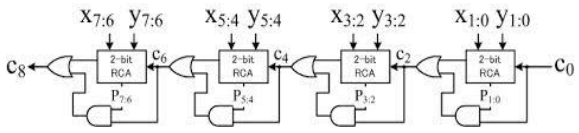

Fig. 3 Carry Skip Adder

due to the carry computation i.e. by skipping over groups of consecutive adder stages. Figure 3.1 shows the CMOS based Carry skip adder which is simulated in the EDA tool to calculate the statistics of the adder.

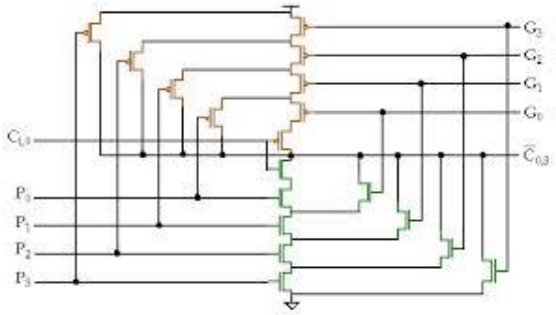

Fig 3.1 CMOS Carry Skip Adder

D. Carry Look-ahead Adder (CLA)

To reduce the computation time, faster way is to add two binary numbers by using carry look ahead adders. It is done by creating two signals (P and G) for each bit position, based on if a carry is propagated through from a less significant bit position (at least one input is a '1'), a carry is generated in that bit position (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half- adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created.

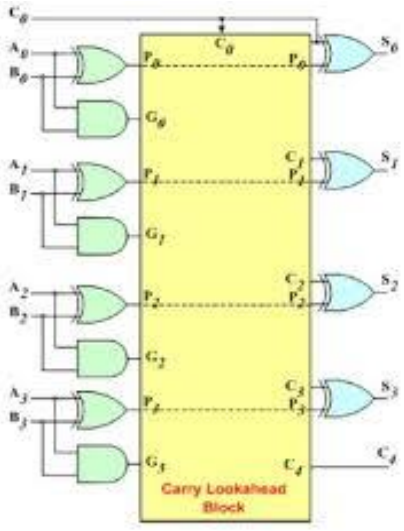

Fig. 4 Carry Look-ahead Adder

In carry look-ahead architecture instead of rippling the carry through all stages (bits) of the adder, it calculates all carries in parallel based on equation (2).

$$Ci = Gi + Pi.Ci\text{-}1 \qquad (2)$$

In equation (2) the Gi and Pi terms are defined as carry generate and carry propagate for the ith bit. If carry generate is true then a carry is generated at the Ith bit. If carry propagate is true then the carry-in to the Ith bit is propagated to the carry-in of i+1 bit. They are defined by equations (3) and (4) where Ai and Bi are the binary inputs being added.

$$Gi = Ai \cdot Bi \qquad (3)$$

$$Pi = Ai + Bi \qquad (4)$$

Figure 4.1 shows the CMOS based Carry look ahead adder which is simulated in the EDA tool to calculate the statistics of the adder.

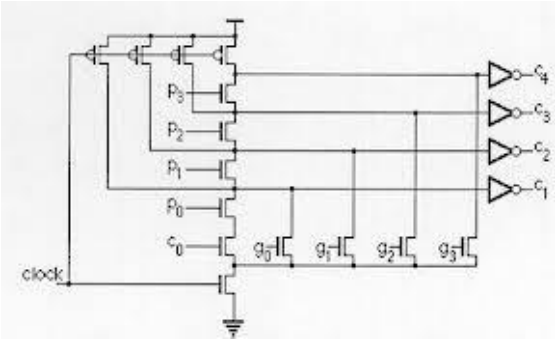

Fig 4.1 CMOS Carry Look-Ahead Adder

E. Carry Increment Adder (CIA)

A carry increment adder (CIA) using a clock phase in which the CIA performs at an increased speed but uses a much smaller chip area than a general fast adder structure. In the CIA from 1 to N partial adder modules (RCA) which generate partial sum and partial carry value using desired bits of two input data (a, b) as a module. The wider the addition bits width, the greater the speed and the smaller the chip area used. In carry increment adder architecture instead of computing two results for each block and selecting the correct one, only one sum is calculated and incremented afterwards if necessary, according to the carry input. Thus the second adder and the multiplexers in the carry-select scheme can be replaced by a much smaller incrementer structure as shown in Fig. 5. Put differently, the computation of a second sum and carry bit is reduced to the generation of a propagate signal per bit position.

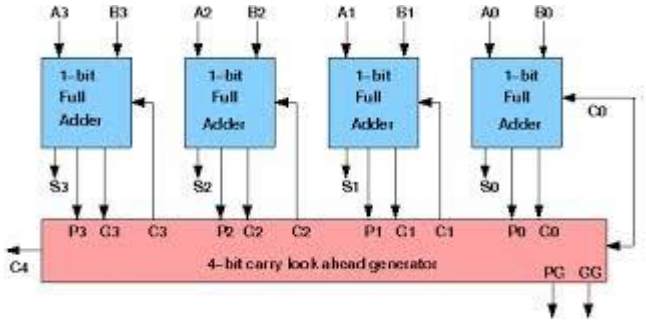

Fig. 5 Carry Increment Adder

Figure 5.1 shows the CMOS based CIA which is simulated in the EDA tool to calculate the statistics of the adder.

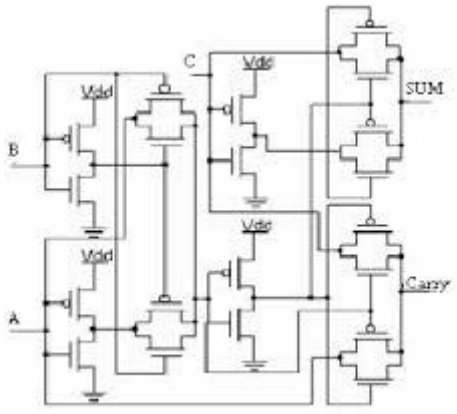

Fig 5.1 CMOS Carry Increment Adder

F. Carry Save Adder

A Carry-Save Adder is just a set of one-bit fulladders, without any carry-chaining. Therefore, an n-bit CSA receives three n-bit operands, namely A(n-1)..A(0), B(n-1)..B(0), and CIN(n-1)..CIN(0), and generates two n-bit result values, SUM(n-1)..SUM(0) and COUT(n-1)..COUT(0).

The most important application of a carry-save adder is to calculate the partial products in integer multiplication. This allows for

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architectures, where a tree of carry-save adders (a so called Wallace tree) is used to calculate the partial products very fast. One 'normal' adder is then used to add the last set of carry bits to the last partial products to give the final multiplication result. Usually, a very fast carry-lookahead or carry-select adder is used for this last stage, in order to obtain the optimal performance.

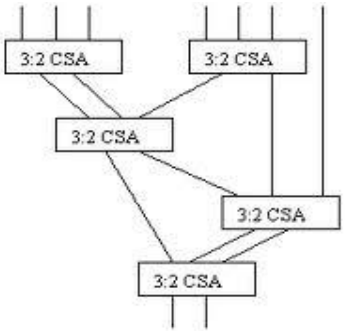

Fig 6. Carry Save Adder

Figure 6.1 shows the CMOS based carry save adder which is simulated in the EDA tool to calculate the statistics of the adder.

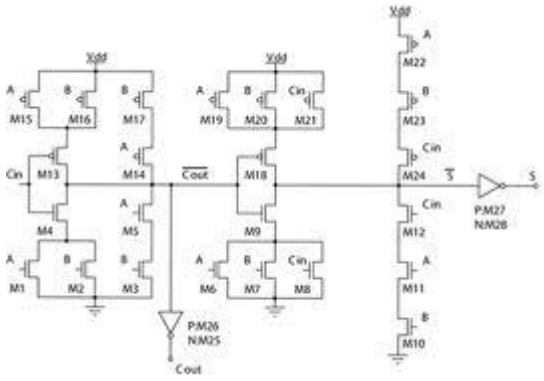

Fig 6.1 CMOS Based Carry Save Adder

G. Carry bypass Adder

The n-bit-carry-skip adder consists of a n-bit-carry-ripple-chain, a n-input AND-gate and one multiplexer. Each propagate bit , that is provided by the carry-ripple-chain is connected to the n-input AND-gate.

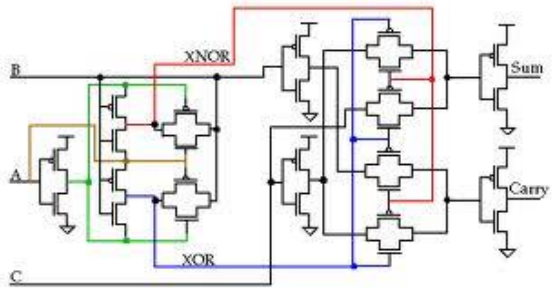

Fig 7.1CMOS Carry Skip Adder

III. SIMULATIONS: Architecture of ADDERS based on Speed, area and power dissipation

Here different adder architectures are simulated and analyzed based on power dissipation, area and speed. The computation time and area is reduced in a large amount in parallel feedback carry adder (PFCA) when compared to other full adders (Ex: Ripple carry adder, carry-look ahead adder etc.)The advantage of PFCA will be more when n is larger. PFCA is faster in speed and smaller in area. The power dissipation of low power 1-bit full adder circuits such as 10-T adders, 11-T adders is analyzed.

Table 2:

S. No	PFCA		RCA		CLA	
	Sum	Carry	Sum	Carry	Sum	Carry
1	1.291	1.291	1.620	1.620	1.620	1.740
2	3.380	3.380	6.247	6.247	6.247	6.561
3	6.513	6.513	13.91	13.919	13.911	14.141
4	10.19	10.191	25.771	25.779	25.771	25.812

Power dissipation (µw) with respect to voltages for 1-bit

	PFCA	RCA	CLA
Transistor count	86	168	188

Transistor count for 4-Bit

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TABLE 3:

	PFCA		RCA		CLA	
Temp	**Carry**	**Sum**	**Carry**	**Sum**	**Carry**	**sum**
27	10.209	10.209	20.052	20.052	21.151	21.151
37	10.227	10.227	20.082	20.082	21.159	21.159
47	10.246	10.246	21.638	21.638	22.722	22.722
57	10.272	10.272	21.658	21.658	22.723	22.723
67	10.276	10.276	22.121	22.121	23.148	23.148
77	10.280	10.280	23.991	23.991	24.107	24.107
87	10.439	10.439	24.812	24.812	25.473	25.473
97	10.586	10.586	25.212	25.212	26.223	26.223

Power dissipation (µw) w.r.t temperature for 1-bit

RESULTS: The PFCA architecture intended to demonstrate:

1) It is easy to implement the PFCA even with larger n because it does nothing to do with the length of adder, that is, to implement the 1024-bit PFCA is as easy as the 16-bit PFCA.

2) The number of transistor to implement the PFCA and the power dissipation is lesser than that of RCA and CLA.

IV. SIMULATION: New performance / power / area efficient, reliable Full adder design

A hybrid pseudo static full adder cell designed using data driven dynamic logic. Simulation results show the adder to out of perform its competitors, both static as well as dynamic topologies in terms of performance, while maintaining relatively similar area and power characteristics. This paper shows a complete characterization of the popular adder cells in terms of delay, area, power, and noise margin and reliability analysis for both super threshold and sub threshold operating regimes.

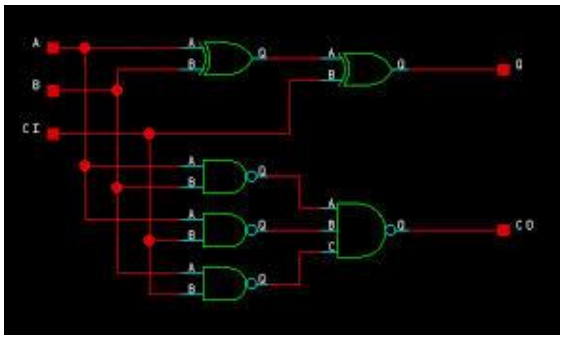

Fig 8: SIMULATION Results

TOOLS USED: CIRCUIT SIMULTION using Spectre simulator from cadence.

Performance comparison of full adder cells as shown in table 4:

TABLE 4:

Adder	Delay (ps)	Power (µW)	Area (µm²)	Noise margin (mV)
28T	175	14.208	122.158	545
10T adder	171.5	12.30	120	421
Domino	137	15.264	140	485
Pure D3L	112.5	14.12	143.23	522
Hybrid D3L	80.04	15.132	132	530

Performance analysis of fast adders using VHDL

It represents performance analysis of different fast adders by taking three parameters i.e area, speed and power. The modified carry skip adders presented in this paper provides better speed and better power consumption as compare to conventional carry skip adder and other adders like ripple carry adder, carry look ahead adder, ling adder, carry select adder. The modified carry skip adders with fix block require few more CLB's because of carry look ahead logic

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whereas with variable block scheme, area optimization is achieved.

TOOL USED: VHDL language, Xilinx 9.1 synthesis tool and ModelsimXE III 6.2 g for simulation. TABLE 5:

Carry skip adder	CLB's	Delay (ns)	Delay (ns)	Power (mW)	Power (mW)
16-bit		Sum	Carry	Dynamic	static
4 blocks	23	23.2	23.1	16.3	219/71
2 blocks	26	20.8	21.7	16.1	219.69
8 blocks	24	26.6	24.5	14.8	219.54

TABLE 6:

Adders(with block variable size)	CLB's	Delay (ns)	Delay (ns)	Power (mW)	Power (mW)
2*7 bit+2*1 bit		Sum	Carry	Dynamic	Static
Ripple carry	24	22.9	22.5	7.9	218.7
Look ahead	24	25.3	24.3	7.6	218.7
Conventional carry skip adder	26	22.3	20.5	14.9	219.5
Modified carry skip adder	26	16.8	12.2	13.8	219.5

RESULTS: There are trade-offs between performance parameters i.e area, delay and power. For designing delay efficient adder, we have proposed a hybrid carry look ahead/carry skip adders in which carry look ahead logic is used instead of ripple carry adder in each block to generate output sum and carry bit for next block. This result in fast operation but at the cost of few more CLB's due to carry look ahead logic.

V. SIMULATION: Area, delay and power comparison of adder topologies w.r.t gate count.

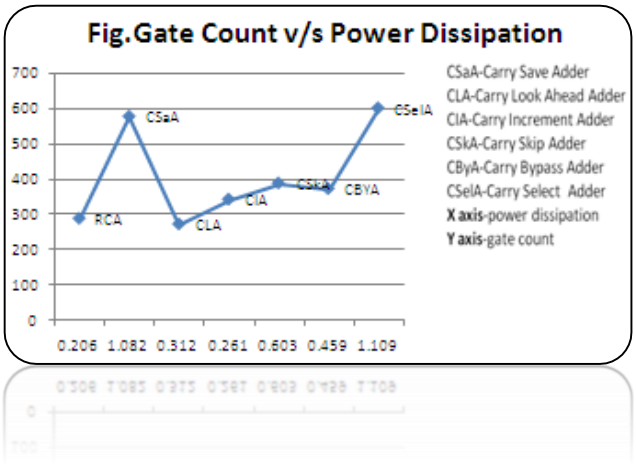
The adders used here are ripple carry adder, carry look ahead adder, carry skip adder, carry select adder, carry increment adder, and carry save adder and carry bypass adder.

Table 1. Shows the comparative analysis of various CMOS adder on the basis of NMOS and PMOS transistor used in the various Adder architectures w.r.t Power Dissipation, Area and Delay.

TABLE 1:

Area topology	Gate count			Power dissipation(mW)	Area µm²	Delay ns
	nMOS	pMOS	total			
RCA	144	144	288	0.206	2214	4.208
CSaA	288	288	576	1.082	5904	2.924
CLA	136	136	272	0.312	2160	3.1
CIA	171	171	342	0.261	2793	2.880
CSkA	194	194	388	0.603	3486	3.022
CByA	186	186	372	0.459	3116	3.01
CSelA	300	300	600	1.109	6201	2.75

RESULTS: The adder topology which has the best compromise between area, delay and power dissipation are carry look-ahead adder and carry increment adders and they are suitable for high performance and low power circuits. The fastest adders are carry select and carry save adders with the penalty of area. The simplest adder topologies that are suitable for low power applications are ripple carry adder, carry skip and carry bypass adder with least gate count and maximum delay.



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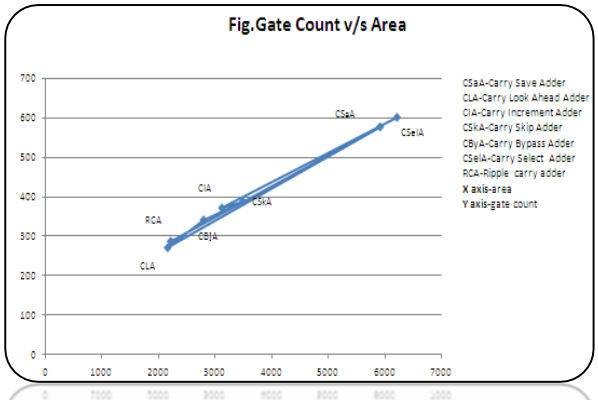

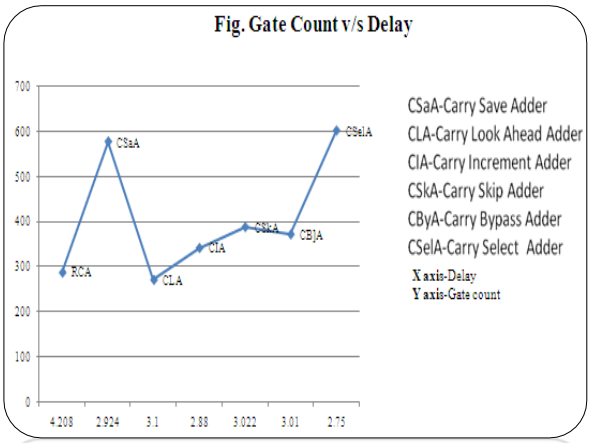

VI. CONCLUSION

In this paper, different type of adders (Carry Skip, Carry Look Ahead, Carry Select and Carry Increment) has been designed and evaluated on power, delay and area parameter. Both Carry Skip and Carry Look Ahead uses least number of transistors while Carry Increment has highest number of transistors i.e. 284 transistors. The Carry Skip Adder (CSKA) has the least Power Delay Product (PDP) in both 180nm and 90nm technology implementation. The overall performance of Carry Look Ahead Adder is comparable to that of Carry Skip Adder in both implementations. The delay of Carry Increment Adder is lowest among all adder types in 180nm technology and hence it emerges as the fastest adder but its power dissipation is very high.

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