SKY130D1SK1

Package : The outer 256 pin package(for eg), pin locations are driven by board

Pads : Package is connected to chip through pads, any signal go too and fro the chip is through the PADS only.

Core: Has all the logic ( RISC V SOC, Foundry Ips etc )in it

Machine generated alternative text:
Die 
PADS 
Vdd3V3 
vdd1v8 
Core 
vddl 
comp_inn 
comp_inp 
gpi05 
gpi07 
gpiol 
gpiol 
gpiol 
gPi01 
gpiol 

Die is manufactured on Si wafer.

Foundry IP : IP need some specific technique to be ready.

Macro : Pure digital logic.

Interface files are used to communicate with Foundry.

SKY L1

Machine generated alternative text:
Cat Swap 
nelude estdio.h* 
swap (size_t my! l, size_t s) 
size_t ten: 
tenp my(sl; 
nylsl • 
•yls•ll • temp: 
unatgekunatg.VirtuatBox 
objdu•p •d suap o 
sp. .48 
11 
-'Oesktop,'toots/riscv 
file format elfu.littleriscv 
sir/ risev- 
toots 
elf. 
onyx I 
ACA012'X' 
OA12*1 
Nvxe_5S., 
OA12i*1 
txt-I 
OA12tX' 
6/1122* 
oøposx' 
OA121 
sassenbly of section 
. text: 
addi 
addi 
stu 
addi 
stu 
sp, 
al, .48"0) 
aS,a5 ad 
a5.0(a5) 
980 •swap • Oxb 
oeeooel eswap»: 
'422 
180e 
fca43c23 
fcb43823 
078e 
fd843103 
97ba 
639t 
fet43423 
one 
fd8431Ø3 
RISC-V Architecture! 
i 

ISA : Instruction set architecture, used to interact with computer.

For C Program to run on HW with shown layout(chip interior), it required to be first compiled in assembly language program(RISC V assembly language program) which is then converted in machine language (binary). Finally these bits gets executed in this layout.

Interface between the RISC V arch and layout is HDL. We need to implement this RISC V specs using some RTL.

From RLT to layout it is RTL2GDS Flow.

Machine generated alternative text:
S Cat Swap 
etude estdio.h* 
p (size_t myll, size t s) 
size_t ten: 
tenp my's l; 
•yls•ll • temp: 
unatgekunatg.VirtuatBox 
sp. .48 
0:01 
t 0:01 
0:01 
0:01 
1 0:01 
1 9:01 
0:01 
.01 
instr_jalr 
01 
121 
01 7'bae91e11 
.91 
elf. 
objdu•p •d 
swap. o 
onyx I 
ACA0121X' 
OA12*1 
NVX8_5S., 
OA121*i 
IXI_I 
OA'2tX' 
6A122* 
instr_sub) 
sir/ risev- toots 
file format elf64-1ittleriscv 
isasseaty of section 
. text: 
eøeoøeeoeo «swap.exl» 
eøøøeoeeoøel eswap»: 
addi 
addi 
addi 
stu 
sp, 
as, .48(s0) 
aS,aS ad 
a5.0(a5) 
05, .2qs0) 
a5.a5,1 
a4, .40(s0) 
RISC-V Architecture 
'422 
IBoe 
fca43c23 
fcb43823 
td043J83 
078e 
fd843103 
97ba 
0785 
one 
'"843103 
module picorv32 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
parameter 
ENABLE COUNTERS 1 
ENABLEROUNTERS64 1 
Implementation (picorv32 cpu core) 
ENABLE REGS 
ENABLE REGS 
always clk) begin 
LATCHED MEM 
Two STAGE SHI 
BARREL SHIFT 
TWO CYCLE CO 
TWO CYCLE Al. 
COMPRESSED 1 
CATCH MISALI 
is 
is 
is 
if 
•a Hinstr_lui, instr_auipc, instr_jal); 
add sub I (instr Lui, instr_auipc, inst r _ jai, 
siti bit slt I (instr slti, instr bit, instr_slth 
sltiu bitu situ Hinstr_sltiu, instr_bltu, instr_sltu); 
Ibu lhu_lw •a Ilinstr Ibu, instr lhu, instr_lw); 
instr_jalr, instr_addi, 
sltiu, instr situ); 
latched114: 
latched(31• 
instr add, 
instr 
rdata 
rdata 
rdata 
compare I (is _ beq bne_blt 
nem_done) 
instr siti, instr_slt, 
begin 
01 7'bge10111; 
men 
men 
me. 
instr 
instr 
instr 
instr 
instr 
lui 
auipc 
_ jal 
retirq 
waitirq 
mem 
nem 
rem 
mem 
mem 
rdata 
rdata 
rdata 
rdata 
rdata 
rdata 
latched16• 
latched16: 
latched(6• 
latched16: 
latched16: 
latched16• 
ENABLE IRO; 
. 251 

SKY\_L2 :

How applications like Firefox runs on hardware ?

Application software enters into system software which converts it to binary language.

Major components of system software are OS, compiler, assembler.

OS handles IO operations and memories and take app to assembly language program and then to Machine language, that can be handled by HW.

C/C++/java --> Compiler --> RISCv Format (.exe file) (depends on instruction set)-->Assembler takes this and converts to binary numbers.

Machine generated alternative text:
Mozilla Acrobat Oracle VM 
Firefox Reader DC VirtualBox 
aao 
Application Software 
or Apps 
Il System Software 
Windows T 
ns r 
nstr2 
01 
0101001001 
• Handle 10 operations 
• Allocate memory 
• Low level system functions 
Hardware 
c 
Doutl 
Dout3 
Clk Out 
Dout2 
Dout4 
„DEC p) 
m .:nni 

Instruction set arch is interface between compiler and assembler

Assembler output is in Binary.

SKY130\_D1\_SK2:

Machine generated alternative text:
Digital ASIC 
Design 
RTL IP's 
EDATools 
PDK DATA 
ASIC 

PDK: it is a process design kit & is a interface between fab and design.

Machine generated alternative text:
What is a 
PDQ 
• PDK Process Design Kit 
• Collection of files used to model a fabrication 
process for the EDA tools used to design an IC 
• Process Design Rules: DRC, LVS, PEX 
• Device Models 
• Digital Standard Cell Libraries 
• I/O Libraries 

For open source ASICS we need below tools

Machine generated alternative text:
Open Source 
Digital ASIC 
Design 
Qflow 
openROAD 
openLANE 
EDA 
Tools 
ASIC 
RTL 
Designs 
i brecores.org 
opencores.org 
gi thub.com 
PDK 
Data 
Google 
SKgUJQter 

SKY\_L2:

Machine generated alternative text:
RTL 
Synth 
Simplified RTL 
to GDSII Flow 
Fp+pp 
PDK 
Route 
Place 
CTS 
GDSII 
Sign Off 
• Synthesis 
• Floor/Power Planning 
• Placement 
• Clock Tree Synthesis 
• Routing 
• Sign Off 

These are some major implementation steps.

Machine generated alternative text:
Clock Tree 
Synthesis 
RTL 
Synth 
Fp+pp 
PDK 
Place 
CTS 
Route 
GDSII 
Sign Off 
• Create a clock distribution network 
• To deliver the clock to all sequential elements (e.g., FF) 
• With minimum skew (zero is hard to achieve) 
• And in a good shape 
• Usually a Tree (H, X, ...) 

Machine generated alternative text:
RTL 
Synth 
Sign Off 
Fp+pp 
PDK 
Route 
GDSII 
Sign Off 
Place 
CTS 
• Physical Verifications 
• Design Rules Checking (DRC) 
• Layout vs. Schematic (LVS) 
• Timing Verification 
• Static Timing Analysis (STA) 

Machine generated alternative text:
OpenLANE 
ASIC Flow 
Des' n 
RTL Synthesis 
(Yosys abc) 
STA 
(OponSTA) 
Floor-planning 
Placement 
Optimization 
Fake ant. diodes 
Insertion Script 
Global Routing 
Exploration 
SKY130 
LEC 
Dotaøed 
(Triton Route) 
ant. diodes 
Swapping 
RC Extraction 
STA 
(C»enSTA) 
(magic & notgen) 
gds2 Strearning 
GDS" 

SKY130\_DY1\_SK3:

Getting familiar to open source EDA TOOLS

Machine generated alternative text:
File Edit 
View 
-xr-x 5 
-x 44 
vsduser@vsdsquadron: 
Search 
1000 
1000 
1000 
1000 
1000 
1000 
1000 
1000 
1000 
1000 
1000 
Terminal Help 
29 
29 
29 
29 
29 
29 
29 
29 
29 
29 
19 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2023 
docker build 
designs 
configuration 
conf. py 
clean runs. tcl 
README . md 
Makefile 
LICENSE 
CONTRIBUTING . md 
AUTHORS . md 
default.cvcrc 
drwxr 
drwxr-xr 
drwxr 
-rw-r 
-rwxr-xr 
-xr- 
997 
997 
997 
997 
997 
997 
997 
997 
997 
997 
1000 
4096 
4996 
4096 
5514 
966 
25599 
7273 
11350 
1285 
799 
963 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
May 
x 
-x 
2 
1 
1 
1 
1 
1 
1 
1 
1 
bash-4.2S 
L INFO) : 
. / flow. tcl -interactive 
vo.21 
interactively 
Version: 
Running 

* 1. Open terminal in UBUNTU
  2. Change working directory to work/tools/openlane\_working\_directory/openlane
  3. There you will see flow.tcl file by using ls -ltr.
  4. Type "docker" in terminal,
  5. Source flow.tcl in interactive mode by typing ./flow.tcl -interactivep it will shows the above view.
  6. Use "package require openlane 0.9".
  7. You can see already build designs present in designs in directory work/tools/openlane\_working\_directory/openlane/designs.
  8. Before running the synthesis, need to setup data for design, as only few files are there
  9. Machine generated alternative text:
     skY130A_skY130_ 
     config . tcl 
     vsduser@vsdsquadron : —l lopenlane Idesigns/p 
     icorv32aS Is 
     -l tr 
     vsduser 
     vsduser 
     vsduser 
     vsduser 
     vsduser 
     vsduser 
     vsduser 
     docker 
     docker 
     docker 
     docker 
     docker 
     docker 
     docker 
     4096 
     299 
     299 
     299 
     209 
     209 
     444 
     Jun 
     Jun 
     Jun 
     Jun 
     Jun 
     Jun 
     Jun 
     29 
     29 
     29 
     29 
     29 
     29 
     29 
     2021 
     2021 
     2021 
     2021 
     2021 
     2021 
     2021 
     src 
     skY130A 
     skY130A 
     skY130A 
     skY130A 
     skY130 
     skY130 
     skY130 
     skY130 
     fd 
     fd 
     fd 
     fd 
     fd 
     sc 
     sc 
     sc 
     sc 
     sc 
     ms config. tcl 
     Is _ config . tcl 
     hs config. tcl 
     hdll_config . t 
     hd_config . tcI 
     total 
     28 
     drwxr 
     -xr 
     -rw-r 
     -rw-r 
     -rw-r 
     -rw-r 
     - rwxr-xr 
     - rwxr-xr 
     -x 
     -x 
     -x 
     2 
     1 
     1 
     1 
     1 
     1 
     1 

* 1. To setup, use prep -design picorv32a
  2. It will merge files and we don’t need different files it will be shown like below in terminal

Machine generated alternative text:
vsduser@vsdsquadron: 
File Edit View Search 
Terminal Tabs Help 
vsduser@vsdsquadron: -/Desktop/work/t.. 
vsduser@vsdsquadron: -/Desktop/work/t. 
t INFC): Current run 
directory is icpenLANE_flow/designs/picorv32a/ runs/ 26-04_14- 
Ll 
(INFO): Preparing LEF Files 
(INFO): Extracting the number of available metal layers from / home/vsduser/Deskt 
)p/work/tools/openlane working dir/pdks/sky130A/libs. 
/ sky130_fd sc_hd . t lef 
(INFO): The number of available metal layers is 6 
(INFO): The available metal layers are lil metl met2 met3 met4 met5 
(INFO): Merging LEF Files... 
nergeLef. py 
sky130 fd sc 
sky130 fd sc 
sky130 ef sc 
sky130 ef sc 
sky130 ef sc 
sky130 ef sc 
sky130 ef sc 
sky130 ef sc 
nergeLef. py 
. Merging LEFs 
hd. lef: SITES matched found: O 
hd. lef: MACROS matched found: 437 
hd 
fill 12. lef: SITES matched found: O 
hd 
fill 12. lef: MACROS matched found: 1 
hd 
decap_12. lef: SITES matched found: O 
hd 
decap_12. lef: MACROS matched found: 1 
hd 
fakediode 2. lef: SITES matched found: O 
hd 
fakediode 2. lef: MACROS matched found: 1 
. Merging LEFs complete 
(INFO) : 
(INFO) : 
(INFO) : 
(INFO) : 
Trimming Liberty.. 
Generating Exclude List.. 
Storing configs into config. tcl 
Preparation complete 

* 1. A new folder named Runs will come into the directory

Machine generated alternative text:
vsduser@vsdsquadron: 
drwxr-xr-x 2 
skY130A_skY130_ 
drwxr-xr-x 3 
File Edit View Search Terminal Tabs Help 
vsduser@vsdsquadron: -/Desktop/work/t. 
vsduser@vsdsquadron: -/Desktop/work/t.. 
29 2021 sky130A sky130 fd tcl 
29 2021 sky130A sky130 tcl 
29 2021 config. t 
29 2021 . tcI 
29 2021 config.tcl 
- rw-r 
-rw-r 
-rw-r 
- rwxr- 
- rwxr 
1 vsduser 
1 vsduser 
1 vsduser 
docker 209 Jun 
docker 209 Jun 
docker 209 Jun 
docker 209 Jun 
docker 444 Jun 
xr-x 1 vsduser 
-xr-x 1 vsduser 
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
icorv32aS Is 
-l tr 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
docker 
docker 
docker 
docker 
docker 
docker 
docker 
4096 
209 
209 
209 
209 
209 
444 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Apr 
29 
29 
29 
29 
29 
29 
29 
26 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
19:41 
src 
skY130A 
skY130A 
skY130A 
skY130A 
skY130 
skY130 
skY130 
skY130 
fd 
fd 
fd 
fd 
fd 
sc 
sc 
sc 
sc 
sc 
ms config. tc 
Is config. tc 
hs config. tc 
hdll config. 
hd_config . tc 
total 
tcl 
32 
1 
1 
1 
1 
-rwxr-xr-x 1 
-rwxr-xr-x 1 
icorv32a 
config . tcI 
run 
vsduser 4096 

* 1. To view TLEF information, go to directory work/tools/openlane\_working\_directory/openlane/designs/picorv32a/runs/<date>/tmp, and open merge.lef. You will get layer and wire and cell level information.

Machine generated alternative text:
END nwell 
LAYER pwell 
TYPE MASTERSLICE 
"TYPE 
PROPERTY LEF58 TYPE 
END pwell 
LAYER lil 
TYPE ROUTING , 
DIRECTION VERTICAL 
PITCH 0.46 0.34 
OFFSET 0.23 0.17 
WIDTH 0.17 
# SPACING e .17 
SPACINGTABLE 
PARALLELRUNLENGTH e 
WIDTH e 0.17 
AREA 9.9561 
THICKNESS 0.1 
EDGECAPACITANCE 40.697E-6 
PWELL 
1 
6 
CAPACITANCE CPERSQDIST 36.9866E-6 ; 

* 1. Report and result will have information after runs.
  2. Conf.tcl tell info of parameters taken during the run.

Machine generated alternative text:
View searcn 
lerrmnal 
laDs Help 
x vsduser@vsdsquadron: -/Desktop/work/t... 
vsduser@vsdsquadron: -'Desktop/work/t. 
drwxr-xr-x 2 vsduser vsduser 
k layout 
4096 Apr 26 19:41 
drwxr-xr-x 2 vsduser vsduser 
4096 Apr 26 19:41 
cvc 
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
icorv32a/runs/26-04_14-11/tmpS less merged 
merged: No such file or directory 
vsduser@vsdsquadron : — / Desktop lopenlane Idesigns/p 
14-11/tmpS less merged. lef 
less merged. lef 
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
14-11/tmpS cd 
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
icorv32a/runs/26-04 
L 3 J+ Stopped 
icorv32a/runs/26-04 
icorv32a/runs/26-04 
14-11S Is 
-l tr 
170 
4096 
4096 
4096 
1585 
15 
4996 
20869 
Jun 
Apr 
Apr 
Apr 
Apr 
Apr 
Apr 
Apr 
28 
26 
26 
26 
26 
26 
26 
26 
2021 
19:41 
19:41 
19:41 
19:41 
19:41 
19:41 
19:41 
PDK SOURCES 
tmp 
results 
reports 
cmds . log 
OPENLANE VERSION 
loqs 
confi . tcl 
total 
52 
- rwxr-xr- 
x 
drwxr- 
-x 
drwxr 
-xr-x 
drwxr 
-xr-x 
-rw-r 
-rw-r 
drwxr- 
xr- 
x 
-rw-r 
1 
11 
11 
11 
1 
1 
11 
1 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
icorv32a/runs/26-04_14-11 

* 1. In open lane we can make changes in the run. Parameters like core utilization can be changed.
  2. Further run the synthesis by run\_synthesis in Openlane prompt. It will run BIOS Synthesis and ABIS run (to get chip module area).

Machine generated alternative text:
vsduser@vsdsquadron: 
File Edit View Search Terminal Tabs Help 
vsduser@vsdsquadron: -/Desktop/work/t. 
x vsduser@vsdsquadron: -'Desktop/work/t. 
LINFOJ: setting input delay to: 4.946000000000001 
set max fanout S: :env(SYNTH MAX FANOUT) L current design J 
set c 1k indx Llsearch L all inputs J Lget port S: 
#set r st indx Llsearch L all inputs J Lget port resetnJJ 
set all inputs wo c 1k Llreplace L all inputs J SC 1k indx Sclk indxJ 
#set all inputs wo clk_rst Llreplace Salt _ inputs wo_clk Srst_indx Srst_indxJ 
set all inputs wo_clk r st Salt _ inputs wo_clk 
correct resetn 
set input delay Sinput delay value 
-clock Lget_clocks S: Sall 
inputs wo c 1k r st 
#set input delay 0.0 -clock Lget clocks S: :env(CLOCK PORT) J (resetn) 
set output delay Soutput delay value 
-clock Lget_clocks S: Lal 
outputs J 
# TODO set this as parameter 
set driving_cell -lib cell S: CELL) -pin S: 
CELL PIN) L all inputs J 
set cap _ load Lexpr S: CAP LOAD) / 1000.01 
puts "IL INFOXJ: Setting load to: Scap_load" 
L INFO): setting load to: 0.01765 
set _ load Scap_load L all outputs J 
tns -759.46 
wns -24.89 
LINFO): Synthesis was successful 

* 1. STA has been done, synthesis and ABIS run also get completed, we can see chip module area

Machine generated alternative text:
File Edit View Search Terminal Tabs Help 
vsduser@vsdsquadron: -/Desktop/work/t.. 
x vsduser@vsdsquadron: -/Desktop/work/t. 
147712.9184ae: 
skY130 
skY130 
skY130 
skY130 
skY130 
skY130 
skY130 
skY130 
skY130 
skY130 
fd 
fd 
fd 
fd 
fd 
fd 
fd 
fd 
fd 
sc 
sc 
sc 
sc 
sc 
sc 
sc 
sc 
sc 
sc 
hd 
hd 
hd 
hd 
hd 
hd 
hd 
hd 
hd 
hd 
031ai 2 
032a 2 
041a 2 
or2 2 
or2b 2 
or3 2 
or3b 2 
or4 2 
or4b 2 
or4bb 2 
1 
109 
2 
1088 
25 
68 
5 
6 
2 
MEM: 
96 
Chi area for module 
icorv32a 
29. Executing Verilog backend. 
Dumping module Apicorv32a' . 
Warnings: 307 unique messages, 307 total 
End of script. Logfile hash: eede8add8e, CPU: 
user 42.27s system 0.26s, 
54 MB peak 
Yosys 0.9+3621 (git shal 84e9fa7, gcc 8.3.1 
-fPIC -os) 
Time spent: 51% 2x abc (43 sec), 13% 33x opt 
expr (11 sec), 
LINFO): Changing net list from to /openLANE 
- 11/ resu Its/ synthesis/ picorv32a . synthesis . v 
LINFO): Running Static Timing Analysts... 
flow/ designs/ pico rv32a/ runs/ 26-04_1 

* 1. Flop ratio = No. of D Flip flop/total no. of cells
  2. So Fxtp= 1613

Machine generated alternative text:
skY130 
skY130 
sk 130 
sk 130 
fd 
fd 
sc 
sc 
sc 
sc 
hd 
hd 
hd 
hd 
buf 1 
buf 2 
conb 1 
dfxt 2 
1656 
8 
1613 

And, total no. of cells=14876

Machine generated alternative text:
picorv32a 
Number 
Number 
Number 
Number 
Number 
Number 
Number 
Number 
of 
of 
of 
of 
of 
of 
of 
of 
wi res: 
wire bits: 
public wires: 
public wire bits: 
memory bits: 
rocesses: 
cells: 
14596 
14978 
1565 
1947 
14876 
1 
35 
a21110 2 
a2110 2 
sky130 fd sc hd 
skv130 fd sc hd 

Flop count = 1613/14876=0.1084\*100= 10.8%

* 1. To see run result for synthesis, go to directory work/tools/openlane\_working\_directory/openlane/designs/picorv32a/runs/<date>/results/synthesis. It contains synthesized netlist
  2. You can view synthesized netlist.

Machine generated alternative text:
vsduser@vsdsquadron: -/Deskt0D/work/t. 
vsduser@vsdsquadron: -/Desktop/work/t.. 
re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wi re 
wtre 
01197 
01198 
01199 
01200 
01201 
01202 
01203 
01204 
01205 
01206 
01207 
01208 
01209 
01210 
01211 
01212 
01213 
01214 
01215 
01216 
01217 
01218 
01219 

* 1. To see timing report go to reports folder, where all reports exists