SKY130\_D3\_SK

* 1. Will see wrt invertor as a cell.
  2. Download .magic file from github.
  3. If want change how IO pins are aligned in the core,ie pin configuration , use

Machine generated alternative text:
vsduser@vsdsquadron : — / lopenlane Idesigns/p 
tcorv32a/runs/28-04_09-06/resuIts/fIoorpIanS magic -T /home/vsduser/Desktop/work 
/ tools/openlane working dir/pdks/sky130A/libs. tech/magic/sky130A. tech lef read . 
. / . ./tmp/merqed. lef def read picorv32a. floorplan.def 

* 1. As seen below, all pins are equidistant

Machine generated alternative text:
picorv32a 
Topmost cell in the window 

* 1. If want to change for some other IO pin strategy, IO places supports 4 IO strategy.
  2. So we will take the variable that selects mode for IO
  3. Navigate to openlane/configuration folder
  4. FP\_IO switch is there to select this, it will be in floorplaning file.

Machine generated alternative text:
vsduser@vsdsquadron: -'Desktop/work/t . 
vsduser@vsdsquadron: -/Desktop/work/t... 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
set 
SIZING) relative 
CORE UTIL) 50 
CORE MARGIN) e 
ASPECT_RATIO) 1 
PDN 
PDN 
PDN 
PDN 
PDN 
PDN 
PDN 
PDN 
10 
10 
10 
10 
10 
10 
VOFFSET) 16.32 
VPITCH) 153.6 
HOFFSET) 16.65 
HPITCH) 153.18 
AUTO_ADJUST) 1 
CORE RING) e 
ENABLE_RAILS) 1 
CHECK_NODES) 1 
MODE) 1; matchin 
HLENGTH) 4 
VLENGTH) 4 
VEXTEND) -1 
HEXTEND) -1 
VTHICKNESS MULT) 2 
mode 
1 random e utdistant mode 

* 1. Set it to 2 and rerun floorplan to change the spacing between the pins.

Now will see rise propagation, fall propagation delay etc

SPICE SIMULATIONS ON MOSFETs::

* 1. Will create spice deck: ie connectivity info of the netlist.
  2. pMOS arrow is inside, nMOS is outside

Machine generated alternative text:
SPICE deck 
• Component connectivity 
Vdd 
Ml 
Vin 
M2 
Vss 
cload 
Vss 

* 1. PMOS source to Vdd, NMOS source to Vss.
  2. Define components values, channel length is 0.25u and with be .375u for both.
  3. Ideally pmos should be 2x or 3x of nmos
  4. Will define all values as below

Machine generated alternative text:
SPICE deck 
• Component connectivity 
• Component values 
Identify 'nodes' 
Name 'nodes' 
Vin 
Ml 
0.375u/0.25u 
2.5V 
Vdd 
M2 
0.375u/0.25u 
cload 
Vss 

* 1. Now will start writing the spice deck
  2. \*\* specify comments
  3. Drain gate substre source is the format for specifying as below to define connectivity

Machine generated alternative text:
Ml out in vdd vdd W—O. 375u L—O.25u 
M2 out in 0 nmos W—0.375u IFO.25u 

M1 is drain connected to out, gate to in node and substrate and source both to vdd

* 1. cload os between out and node 0 of value 10fF
  2. Supply voltage vdd between vdd and 0 of 2.5v
  3. Input voltage Vin Between and 0 of 2.5v

Machine generated alternative text:
cload out O IOf 
Vin in 0 2.5 

* 1. Sweeping the gate input of nmos from certain voltage
  2. i.e sweeped gate input voltage from 0 to 2.5 of steps of 0.05v
  3. Final steps is to describe he modelfile have complete info of nmos and pmos

Machine generated alternative text:
. include tsmc 025um model. mod 
.LIB "tsmc 025um model -mod" CMOS MODELS 

* 1. Will do spice sim for parameters

Machine generated alternative text:
SPICE waveform : device 
(Wn/Ln:Wp/Lp 1.5) 

* 1. Modelfile looks like below have nmos and pmos parameters

Machine generated alternative text:
• SPICE 3fS Level B, 
• Feb 23/01 
• LOT: MBH 
49 
27 
star-HsprcE Level 
WAF: 
Temper a t u re _pa rame ter f a ul t 
. MODEL NNos ( 
49, 
Level 
VTHO 
wr2w 
S. BE-9 
0.3907S3S 
4.214601E-3 
3.1 
1 
12-7 
0.4376003 
2.3S49E17 
e.26S2S2e-3 
: 2. S1734SE-6 
0.3707226 
-9.89493E-10 
1.25449925 
2.S79719E-B 
: -3.7220937 
2.310668E-7 
0.2411602 
316.5922683 
2.1S4013E-1e 
2.4746322-11 
0.2428704 
1.2735648 
+ÄGS 

* 1. Netlist is like below

Machine generated alternative text:
MODEL Descriptions 
Vdd 
H2 out O O w-o.37Su LEO.2Su 
vddvdd 0 2. S 
0 2.S 
• SIMULATION cc—ands 
. dc 0 2. S 0.05 
. LIB -tsnc 02Sun nodel.nod" e•ws 

* 1. Will do spice simulation on this
  2. Source circuit file
  3. Execute the circuit
  4. Look at node voltages present
  5. Plot out vs input
  6. VI characters will come

Machine generated alternative text:


* 1. Switching threshold is a point where vin = vout

Machine generated alternative text:
SPICE waveform : 
device 
1.5) 
SPICE waveform : Wn:O.375, Wp:O.9375u, 
device 
(Wn/Ln:1.5, wp/tp 3.75) 
Static behavior Evaluation : CMOS inverter Robustness 
1. Switching Threshold, Vm 
Vm is the point where Vin Vout 

* 1. In this point both are turned on so high possibility of leakage current.
  2. These are the switching thresholds are ~0.98v and ~1.2V

Machine generated alternative text:
SPICE waveform : 
device 
(Wn/Ln:Wp/Lp 1.5) 
Vm 0.98v 
SPICE waveform : Wn:O.37S, Wp:O.937Su, 
device 
(Wn/Ln:1.5, wp/tp 3.75) 
Static behavior Evaluation : CMOS inverter Robustness 
1. Switching Threshold, Vm 
m IS 
e pom w ere 
ou 

* 1. Both pMOS and nMOS are in saturation.

Machine generated alternative text:
Vrn 1.2v 
Vm is the point where Vin Vout 
Vm - 0.98v 
Static behavior Evaluation : CMOS inverter Robustness 
1. Switching Threshold, Vm 
Vout 
N'aos 
2 
1.5 
1 
0.5 
0 0.5 
1 
1.5 
Vin 

* 1. The pulse is defined as below

Machine generated alternative text:
Home 
Pa Ste 
Clipboard 
Date and 
drawing time 
a 
Find 
select an 
2Su device 
x 
, , wp/Lp:3.75) 
o 
2.5v 
lops 
Font 
Ops 
Para grapn 
Insert 
object 
MI out 
M2 out in 
Vdd vdd O 
vdd pmos FO .37Su IFO. 2Su 
O O nmos w—o.37Su 
2.5 
2ns 
SIWATION 
. lop 4n 
02Sum mode I. 
CMOS 

* 1. Pulse: starts from 0 end at 2.5 shift is 0 starts at 0, rise and fall time of 10ps, pulse width is 1ns and complete cycle of 2ns, will use this as input to CMOS.
  2. We will do transient analysis.

Machine generated alternative text:
ps 
1.0 

* 1. Zoomed in rise wave be below

Machine generated alternative text:
1 _ 26 
1_2S 
1_2S 
1_24 
1.24 
1.23 
1, 00 
1.02 
1.04 
1.10 
1.12 
1.14 
1.18 

Rise delay will be 0.14831 or 148 ps

* 1. For fall delay will do same

Machine generated alternative text:
1.26 
1.26 
1.2S 
1.2S 
1.24 

Fall delay 71ns

Machine generated alternative text:
v i branch 
ngspice 12 
1 0144Se-009. 
1 16277e-009. 
xo • 2.004ese-009. 
xo • 2.076S3e-009. 
yo 
VS 
yo 1.2S006 
yo • 1.2S 
yo • 1.25 
1.2S006 
real . 
43 

* 1. Vm=0.99,

Machine generated alternative text:
x.Wn 
Vm 0.99v 
I Wp/Lp 
Wn/Ln 
Wp/Lp 
2Wn/Ln 
Wp/Lp 
3Wn/Ln 
Wp/Lp 
4Wn/Ln 
Wp/Lp 
5Wn/Ln 
148p 
10:10 / 10: 

* 1. Clone the git

Machine generated alternative text:
vsduser@vsdsquadron : -l . 
tech/magicS cd 
cd openlane 
git clon 
-l tr 
e https://github.com/nickson-jose/vsdstdcelldesign.git 
Cloning into 'vsdstdcelldesign' 
remote: Enumerating objects: 492, done. 
remote: Counting objects: 100% (18/18), done. 
remote: Compressing objects: 100% (18/18), done. 
remote: Total 492 (delta 7), reused O (delta O), pack-reused 474 
Receiving objects: 100% (492/492), 24.08 MiB | 5.33 MiB/s, done. 
Resolving deltas: 100% (210/210), done. 
Is 
total 
140 
drwxr 
-rw-r 
-rw-r 
drwxr 
-rw-r 
-rw-r 
-rw-r 
- rwxr-xr 
drwxr 
drwxr 
drwxr 
-rw-r 
-rw-r 
drwxr 
-rwxr-xr 
-rw-r 
-rw-r 
scripts 
run designs. py 
report generation wrapper . py 
regression _ results 
README . md 
Makefile 
LICENSE 
flow. tcI 
docs 
docker build 
designs 
CONTRIBUTING . md 
conf. py 
configuration 
clean runs.tcl 
AUTHORS . md 
default . cvcrc 
vsdstdcelldesi n 
-xr 
-xr 
-xr 
-xr 
-xr 
-xr 
-x 
-x 
-x 
-x 
-x 
-x 
-x 
15 
1 
1 
3 
1 
1 
1 
1 
5 
5 
44 
1 
1 
2 
1 
1 
1 
6 
vsduser 
vsduser 
vsduser 
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4996 
20787 
7898 
4096 
25599 
7273 
11359 
6519 
4096 
4096 
4096 
1285 
5514 
4096 
966 
709 
963 
4096 
Jun 
Jun 
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May 
May 
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29 
20 
1 
2921 
2021 
2021 
2021 
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2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2023 
10:11 
drwxrwxr-x 
vsduser@vsdsquadron : — / / openlane 

* 1. Copy this file below to

Machine generated alternative text:
vsduser@vsdsquadron : — / Desktop / pdks/sky130A/Iibs . 
tech/magicS cp sky130A. tech /home/vsduser/Desktop/work/tools/openlane working di 
r/openlane/vsdstdcelldesign/ 
vsduser@vsds 
tech/magicS 

Machine generated alternative text:
I tbs. ref/ I tbs. tech/ 
. config/ 
cd 
ks/sky130A/libs . tech/ 
irsim/ 
magic/ 
ngspice/ 
k layout/ netgen/ openlane/ 
cd 
ks/sky130A/libs . tech/magic/ls 
bash: cd: too many arguments 
cd 
ks/sky130A/libs . tech/magic 
vsduser/Desktop/work/tools/openlane working dir/p 
xschem/ 
qflow/ 
xcircuit/ 
vsduser/Desktop/work/tools/openlane working dir/p 
-l tr 
vsduser/Desktop/work/tools/openlane working dir/p 
vsduser@vsdsquadron : — / / pdks/sky130A/Iibs 
tech/magicS Is -l tr 
docker 
docker 
docker 
docker 
docker 
docker 
docker 
docker 
docker 
4996 
4996 
136719 
203669 
3013 
11471 
5098 
15144 
21168 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
Jun 
28 
28 
28 
28 
28 
28 
28 
28 
28 
2921 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
2021 
bum bond enerator 
sk 130A.tech 
sky130A. tcl 
sky130A.magicrc 
skY130A-GDS . tech 
sky130A-BindKeys 
generate _ fill . py 
check_density . py 
total 
408 
drwxr 
-xr 
-x 
drwxr 
-xr- 
x 
- rwxr-xr 
-x 
-rwxr-xr 
-x 
-rwxr-xr- 
x 
-rwxr-xr- 
x 
-rwxr-xr 
-x 
-rwxr-xr 
-x 
-rwxr-xr 
-x 
2 
2 
1 
1 
1 
1 
1 
1 
1 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser@vsdsquadron : — / / pdks/sky130A/Iibs 
tech/magicS 

* 1. It got copied in the desired location,

Machine generated alternative text:
vsduser@vsdsquadron : —l / openlane/vsdstdcel 
IdesignS Is 
total 180 
1 
-rw-rw-r-- 
1 
-rw- rw-r- 
drwxrwxr-x 2 
drwxrwxr-x 2 
drwxrwxr-x 2 
1 
-rw- rw-r-- 
-rwxr-xr-x 1 
-l tr 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
13525 
11357 
4096 
4096 
4096 
2716 
Apr 
Apr 
Apr 
Apr 
Apr 
Apr 
Apr 
30 
30 
30 
30 
30 
30 
30 
23:38 README.md 
23:38 LICENSE 
23:38 Images 
23:38 extras 
23:38 libs 
23:38 sky130 inv . mag 
vsduser 136710 
vsduser@vsdsquadron : —l / openlane/vsdstdcel 
IdesignS 

* 1. To see the layout use magic,

Machine generated alternative text:
vsduser@vsdsquadron : —l Desktop/work/tools/openlane 
IdesignS Is 
extras Images Iibs 
LICENSE README.md skY130A. 
vsduser@vsdsquadron : — / Desktop/work/tools/openlane 
IdesignS magic -T sky130A. tech sky130_inv . mag & 
L IJ 4678 
vsduser@vsdsquadron : —l Desktop/work/tools/openlane 
IdesignS 
working_dir/openlane/vsdstdcel 
tech sky130_inv . mag 
working_dir/openlane/vsdstdcel 
working_dir/openlane/vsdstdcel 

It will come like shown below

Machine generated alternative text:


16-MASK CMOS PROCESS ::

* 1. Select the substrate (P)
  2. Creating active region for transistors
  3. N-well and P-well formations

Well diffusion by using dry furnace to get wells.

As per from threshold voltage equation, which depends on body effect, we will try to maintain body effect parameters.

* 1. For formation of gate will maintain doping concentration and masking.
  2. Open the lightly doped drain (LDD)for P+(SD), P-(LDD), N(substarte)) (N+ (SD), N-(LDD), P (substrate)). Its P+P-and N in this order only becoz of hot electron effect and short chennel efffect
     1. When device size reduces, high energy carriers can break Si-SI bonds- hot electron effect
     2. When we move to shorter channel length drain voltage penetrate to channel area and tough to control voltage- short channel effect
  3. Source and drain formation
  4. Creating metal contacts
  5. Higher metal level formation
  6. Chemical mechanical polishing.

Basic cmos invertor

Machine generated alternative text:
To m 
13 
cell 
dow 

* 1. Take cursor to block and type what, you can see what is what
  2. Machine generated alternative text:
     File Console 
     ( 9.919, 
     Edit Interp Prefs History Help 
     ( 9.999, 
     o. 999) , 
     9.919 x 9.919 
     o, 
     1, 
     tkcon 2.3 Main 
     1 
     1 
     microns: 
     lambda : 
     Main console 
     display active (Tc18.6.8 / Tk8.6 8) 
     find 
     DRC 
     next 
     error 
     invalid command name "DRC" 
     select: Topmost cell in the window 
     select: Topmost cell in the window 
     select: Topmost cell in the window 
     % what 
     Selected mask layers: 
     nwell 
     ( Topmost 
     Unknown macro or short 
     % what 
     Selected mask layers: 
     cell in 
     command : 
     cell in 
     the window ) 
     the window ) 
     nmos 
     ( Topmost 
  3. You can also see parasitic capacitances value by creating a file using ext2spice which looks like
  4. Press G to see the blocks.

Machine generated alternative text:


Machine generated alternative text:
SPICE3 file created from sky139_inv . ext 
ad—I .44n 
pd O. 
as-I .37n 
ad—I .44n 
pd O. 
as-I . 52n 
technology : 
sky130A 
152m 
152m 
ps-o.148m w 
ps-o .156m 
. option scale—lom 
. subckt skY130 inv A Y VPWR VCND 
XO Y A VGND VCND nfet 
23 
-35 
Xl Y A VPWR VPWR 
-37 
ce VPWR Y 0.117f 
0.0754f 
0.0774 f 
C2 A VPWR 
0.279f 
C3 Y VGND 
0.45f 
C4 A VGND 
0.781f 
C5 VPWR VGND 
. ends 
01v8 
01v8 

LOOKING INTO SPICEDECK::

* 1. Type extract all to create sky130\_inv.ext
  2. Use ext2spice ctresh 0 rthresh 0 command next
  3. Use ext2spice
  4. Open file sky130\_inv.spice and make below changes for more details see step 1-6
  5. Install ngspice model and run, you will see the below window

Machine generated alternative text:
vsduser@vsdsquadron: 
File Edit View Search Terminal Tabs Help 
x vsduser@vsdsquadron: -/Desktop/work/tools/openl... 
vsduser@vsdsquadron: -/Desktop/work/tools/openl. . 
Scale set 
- 27 .eeeeee and TNOM 27 .eeeeee 
Doing analysis at TEMP — 
Warning: va: no DC value, transient time e value used 
times tep 
Initial Transient 
Solution 
Voltage 
3.3 
3.3 
1.63996e-11 
-1.63996e-11 
Timestep too small; time 1.97288e-11, 
aborted 
se-22: 
Node 
vgnd 
vpwr 
va#branch 
vss#branch 
vdd#branch 
doAnalyses : 
va#branch " 
TRAN : 
trouble with node 
run simulation(s) 

* 1. To see the output use plot y vs time for a input, transient response be like below

Machine generated alternative text:
tran2: * spice3 file created from sky130_inv.ext - technology: sky130a 

* 1. Now will see for characterization of cell (finding 4 parameters), will see rise time ie time taken by the output to transient from 20% to 80% of max value ( VDD), fall time be time taken by output waveform to fall from 80% to 20%, similarly fall and rise cell delays ie propagation delays ie 50% of input and 50% of output
  2. You will get rise time from below figur e

Machine generated alternative text:
File 
xo _ 1.44038e- 
yo - 2.30556 
xe 2.59615e- 
xe 1.82692e- 
xe 1.73077e- 
xe 5.65385e- 
ye - 1.26389 
xe 2.18713e- 
ye 0.667581 
xe 2.13478e 
ye 0.636806 
Yl 0.655556 
dx 7.82609e- 
ye 0.66 
ye 0.66 
Edit View 
Search Terminal Tabs Help 
vsduser@vsdsquadron: -/Deskt. . 
08, 
09 
, ye e. 715278 
09 
, ye 0.520833 
09 
, ye 0.416667 
ran2: * spice3 file created from sky130_inv... 
sgo.o 
870.0 
SSO.O 
650.0 ; 
2.140 
2.180 
2.180 
hardcopy 
2.200 
xe 2e-09, ye 0.513889 
4.78846e- 
09 
09, 
09, 
-09, 
11, 
dy 
0.01875 
dx/dy 4. 
Xl 2.21304e- 
17391e-09 
09, 
dy /dx 
2.39583+08 
xe 2.16448e-09, 
xe 2.18119e-09, 

* 1. Cell fall delay is time difference when output has falled to 50% when input is 50%
  2. 20% \* 3.3 = 0.66
  3. Rise time be 2.24-2.18=0.06
  4. Similar we can do for fall time
  5. Now will see cell fall delay ie propagation delay when output is 50% of rise
  6. 50%\*3.33=1.665
  7. Time difference be

Machine generated alternative text:
xe 2.15061e- 
ye - 1.653 
xo 2.18606e- 
09 
09 
ye - 1.65302 

* 1. 2.18-2.15=0.03 be the rise time delay
  2. We have characterized our invertor, now will use this layout and create lef file to be used in open lane then will plug that cell in openlane picorv32a.

MAGIC TOOL ::

See magic basics from magic webpage.

<http://opencircuitdesign.com/magic>

* 1. Technology file : It is one signal file whch contains everything of process it has all layers in colors, connectivity, rules for wiring etc

Tech file list technology of fab process

Google opensource skywater 130 nm

Sources of information are there:

PDK can be found here:

Pdk : <https://github.com/google/skywater-pdk>

Documantation : <https://skwater-pdk--136.org.readthedocs.build>

* 1. For lab exercise take layout from <http://opencircuitdesign.com/open_pdks/archieve/drc_test.tgz>
  2. Unzip the zipped firl you can get below files

Machine generated alternative text:
File Edit View Search Terminal Tabs Help 
vsduser@vsdsquadro. 
vsduser@vsdsquadro 
vsduser@vsdsquadro.- 
vsduser@vsdsquadro.- 
drwxrwxr-x 3 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
vsduser 
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vsduser 
vsduser 
vsduser 
4096 
3178 
3610 
1535 
1684 
897 
11586 
1489 
4648 
2565 
1198 
2103 
1799 
1599 
1114 
757 
1948 
2497 
1351 
536 
5588 
2565 
3025 
135962 
2476 
4114 
1271 
1267 
966 
955 
May 
Sep 
Sep 
Sep 
Sep 
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capm . mag 
difftap . mag 
dnwell . mag 
hvtp . mag 
hvtr . mag 
licon . mag 
li.mag 
Ivtn . mag 
.magtcrc 
mcon . mag 
metl . mag 
met2. mag 
met3. mag 
met4. mag 
met5. mag 
npc . mag 
nsd . mag 
nwell.mag 
pad . mag 
poly . mag 
psd . mag 
rpm . mag 
sky130A. tech 
tunm . mag 
varac.mag 
via2. mag 
via3. mag 
via4.mag 
via . mag 
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-rw- 
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-rw- 
-rw- 
-rw- 
- rw- 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
1 
vsduser@vsdsquadron:—/Desktop/work/drc_test/drc_testsS 

* 1. .mag is layout files
  2. .magicrc is script for starting magic.
  3. Start magic by using magic -D XR
  4. Load file met3.mag, you will see below layout. Here there are number of independent example layouts showing some kind of DRC errors
  5. Each example is labeled with name.
  6. You can see rows listed correspond to each name in document.

Machine generated alternative text:
File Edit Cell Window Layers Drc Options 
Ml DRC 
Loaded: met3 Editing: met3 Tool: box Techr 
(+2.38 +8.67) +2.38 +8.67 
MI_IMI 
anx 

* 1. Select any and type :drc why
  2. You will see below details

Machine generated alternative text:
File Console 
off 
status 
style 
Edit 
tkcon 2.3 Main 
Interp Prefs History Help 
turn off background checker 
reenable background checker 
report if the drc checker is on or off 
set the DRC style 
print out design rules in file or on tty 
print out stats about design rule database 
print out statistics gathered by checker 
print out reasons for errors under box 
printrules 
rulestats 
statistics 
why 
DRC y 
(file) 
invalid command name "DRC" 
drc why 
Meta13 spacing 9.3um (met3.2) 
Loading DRC CIF style. 
drc why 
Meta13 spacing 9.3um (met3.2) 

* 1. Draw box near box3.3c type cif see VIA2, will shows contact cuts
  2. Load the file poly.mag, you will see below view

Machine generated alternative text:


* 1. Check poly 9
  2. Select a poly and type what,you will see below

Machine generated alternative text:
File 
tkcon 2.3 Main 
File Console Edit Interp Prefs History Help 
Main console display active (Tc18.6.8 / Tk8.6.8) 
Cell met3 read from path /home/vsduser/Desktop/work/drc test/drc tests 
poly. mag 
Cell poly read from current working 
directory 
Unknown 
Unknown 
Unknown 
Unknown 
Unknown 
Unknown 
Unknown 
Unknown 
% what 
macro 
macro 
macro 
macro 
macro 
macro 
macro 
macro 
or 
or 
or 
or 
or 
or 
or 
or 
short 
short 
short 
short 
short 
short 
short 
short 
command : 
command : 
command : 
command : 
command : 
command : 
command : 
command : 
cell in the window ) 
Selected mask 
layers : 
hpolyres ( Topmost 

* 1. The box measurements between poly be below

Machine generated alternative text:
File 
Edit 
Window 
Layers 
Drc 
Options 
Ml DRC 
layout 1 
Loaded: poly Editing: poly Tool: box Technology 
tkcon 2.3 Main 
(+20.4 +4) +2.53-0.27 micrc 
( 1967.99, 
3934, 
urx, 
( 18.229, 
( 1822 . 99, 
3644, 
urx, 
( 18.229, 
( 1822 . 99, 
3644, 
992 
u ry 
898 
u ry 
898 
451.99) 
) 4416 
File Console Edit 
Interp Prefs History 
Help 
428.99) , 
856 ) , 
4.279), 
427 . , 
854 ) , 
4.279), 
427 . , 
854 ) , 
lambda : 
internal: 
Root cell 
mlc rons: 
lambda : 
internal: 
% box 
Root cell 
+1 
microns: 
lambda : 
internal: 
48. 
96 
box : 
width 
9.359 
35 . 
79 
box: 
width 
9.359 
35 . 
79 
x 
x 
x 
x 
x 
x 
x 
x 
x 
x 
23 . 
46 
height 
9.229 
22 . 
44 
height 
9.229 
22 . 
44 
1919.99 , 
3838, 
ux, 
17.879, 
1787 . 99 , 
3574, 
ux, 
17.879, 
1787 . 99 , 
3574, 
) area (unitsA2) 
4.499) 9.977 
449.99) 779.99 
) 3989 
) area (unitsA2) 
4.499) 9.977 
449.99) 779.99 
) 3989 

* 1. If 0.22 micron then rule violations
  2. To fix poly9 error, open file sky130A.tech
  3. Search for poly and add one more line with with allpolynonres

Machine generated alternative text:
# xhrpoly poly resistor) 
width xhrpoly 359 "xhrpoly resistor width *d poly. la)" 
# NOTE: xhrpoly resistor requires choice of discrete widths 9.35, 
# uhrpoly poly resistor, 2kOhm/sq) 
width uhrpoly 359 "uhrpoly resistor width *d" 
spacing xhrpoly, uhrpoly,xpc alldiff 489 touching illegal 
9.69, 
up to 1.27. 
5182 , 34 
"xhrpoly/uhrpoly resistor spacing to diffusion *d (poly. 9)" 
spacing xhrpoly, uhrpoly,xpc allpolynonres 489 touching illegal 
"xhrpoly/uhrpoly resistor spacing to diffusion (poly. 9)" 
# MOS Varactor device rules 
overhang *nsd var,varhvt 259 
"N-Tap overhang of Varactor € (var. 4)" 
overhang *mvnsd mvvar 259 
"N-Tap overhang of Varactor c (var. 4)" 
width var,varhvt,mvvar 189 
"Varactor length (var. 1)" 
extend var,varhvt,mvvar *poly 1999 
"Varactor width (var. 2)" 

Machine generated alternative text:
"N-diff distance to 
cifmaxwidth ntap missing 
"P-diff distance to 
variants * 
# POLY 
P-tap in deep nwell.must be 15.9um (Ltl. 2.1)" 
bend illegal 
N-tap must be 15.9um (LU.3)" 
width allpoly 159 "poly.width c (poly. la)" 
spacing allpoly allpoly 219 touching ok "poly. spacing (poly. 2)" 
spacing allpolynonfet alldifflvnonfet 75 corner_ok allfets 
"poly. spacing to Diffusion (poly.4a)" 
spacing npres *nsd 489 touching illegal 
"poly. resistor spacing to N-tap (poly. 9)" 
spacing npres allpolynonres 489 touching illegal 
"poly. resistor spacing to N-tap (poly. 9)" 
overhang *ndiff, rndiff nfet,scnfet,npd,npass 259 "N-Diffusion overhang of nmos (poly. 7)" 
overhang *mvndiff ,mvrndiff mvnfet,mvnnfet 259 
"N-Diffusion overhang of nmos (poly. 7)" 
overhang *pdiff, rpdiff pfet,scpfet,ppu 259 "P-Diffusion overhang of pmos *d (poly. 7)" 
overhang *mvpdiff ,mvrpdiff mvpfet 259 "P-Diffusion overhang of pmos *d (poly. 7)" 
overhang *poly allfets 139 "poly. overhang of transistor (poly. 8)" 
rect only allfets "No bends in transistors (poly. 11)" 
rect only xhrpoly,uhrpoly "No bends in poly resistors (poly. 11)" 
extend xpc/a xhrpoly, uhrpoly 2169 
"poly. contact extends poly resistor by *d (licon.lc I i. 5)" 
spacing xhrpoly, uhrpoly xhrpoly, uhrpoly 1249 touching illegal 
search hit BOTTOM, continuing at TOP 
4818,9-1 

* 1. Load the file using tech load sky130A.tech

Machine generated alternative text:
File Console Edit 
Interp 
44 
Prefs 
History 
3574, 
ux, 
Help 
854 ) , 
3644, 
urx, 
898 
u ry 
3989 
area (unitsA2) 
internal: 
box 
cell box: 
79 
x 
x 
x 
x 
x 
nlcrons: 
lambda : 
internal: 
width 
9.359 
35 . 
79 
height 
9.229 
22 . 
44 
( 17.879, 
( 1787.99, 
( 3574, 
4.279), 
( 18.229, 4.499) 9.977 
( 1822.99, 449.99) 779.99 
427 . , 
854 ) , 
3644, 898 ) 3989 
tech load sky139A. tech 
Input style sky139: scaleFactorz2, multiplier—2 
rhe following types are not handled by extraction and will be treated as non-electrical types: 
mvpbase nnmos obsactive mvobsactive obslil obslilc obsml obsm2 obsm3 obsm4 obsm5 obsmrdl fillblock comment obscommen 
res9p35 res9p69 res1p41 res2p85 res5p73 
Scaled tech values by 2 / 1 to match internal grid scaling 
Existing layout may be invalid. 

* 1. Check the drc

Machine generated alternative text:
Cell poly read from current working directory 
check 
Loading DRC CIF style. 

**L8: exercise to describe DRC error in geometrical construct**

* 1. Need to use the Boolean operators in sequence
  2. After all operators are applied, whatever left is an error
  3. Open sky130A.tech and search for DRC
  4. Check for cifmaxwidth value.

Machine generated alternative text:
File Edit Tools 
Syntax Buffers Window Help 
1. 3761 
9.36 
1. 7361 
9.27 
2 . 9961 
9.36 
2. 3661 
9.42 
2. 7861 
9. 845 
3. 6311 
9.39 
4. 9211 
9. 845 
4. 8661 
9. 595 
5.3711 
1.26 
3.7311 
11.8834 4.9 
render 
render 
render 
render 
render 
render 
render 
render 
render 
render 
render 
render 
style 
METI 
VIAI 
MET2 
VIA2 
MET3 
VIA3 
MET4 
VIA4 
METS 
CAP" 
CAPM2 
RDL 
metal 2 
via 
meta13 
via 
meta14 
via 
meta15 
via 
meta16 
meta18 
meta19 
metal 7 
# NOTE: This style is used for DRC 
scalefactor 19 nanometers 
options calma-permissive-labels 
only, 
not for GDS output 
# Ensure nwell overlaps dnwell at least 9.4um outside and 1. Bum inside 
emplayer dnwell shrink dnwell 
shrink 1939 
templayer nwell missing dnwell 
grow 499 
and-not dnwell shrink 
and-not nwell 
/drc 



* 1. PMOS Drain connected to node Y gate to node A, source and substrate to node Vpwr.
  2. NMOS drain connected to Y, gate to A and source and substrate to node Vgnd.
  3. Need node 0 with vdd 3.3V
  4. Pulse voltage needed between A nad Vgnd of voltage Va
  5. Any voltage is measured wrt one box dimention i.e. 0.01micron
  6. Make below changes for including pmos, nmos library files, supply and pulse voltages.

Machine generated alternative text:
* SPICE3 file created from sky139 
. option scale—9.91u 
. include ./libs/pshort. lib 
. include ./libs/nshort. lib 
// . subckt skY139_inv A Y VPWR VGND 
inv. ext 
technology: sky139A 
Y A VGND VGND 
Y A VPWR VPWR 
VDD VPWR 
3.3V 
VSS VGND 
A VGND PULSE (OV 
va 
CO VPWR Y 9.117f 
e . 9774f 
Cl VPWR A 
9.279f 
Y VGND 
C4 A VGND 9.45f 
e. 781f 
VPWR VGND 
// . ends 
. tran In 29n 
. control 
run 
. endc 
. end 
nshort model. 
pshort model. 
3.3v 9.1ns e. 
All 
ad 1.43k pd-152 as-I .37k ps-148 w-3.5e+@7 1-2.3+97 
-1.44k 
pd-152 as-I .52k ps-156 w-3.7e+97 1-2.3e+97 
Ins 2ns 4ns) 
19, 36 

* 1. Add .tran from 1ns to 20ns for transient analysis
  2. Run this in ngspice