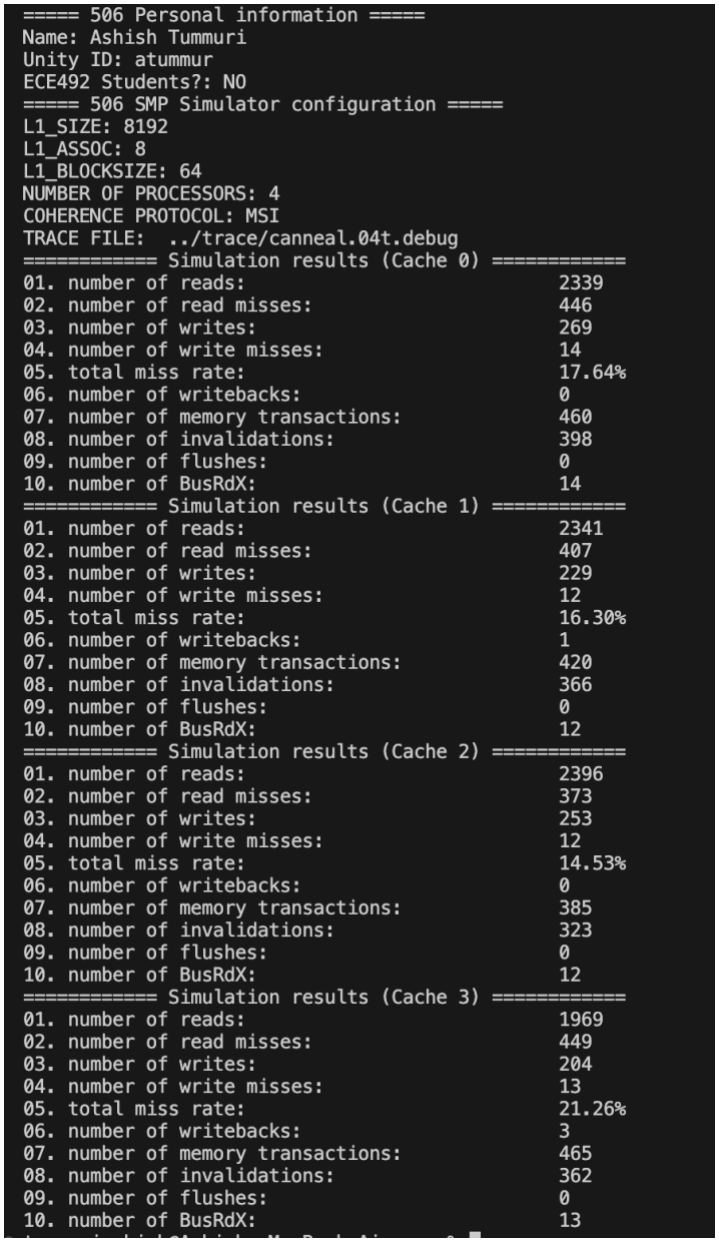
ECE/CSC 406/506: Architecture of Parallel Computers

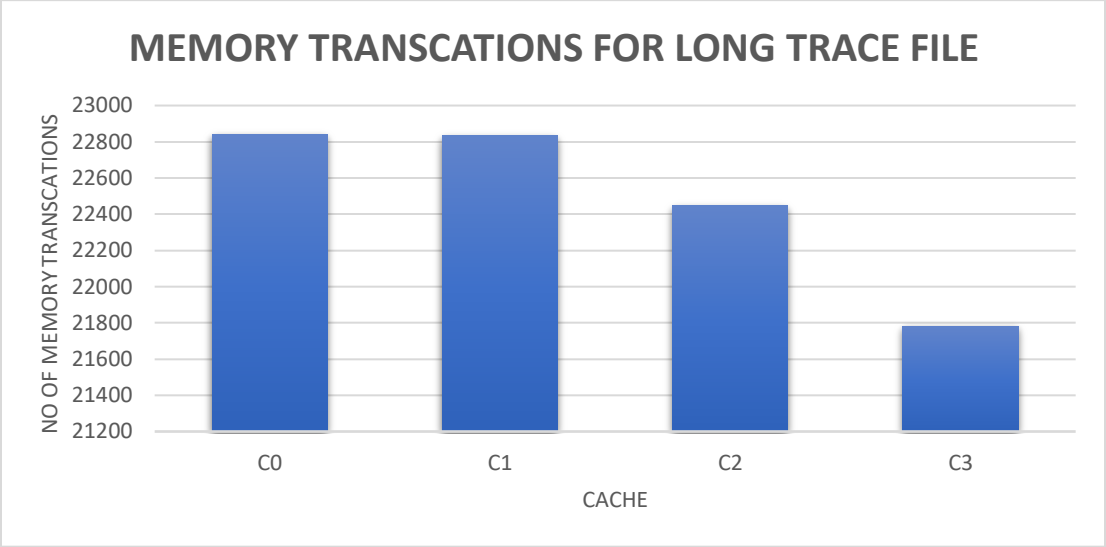
Project 2. Coherence Protocols

1 A) Implemented Modified MSI and here is the output of the simulator for debug trace file



```
===== 506 Personal information =====
Name: Ashish Tummuri
Unity ID: atummur
ECE492 Students?: NO
===== 506 SMP Simulator configuration =====
L1_SIZE: 8192
L1_ASSOC: 8
L1_BLOCKSIZE: 64
NUMBER OF PROCESSORS: 4
COHERENCE PROTOCOL: MSI
TRACE FILE:  ../trace/canneal.04t.debug
============ Simulation results (Cache 0) ============
01. number of reads:                          2339
02. number of read misses:                    446
03. number of writes:                         269
04. number of write misses:                   14
05. total miss rate:                          17.64%
06. number of writebacks:                     0
07. number of memory transactions:            460
08. number of invalidations:                  398
09. number of flushes:                        0
10. number of BusRdX:                         14
============ Simulation results (Cache 1) ============
01. number of reads:                          2341
02. number of read misses:                    407
03. number of writes:                         229
04. number of write misses:                   12
05. total miss rate:                          16.30%
06. number of writebacks:                     1
07. number of memory transactions:            420
08. number of invalidations:                  366
09. number of flushes:                        0
10. number of BusRdX:                         12
============ Simulation results (Cache 2) ============
01. number of reads:                          2396
02. number of read misses:                    373
03. number of writes:                         253
04. number of write misses:                   12
05. total miss rate:                          14.53%
06. number of writebacks:                     0
07. number of memory transactions:            385
08. number of invalidations:                  323
09. number of flushes:                        0
10. number of BusRdX:                         12
============ Simulation results (Cache 3) ============
01. number of reads:                          1969
02. number of read misses:                    449
03. number of writes:                         204
04. number of write misses:                   13
05. total miss rate:                          21.26%
06. number of writebacks:                     3
07. number of memory transactions:            465
08. number of invalidations:                  362
09. number of flushes:                        0
10. number of BusRdX:                         13
```

1 B) Plot of Memory Transactions of Long trace file:



2 A) Implemented Dragon Protocol and here is the output of the simulator for debug trace file

```
===== 506 Personal information =====
Name: Ashish Tummuri
Unity ID: atummur
ECE492 Students?: NO
===== 506 SMP Simulator configuration =====
L1_SIZE: 8192
L1_ASSOC: 8
L1_BLOCKSIZE: 64
NUMBER OF PROCESSORS: 4
COHERENCE PROTOCOL: Dragon
TRACE FILE:  ../trace/canneal.04t.debug
============ Simulation results (Cache 0) ============
01. number of reads:                          2339
02. number of read misses:                    235
03. number of writes:                         269
04. number of write misses:                   3
05. total miss rate:                          9.13%
06. number of writebacks:                     7
07. number of memory transactions:            245
08. number of interventions:                  43
09. number of flushes:                        0
10. number of Bus Transactions(BusUpd):       18
============ Simulation results (Cache 1) ============
01. number of reads:                          2341
02. number of read misses:                    230
03. number of writes:                         229
04. number of write misses:                   2
05. total miss rate:                          9.03%
06. number of writebacks:                     9
07. number of memory transactions:            241
08. number of interventions:                  41
09. number of flushes:                        0
10. number of Bus Transactions(BusUpd):       20
============ Simulation results (Cache 2) ============
01. number of reads:                          2396
02. number of read misses:                    220
03. number of writes:                         253
04. number of write misses:                   2
05. total miss rate:                          8.38%
06. number of writebacks:                     6
07. number of memory transactions:            228
08. number of interventions:                  45
09. number of flushes:                        0
10. number of Bus Transactions(BusUpd):       15
============ Simulation results (Cache 3) ============
01. number of reads:                          1969
02. number of read misses:                    233
03. number of writes:                         204
04. number of write misses:                   0
05. total miss rate:                          10.72%
06. number of writebacks:                     13
07. number of memory transactions:            246
08. number of interventions:                  70
09. number of flushes:                        0
10. number of Bus Transactions(BusUpd):       13
```

2 B)

- To compare these two, we look at several key metrics that inform us about the performance and efficiency of each protocol. Here's a brief explanation of the results based on the data provided:
- **Total Miss Rate**: The total miss rate reflects the percentage of memory accesses that result in a cache miss. A lower miss rate generally indicates better performance because it means fewer accesses require slower memory fetches. total miss rates show that the Dragon protocol has a significantly lower total miss rate for each cache compared to the MSI protocol. This indicates that the Dragon protocol is more effective at reducing cache misses, which would typically result in better overall performance due to less frequent access to slower main memory.
- **Number of Writebacks**: Writebacks occur when a modified cache line is replaced and needs to be written back to memory. Fewer writebacks are typically better because they mean the system is doing less redundant work. The Modifies MSI protocol has fewer writebacks across all caches, which could indicate more efficient utilization of cache lines.
- **Number of Interventions and Invalidations**: Interventions and invalidations are mechanisms used to maintain cache coherence. Interventions occur when a cache forwards a copy of data from its own cache to another cache, and invalidations occur when a cache line is marked as invalid due to updates from other caches. The Dragon protocol has fewer interventions and invalidations in all caches, suggesting that it might handle coherence with less overhead than MSI.
- **Memory Transactions**: This is the count of actual memory read and write operations due to cache misses. Fewer memory transactions indicate better cache performance. The Dragon protocol results in fewer memory transactions in all caches, suggesting it is more effective at reducing the load on memory.

- In summary, as showing the below two protocol output comparisons, the Dragon protocol appears to perform slightly better than the Modified MSI protocol in terms of total miss rate, number of writebacks, number of memory transactions, and bus transactions. It also seems to manage coherence with fewer interventions and invalidations. However, the differences are not dramatic, suggesting that both protocols perform similarly, with Dragon having a slight edge in efficiency.

```
./smp_cache 8192 8 64 4 0 ../trace/canneal.04t.longTrace
===== 506 Personal information =====
Name: Ashish Tummuri
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===== 506 SMP Simulator configuration =====
L1_SIZE: 8192
L1_ASSOC: 8
L1_BLOCKSIZE: 64
NUMBER OF PROCESSORS: 4
COHERENCE PROTOCOL: MSI
TRACE FILE:  ../trace/canneal.04t.longTrace
============ Simulation results (Cache 0) ============
01. number of reads:                            112661
02. number of read misses:                      21453
03. number of writes:                           11942
04. number of write misses:                     689
05. total miss rate:                            17.77%
06. number of writebacks:                       700
07. number of memory transactions:              22842
08. number of invalidations:                    20585
09. number of flushes:                          93
10. number of BusRdX:                           689
============ Simulation results (Cache 1) ============
01. number of reads:                            110830
02. number of read misses:                      21491
03. number of writes:                           11710
04. number of write misses:                     663
05. total miss rate:                            18.08%
06. number of writebacks:                       679
07. number of memory transactions:              22833
08. number of invalidations:                    20666
09. number of flushes:                          77
10. number of BusRdX:                           663
============ Simulation results (Cache 2) ============
01. number of reads:                            114938
02. number of read misses:                      21043
03. number of writes:                           12383
04. number of write misses:                     690
05. total miss rate:                            17.07%
06. number of writebacks:                       714
07. number of memory transactions:              22447
08. number of invalidations:                    19988
09. number of flushes:                          97
10. number of BusRdX:                           690
============ Simulation results (Cache 3) ============
01. number of reads:                            113428
02. number of read misses:                      20337
03. number of writes:                           12108
04. number of write misses:                     684
05. total miss rate:                            16.74%
06. number of writebacks:                       759
07. number of memory transactions:              21780
08. number of invalidations:                    18552
09. number of flushes:                          76
10. number of BusRdX:                           684
```

```
./smp_cache 8192 8 64 4 1 ../trace/canneal.04t.longTrace
===== 506 Personal information =====
Name: Ashish Tummuri
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===== 506 SMP Simulator configuration =====
L1_SIZE: 8192
L1_ASSOC: 8
L1_BLOCKSIZE: 64
NUMBER OF PROCESSORS: 4
COHERENCE PROTOCOL: Dragon
TRACE FILE:  ../trace/canneal.04t.longTrace
============ Simulation results (Cache 0) ============
01. number of reads:                            112661
02. number of read misses:                      9614
03. number of writes:                           11942
04. number of write misses:                     5
05. total miss rate:                            7.72%
06. number of writebacks:                       1006
07. number of memory transactions:              10625
08. number of interventions:                    1994
09. number of flushes:                          15
10. number of Bus Transactions(BusUpd):         1290
============ Simulation results (Cache 1) ============
01. number of reads:                            110830
02. number of read misses:                      9472
03. number of writes:                           11710
04. number of write misses:                     6
05. total miss rate:                            7.73%
06. number of writebacks:                       979
07. number of memory transactions:              10457
08. number of interventions:                    1978
09. number of flushes:                          19
10. number of Bus Transactions(BusUpd):         1309
============ Simulation results (Cache 2) ============
01. number of reads:                            114938
02. number of read misses:                      9456
03. number of writes:                           12383
04. number of write misses:                     6
05. total miss rate:                            7.43%
06. number of writebacks:                       984
07. number of memory transactions:              10446
08. number of interventions:                    1937
09. number of flushes:                          17
10. number of Bus Transactions(BusUpd):         1404
============ Simulation results (Cache 3) ============
01. number of reads:                            113428
02. number of read misses:                      9568
03. number of writes:                           12108
04. number of write misses:                     4
05. total miss rate:                            7.62%
06. number of writebacks:                       986
07. number of memory transactions:              10558
08. number of interventions:                    1977
09. number of flushes:                          10
10. number of Bus Transactions(BusUpd):         1304
```