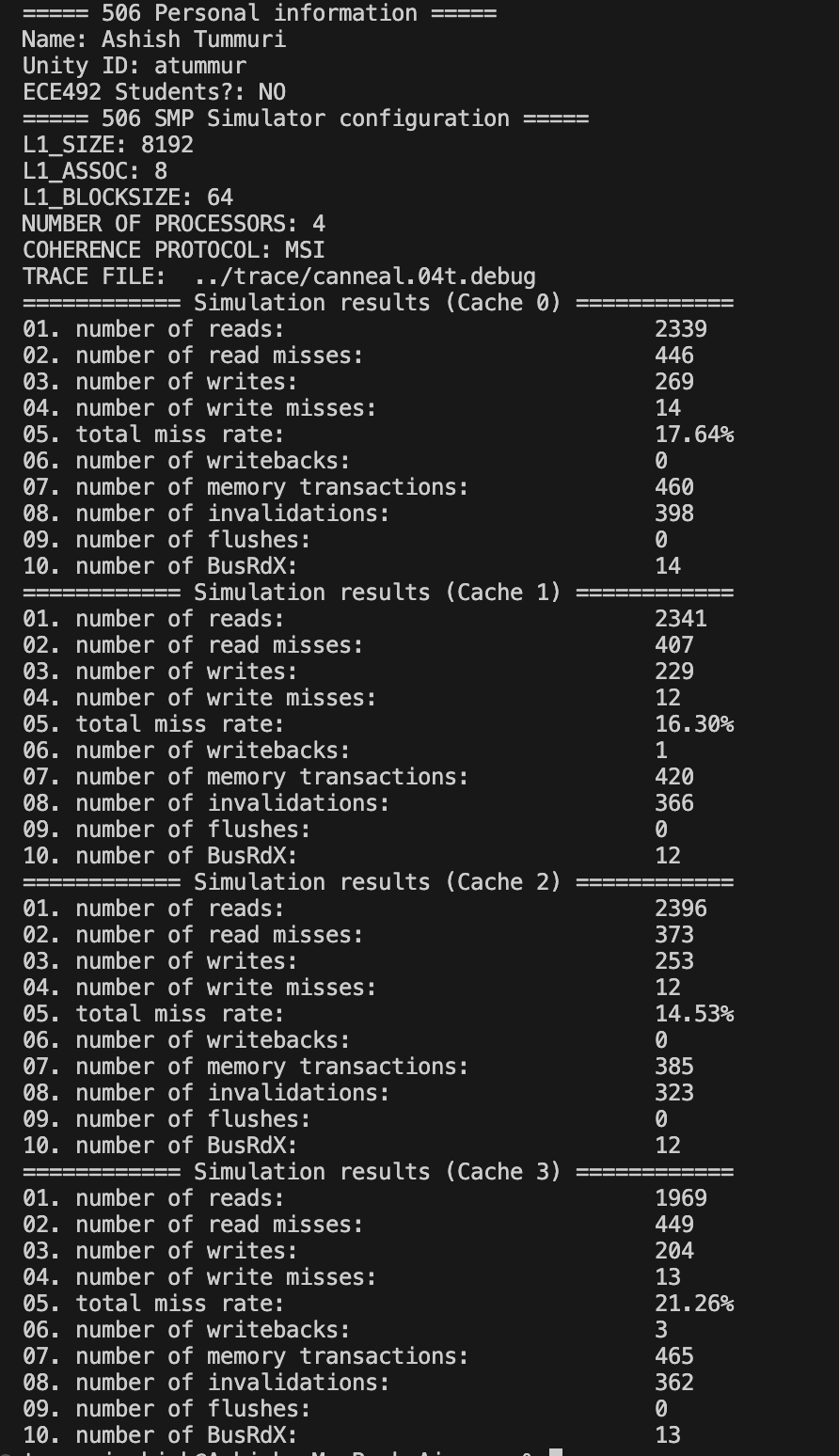
**ECE/CSC 406/506: Architecture of Parallel Computers**

**Project 2. Coherence Protocols**

1. A) Implemented Modified MSI and here is the output of the simulator for debug trace file



1. B) Plot of Memory Transactions of Long trace file:

2 A) Implemented Dragon Protocol and here is the output of the simulator for debug trace file

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated2 B)

A screenshot of a computer

Description automatically generated2 B)

jh