گزارشکار آزمایش ۵

: mux_2to1

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux_2to1 is
port (
S,I0,I1 : in std_logic;
Y : out std_logic
);
end mux_2to1;
architecture structure of mux_2to1 is
signal C0,C1 : std_logic;
begin
C0 <= not S and I0;
C1 <= S and I1;
Y <= C0 or C1;
end structure;
```

: DFF

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity DFF is
port(
        Clk : in std_logic;
        reset : in std_logic;
        D : in std_logic;
        Q : out std_logic
        );
end DFF;
```

```
architecture Behavioral of DFF is
begin
process(Clk, reset)
                begin
                if (reset = '0') then Q <= '0';
                elsif (rising_edge(Clk)) then Q <= D;
                end if;
        end process;
end Behavioral;
```

: PIOS_3bits

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity PISO_3bits is
port(
A: in std_logic_vector(2 downto 0);
S,Clk,reset : in std_logic;
B : out std_logic
);
end PISO_3bits;
architecture structure of PISO_3bits is
component mux_2to1 is
port (
S,I0,I1 : in std_logic;
Y : out std_logic
);
end component mux_2to1;
component DFF is
port(
```

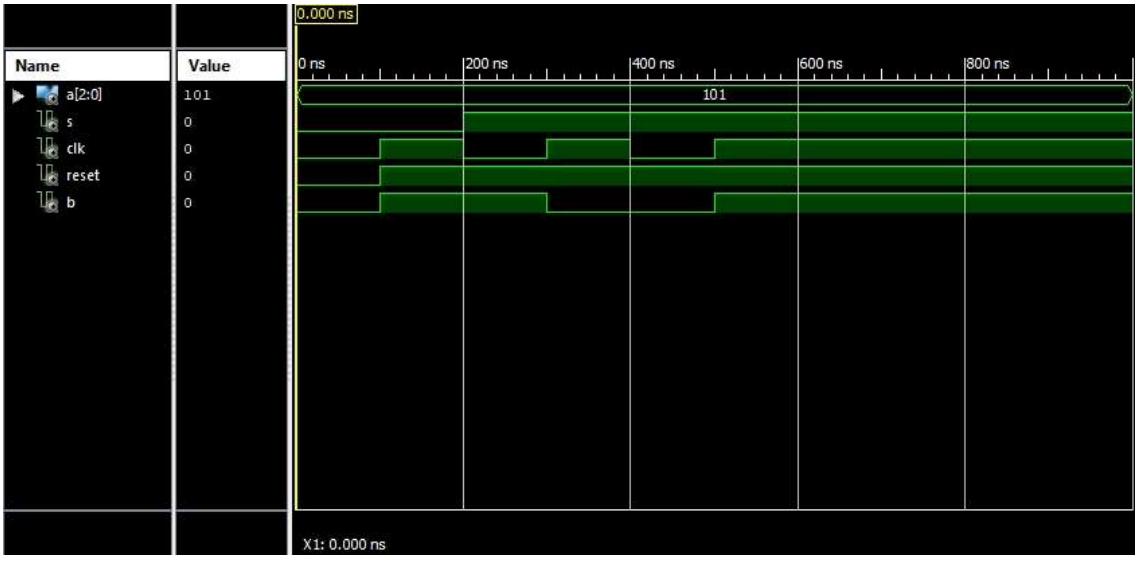
```
        Clk : in std_logic;
        reset : in std_logic;
        D : in std_logic;
        Q : out std_logic
        );
end component DFF;
signal s0,s1,s2,s3,s4 : std_logic;
begin
mux_2 : mux_2to1 port map (S =>S , I0 => A(2),I1 => '0' , Y => s0);
DFF_2 : DFF port map (Clk => Clk , reset => reset , D => s0 , Q =>s1);
mux_1 : mux_2to1 port map (S =>S , I0 => A(1),I1 => s1 , Y => s2);
DFF_1 : DFF port map (Clk => Clk , reset => reset , D => s2 , Q =>s3);
mux_0 : mux_2to1 port map (S =>S , I0 => A(0),I1 => s3 , Y => s4);
DFF_0 : DFF port map (Clk => Clk , reset => reset , D => s4 , Q =>B);
end structure;
```

: PIOS_3bits_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY PISO_3bits_tb IS
END PISO_3bits_tb;
ARCHITECTURE test OF PISO_3bits_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT PISO_3bits
   PORT(
      A : IN  std_logic_vector(2 downto 0);
      S : IN  std_logic;
      Clk : IN  std_logic;
      reset : IN  std_logic;
```

```
        B : OUT  std_logic
       );
   END COMPONENT;
  --Inputs
  signal A : std_logic_vector(2 downto 0);
  signal S : std_logic ;
  signal Clk : std_logic ;
  signal reset : std_logic ;
          --Outputs
  signal B : std_logic;
BEGIN
          -- Instantiate the Unit Under Test (UUT)
  uut: PISO_3bits PORT MAP (
        A => A,
        S => S,
        Clk => Clk,
        reset => reset,
        B => B
       );
 A <= "101";
 S <= '0' , '1' after 200 ns;
 clk <= '0' ,'1' after 100 ns , '0' after 200 ns , '1' after 300 ns , '0' after 400 ns , '1' after 500 ns;
 reset <= '0' , '1' after 100 ns;
END;
```

خروجی شبیه سازی PIOS_3bits_tb :



شمای مدار طراحی شده :