گزارشکار آزمایش ۸

: divider

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
entity divider is
   Port ( dividend : IN  std_logic_vector(7 downto 0);
       divisor : IN  std_logic_vector(3 downto 0);
       zero_error : OUT  std_logic;
       Quotient : OUT  std_logic_vector(7 downto 0);
       Remainder : OUT  std_logic_vector(3 downto 0)
      );
end divider;
architecture Behavioral of divider is
begin
          process(dividend, divisor) is
                    variable B : STD_LOGIC_VECTOR (3 downto 0);
                    variable A: STD_LOGIC_VECTOR (7 downto 0);
                    variable R : STD_LOGIC_VECTOR (3 downto 0);
                    variable flag :  STD_LOGIC ;
          begin
            R:="0000";
            flag:='0';
                    R(0):= dividend(7);
                    A(7 downto 1) := dividend (6 downto 0);
                    A(0) := '0';
                    B := divisor;
                    if (B = "0000") then
```

```
                zero_error <= '1';
                Remainder <="XXXX";
                quotient <= "XXXXXXXX";
        else
            zero_error <= '0';
             for sc in 0 to 7 loop
                  if( R >= B or flag ='1') then
             R := R + (not B) + "0001" ;
                flag := R(3);
                R := R(R'left - 1 downto 0) & A(7);
                A := A(A'left - 1 downto 0) & '1';
            else
             flag := R(3);
              R := R(R'left - 1 downto 0) & A(7);
                A := A(A'left - 1 downto 0) & '0';
        end if;
                end loop;
                Remainder(2 downto 0) <= R(3 downto 1);
                Remainder(3)  <= flag;
                quotient <= A;
            end if;
    end process;
end Behavioral;
```

: divider_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY divider_tb IS
END divider_tb;
```

```
ARCHITECTURE test OF divider_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT divider
   PORT(
       dividend : IN  std_logic_vector(7 downto 0);
       divisor : IN  std_logic_vector(3 downto 0);
       zero_error : OUT  std_logic;
       Quotient : OUT  std_logic_vector(7 downto 0);
       Remainder : OUT  std_logic_vector(3 downto 0)
      );
   END COMPONENT;
  --Inputs
  signal dividend : std_logic_vector(7 downto 0) := (others => '0');
  signal divisor : std_logic_vector(3 downto 0) := (others => '0');
          --Outputs
  signal zero_error : std_logic;
  signal Quotient : std_logic_vector(7 downto 0);
  signal Remainder : std_logic_vector(3 downto 0);
BEGIN
          -- Instantiate the Unit Under Test (UUT)
  uut: divider PORT MAP (
        dividend => dividend,
        divisor => divisor,
        zero_error => zero_error,
        Quotient => Quotient,
        Remainder => Remainder
       );
 dividend<= "11100000", "11111111" after 200 ns , "10010000" after 400 ns;
 divisor<="1100"  ; END;
```

خروجی شبیه سازی divider_tb :