گزارشکار آزمایش۲

گیت Not

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity not_gate is
port(
A: in std_logic;
B :out std_logic
);
end not_gate;
architecture Behavioral of not_gate is
begin
B <= not A ;
end Behavioral;
```

گیت And با ۲ ورودی

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity and_gate is
port(
A, B: in std_logic;
o :out std_logic
);
end and_gate;
architecture Behavioral of and_gate is
begin
o <= A and B ;
end Behavioral;
```

گیت Nor

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity nor_gate is
port(
A, B: in std_logic;
o :out std_logic
);
end nor_gate;
architecture Behavioral of nor_gate is
begin
o <= A nor B ;
end Behavioral;
```

گیت Or با ۲ ورودی

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity or_gate is
port(
A, B: in std_logic;
o :out std_logic
);
end or_gate;
architecture Behavioral of or_gate is
begin
o <= A or B ;
end Behavioral;
```

Comparator_1 bit

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator_1bit is
 port(
I, J, gt,eq,lt: in std_logic;
  I_GT_J,I_EQ_J,I_LT_J :out std_logic
);
end comparator_1bit;
architecture structure of comparator_1bit is
component and_gate is
port(
A, B: in std_logic;
o :out std_logic
);
End Component and_gate;
component or_gate is
port(
A, B: in std_logic;
o :out std_logic
);
End Component or_gate;
component nor_gate is
port(
A, B: in std_logic;
o :out std_logic
);
End Component nor_gate;
```

```
component not_gate is
port(
A: in std_logic;
B :out std_logic
);
End Component not_gate;
signal nI ,nJ ,s0,s1,s2,s3,s4: std_logic;
begin
not_gate_0: not_gate port map(A => I , B =>nI);
not_gate_1 :not_gate port map (A =>J , B => nJ);
and_gate_0 :and_gate port map (A =>I , B =>nJ ,o =>s0);
and_gate_1 :and_gate port map (A =>nI , B =>J ,o =>s2);
nor_gate_0 :nor_gate port map (A =>s0 , B =>s2 ,o=>s1);
and_gate_2 :and_gate port map (A=>s1 , B=>eq , o =>I_EQ_J);
and_gate_3 :and_gate port map (A=>s1 , B=>gt , o =>s3);
or_gate_0 : or_gate port map (A=>s0 , B=>s3 , o=>I_GT_J);
and_gate_4 :and_gate port map (A=>s1 , B=>lt , o =>s4);
or_gate_1 : or_gate port map (A=>s2 , B=>s4 , o=>I_LT_J);
end structure;
```

Comparator_4bits

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator_4bits is
 PORT(
        A : IN  std_logic_vector(3 downto 0);
        B : IN  std_logic_vector(3 downto 0);
        GT : IN  std_logic;
        EQ : IN  std_logic;
```

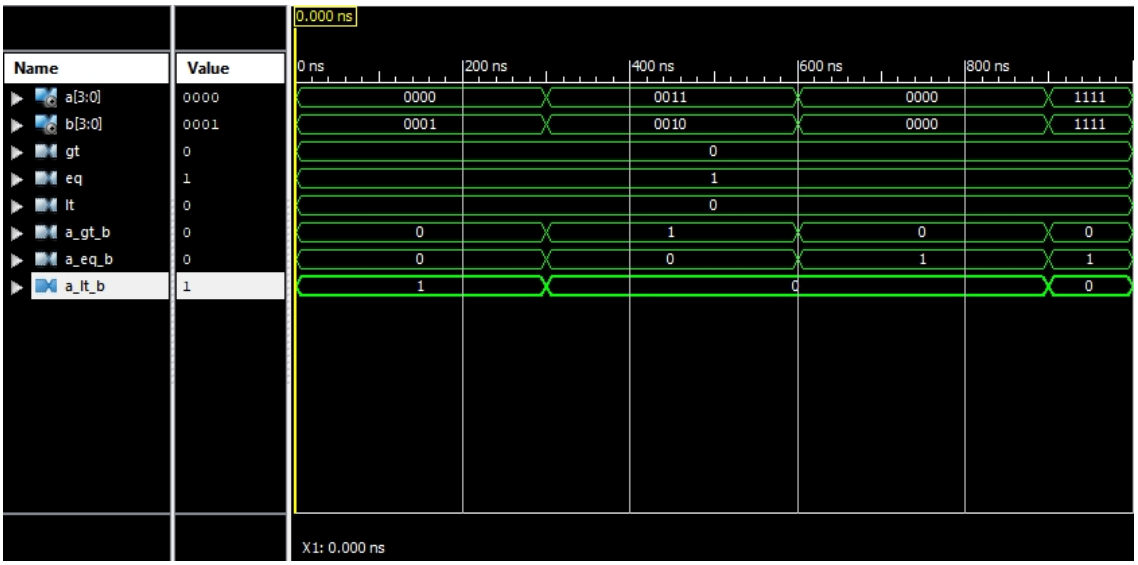
```
        LT : IN  std_logic;
        A_GT_B : OUT  std_logic;
        A_EQ_B : OUT  std_logic;
        A_LT_B : OUT  std_logic
       );
end comparator_4bits;
architecture structure of comparator_4bits is
  COMPONENT comparator_1bit
  port(
I, J, gt,eq,lt: in std_logic;
 I_GT_J,I_EQ_J,I_LT_J :out std_logic
);
   END COMPONENT;
signal s0,s1,s2,s3,s4,s5,s6,s7,s8 : std_logic;
begin
compare_4th_digit : comparator_1bit port map
(I=>A(0),J=>B(0),gt=>(GT),eq=>(EQ),lt=>(LT),I_GT_J =>(s0),I_EQ_J =>(s1),I_LT_J =>(s2));
compare_3th_digit : comparator_1bit port map
(I=>A(1),J=>B(1),gt=>(s0),eq=>(s1),lt=>(s2),I_GT_J =>(s3),I_EQ_J =>(s4),I_LT_J =>(s5));
compare_2th_digit : comparator_1bit port map
(I=>A(2),J=>B(2),gt=>(s3),eq=>(s4),lt=>(s5),I_GT_J =>(s6),I_EQ_J =>(s7),I_LT_J =>(s8));
compare_1th_digit : comparator_1bit port map
(I=>A(3),J=>B(3),gt=>(s6),eq=>(s7),lt=>(s8),I_GT_J =>(A_GT_B),I_EQ_J =>(A_EQ_B),I_LT_J
=>(A_LT_B));
end structure;
```

Comparator_4 bits_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY comparator_4bits_tb IS
END comparator_4bits_tb;
ARCHITECTURE test OF comparator_4bits_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT comparator_4bits
   PORT(
        A : IN  std_logic_vector(3 downto 0);
        B : IN  std_logic_vector(3 downto 0);
        GT : IN  std_logic;
        EQ : IN  std_logic;
        LT : IN  std_logic;
        A_GT_B : OUT  std_logic;
        A_EQ_B : OUT  std_logic;
        A_LT_B : OUT  std_logic
       );
   END COMPONENT;
  --Inputs
  signal A : std_logic_vector(3 downto 0);
  signal B : std_logic_vector(3 downto 0);
  signal GT : std_logic ;
  signal EQ : std_logic ;
  signal LT : std_logic ;
--Outputs
   signal A_GT_B : std_logic;
  signal A_EQ_B : std_logic;
```

```
  signal A_LT_B : std_logic;
BEGIN                                                                    --
Instantiate the Unit Under Test (UUT)
  uut: comparator_4bits PORT MAP (
        A => A,
        B => B,
        GT => GT,
        EQ => EQ,
        LT => LT,
        A_GT_B => A_GT_B,
        A_EQ_B => A_EQ_B,
        A_LT_B => A_LT_B
       );
  stim: process
 begin
    GT <='0'; EQ <= '1' ;LT <='0' ;
 A <= "0000" ; B <= "0001"; wait for 300ns;
 A <= "0011" ; B <= "0010"; wait for 300ns;
 A <= "0000" ; B <= "0000"; wait for 300ns;
A <= "1111" ; B <= "1111"; wait for 100ns;
end process;
END;
```

خروجی شبیه سازی comparator_4 bits_tb



گیت And با ۴ ورودی

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity and_gate_4 is
Port (
        Iand0 , Iand1, Iand2, Iand3: in std_logic;
        Oand: out std_logic
);
End Entity and_gate_4;
Architecture gatelevel of and_gate_4 is
Begin
        Oand <= Iand0 and Iand1 and Iand2 and Iand3;
end gatelevel;
```

Encoder4x2

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Encoder4x2 is
Port (
        I0, I1, I2, I3: in std_logic;
        y1, y0: out std_logic
);
end Encoder4x2;
architecture structure of Encoder4x2 is
component and_gate_4 is --and component
Port (
        Iand0 , Iand1, Iand2, Iand3: in std_logic;
```

```
        Oand: out std_logic
);
End component and_gate_4;
component not_gate is --not component
Port (
        A : in std_logic;
        B : out std_logic
);
End component not_gate;
component or_gate is --or component
Port (
        A , B: in std_logic;
        o: out std_logic
);
End component or_gate;
signal NI0 , NI1, NI2, NI3 : std_logic; --not signals
signal a1 , a2, a3: std_logic; --and signals
begin
        not_gate_instance0: not_gate port map (A=>I0, B=>NI0); --not instances
        not_gate_instance1: not_gate port map (A=>I1, B=>NI1);
        not_gate_instance2: not_gate port map (A=>I2, B=>NI2);
        not_gate_instance3: not_gate port map (A=>I3, B=>NI3);
        and_gate_instance0: and_gate_4 port map (Iand0=>NI0, Iand1=>NI1, Iand2=>I2,
Iand3=>NI3, Oand=>a1); --and instances
        and_gate_instance1: and_gate_4 port map (Iand0=>NI0, Iand1=>NI1, Iand2=>NI2,
Iand3=>I3, Oand=>a2);
        and_gate_instance2: and_gate_4 port map (Iand0=>NI0, Iand1=>I1, Iand2=>NI2,
Iand3=>NI3, Oand=>a3);
```

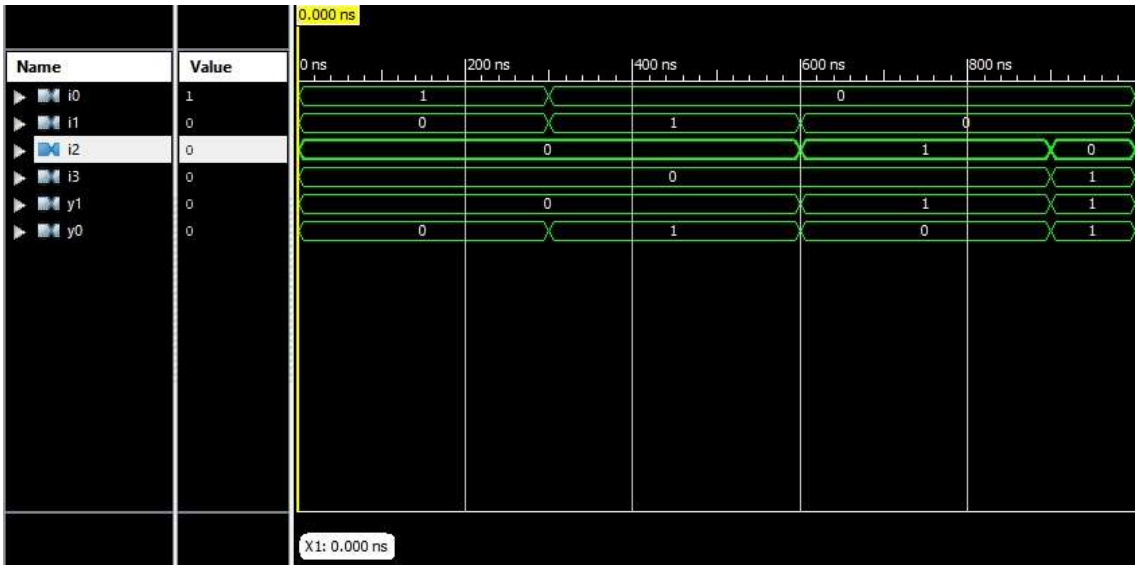
```
        or_gate_instance0: or_gate port map (A=>a1, B=>a2, o=>y1); --or_instances
        or_gate_instance1: or_gate port map (A=>a3, B=>a2, o=>y0);
end structure;
```

Encoder4x2_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Encoder4x2_tb IS
END Encoder4x2_tb;
ARCHITECTURE test OF Encoder4x2_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT Encoder4x2
   PORT(
       I0 : IN  std_logic;
       I1 : IN  std_logic;
       I2 : IN  std_logic;
       I3 : IN  std_logic;
       y1 : OUT  std_logic;
       y0 : OUT  std_logic
      );
   END COMPONENT;
  --Inputs
  signal I0 : std_logic;
  signal I1 : std_logic;
  signal I2 : std_logic;
  signal I3 : std_logic;
        --Outputs
  signal y1 : std_logic;
  signal y0 : std_logic;
```

```
BEGIN
        -- Instantiate the Unit Under Test (UUT)
  uut: Encoder4x2 PORT MAP (
       I0 => I0,
       I1 => I1,
       I2 => I2,
       I3 => I3,
       y1 => y1,
       y0 => y0
      );
           stim: process
           begin
   I0 <='1' ;I1 <='0' ;I2 <='0' ;I3 <='0' ;wait for 300ns;
           I0 <='0' ;I1 <='1' ;I2 <='0' ;I3 <='0' ;wait for 300ns;
           I0 <='0' ;I1 <='0' ;I2 <='1' ;I3 <='0' ;wait for 300ns;
           I0 <='0' ;I1 <='0' ;I2 <='0' ;I3 <='1' ;wait for 100ns;
           end process;
END;
```

خروجی شبیه سازی Encoder4x2_tb



گیت And با ۳ ورودی

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity and_gate_3 is
port(
A,B,C : in std_logic;
o : out std_logic
);
end and_gate_3;
architecture structure of and_gate_3 is
component and_gate is
port(
A, B: in std_logic;
o :out std_logic
);
End Component and_gate;
signal s1 : std_logic;
begin
and_0 : and_gate port map (A=>A, B=>B, o=>s1);
and_1 : and_gate port map (A=>s1, B=>C, o=>o);
end structure;
```

گیت Or با ۴ ورودی

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity or_gate_4 is
port(
A,B,C,D : in std_logic;
o : out std_logic
```

```
);
end or_gate_4;
architecture structure of or_gate_4 is
component or_gate is
port(
A, B: in std_logic;
o :out std_logic
);
End Component or_gate;
signal s1,s2 : std_logic;
begin
or_0 : or_gate port map (A=>A, B=>B, o=>s1);
or_1 : or_gate port map (A=>C, B=>D, o=>s2);
or_2 : or_gate port map (A=>s1, B=>s2, o=>o);
end structure;
```

---

mux_4to1

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux_4to1 is
port (
S0,S1,I0,I1,I2,I3 : in std_logic;
Y : out std_logic
);
end mux_4to1;
architecture structure of mux_4to1 is
component not_gate is
port(
A: in std_logic;
```

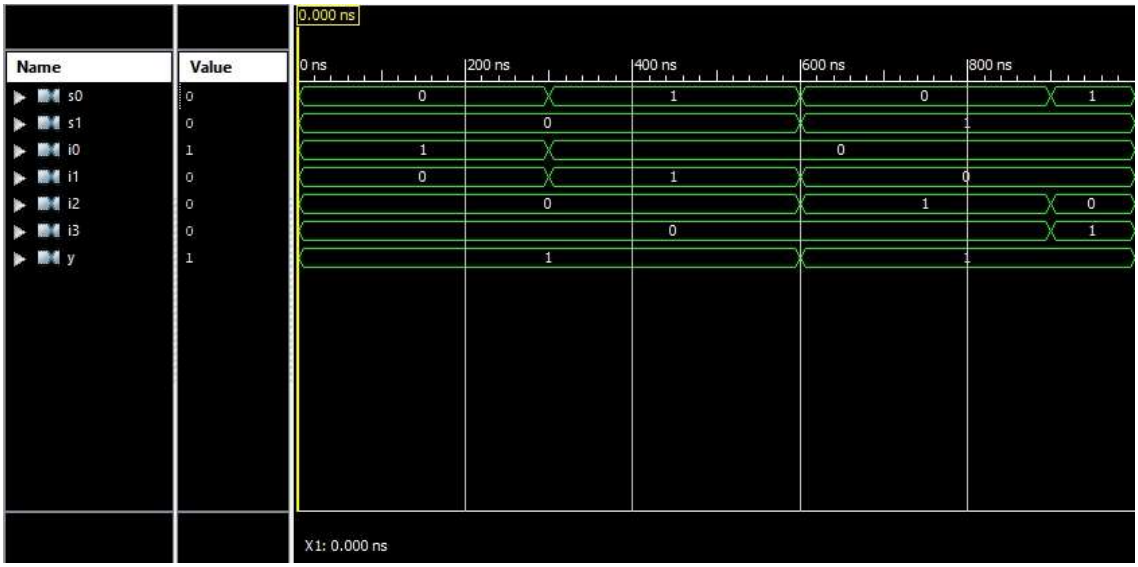
```
B :out std_logic
);
End Component not_gate;
component and_gate_3 is
port(
A, B, C: in std_logic;
o :out std_logic
);
End Component and_gate_3;
component or_gate_4
port(
A, B, C, D: in std_logic;
o :out std_logic
);
End Component or_gate_4;
signal s0_not,s1_not : std_logic;
signal C0,C1,C2,C3 : std_logic;
begin
not_0 : not_gate port map ( A=>S0, B=>s0_not);
not_1 : not_gate port map ( A=>S1, B=>s1_not);
and_0 : and_gate_3 port map ( A=>I0, B=>s1_not, C=>s0_not, o=>C0);
and_1 : and_gate_3 port map ( A=>I1, B=>s1_not, C=>S0, o=>C1);
and_2 : and_gate_3 port map ( A=>I2, B=>S1, C=>s0_not, o=>C2);
and_3 : and_gate_3 port map ( A=>I3, B=>S1, C=>S0, o=>C3);
or_0 : or_gate_4 port map (A=>C0, B=>C1, C=>C2, D=>C3, o=>Y);
end structure;
```

Mux_4to1_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY mux_4to1_tb IS
END mux_4to1_tb;
ARCHITECTURE test OF mux_4to1_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT mux_4to1
   PORT(
      S0 : IN  std_logic;
      S1 : IN  std_logic;
      I0 : IN  std_logic;
      I1 : IN  std_logic;
      I2 : IN  std_logic;
      I3 : IN  std_logic;
      Y : OUT  std_logic
       );
   END COMPONENT;
  --Inputs
  signal S0 : std_logic;
  signal S1 : std_logic;
  signal I0 : std_logic;
  signal I1 : std_logic;
  signal I2 : std_logic;
  signal I3 : std_logic;
          --Outputs
  signal Y : std_logic;
BEGIN
-- Instantiate the Unit Under Test (UUT)
```

```
  uut: mux_4to1 PORT MAP (
        S0 => S0,
        S1 => S1,
        I0 => I0,
        I1 => I1,
        I2 => I2,
        I3 => I3,
        Y => Y
       );
  stim: process
             begin
    s0<= '0' ; s1 <= '0'; I0 <='1' ;I1 <='0' ;I2 <='0' ;I3 <='0' ;wait for 300ns;
            s0<= '1' ; s1 <= '0'; I0 <='0' ;I1 <='1' ;I2 <='0' ;I3 <='0' ;wait for 300ns;
            s0<= '0' ; s1 <= '1'; I0 <='0' ;I1 <='0' ;I2 <='1' ;I3 <='0' ;wait for 300ns;
            s0<= '1' ; s1 <= '1'; I0 <='0' ;I1 <='0' ;I2 <='0' ;I3 <='1' ;wait for 100ns;
            end process;
END;
```

خروجی شبیه سازی mux_4to1_tb



Decoder2x4

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Decoder2x4 is
Port (
I0, I1: in std_logic;
D0, D1, D2, D3: out std_logic
);
end Decoder2x4;
architecture structure of Decoder2x4 is
component and_gate is --and component
Port (
A , B: in std_logic;
o: out std_logic
);
End component and_gate;
component not_gate is --not component
Port (
A : in std_logic;
B : out std_logic
);
End component not_gate;
signal NI0 , NI1 : std_logic;
begin
not_gate_instance0: not_gate port map (A=>I0, B=>NI0);
not_gate_instance1: not_gate port map (A=>I1, B=>NI1);
and_gate_instance0: and_gate port map (A=>NI0, B=>NI1, o=>D0);
and_gate_instance1: and_gate port map (A=>I0, B=>NI1, o=>D1);
```

```
and_gate_instance2: and_gate port map (A=>NI0, B=>I1, o=>D2);
and_gate_instance3: and_gate port map (A=>I0, B=>I1, o=>D3);
end structure;
```

Decoder2x4_tb

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Decoder2x4_tb IS
END Decoder2x4_tb;
ARCHITECTURE test OF Decoder2x4_tb IS
   -- Component Declaration for the Unit Under Test (UUT)
   COMPONENT Decoder2x4
   PORT(
        I0 : IN  std_logic;
        I1 : IN  std_logic;
        D0 : OUT  std_logic;
        D1 : OUT  std_logic;
        D2 : OUT  std_logic;
        D3 : OUT  std_logic
       );
   END COMPONENT;
  --Inputs
  signal I0 : std_logic;
  signal I1 : std_logic;
--Outputs
  signal D0 : std_logic;
  signal D1 : std_logic;
```

```
  signal D2 : std_logic;
  signal D3 : std_logic;
BEGIN
-- Instantiate the Unit Under Test (UUT)
  uut: Decoder2x4 PORT MAP (
        I0 => I0,
        I1 => I1,
        D0 => D0,
        D1 => D1,
        D2 => D2,
        D3 => D3
       );
 stim: process
 begin
I0 <='0' ;I1 <='0';wait for 300ns;
I0 <='1' ;I1 <='0';wait for 300ns;
I0 <='0' ;I1 <='1';wait for 300ns;
I0 <='1' ;I1 <='1';wait for 100ns;
end process;
END;
```

خروجی شبیه سازی Decoder2x4_tb