

Dylan Bray and Ashkan Vafaei Lab 5 Deliverables

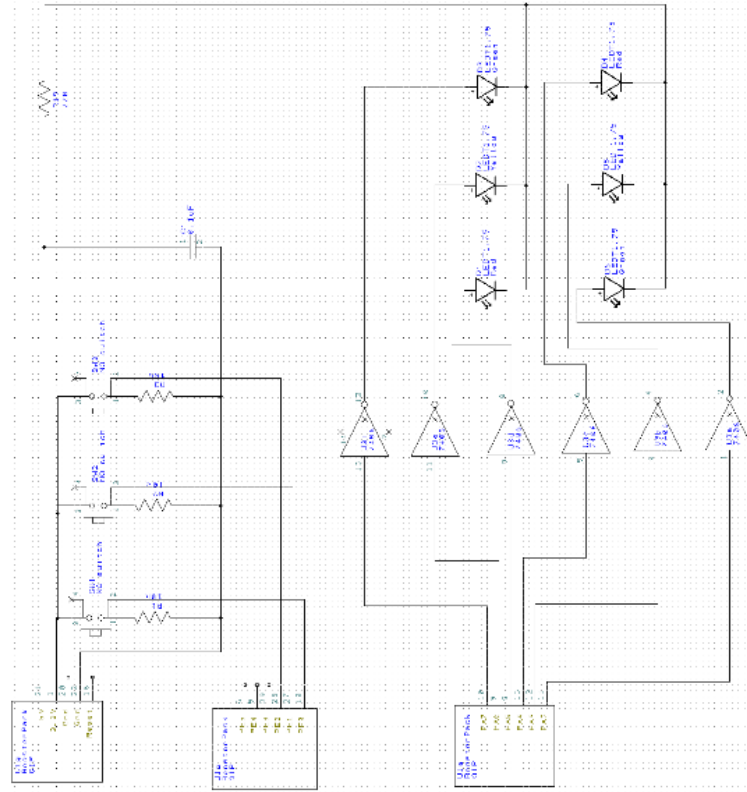
The screenshot displays the Texas Instruments Code Composer Studio (CCS) interface, which is used for developing and debugging embedded systems. The main window is divided into several panes:

- Registers:** A table showing the current state of various registers. The **R15 (PC)** register is highlighted, indicating the current instruction pointer.
- Logic Analyzer:** A large window showing a multi-channel digital signal trace. The trace displays several digital signals (red, green, yellow, and black) over time, with a time scale of 0 s to 12.5 s. The signals show a sequence of logic levels (high and low) corresponding to the execution of the program.
- Source Code:** A window showing the C code being executed. The code includes a `while` loop that delays the system clock using `SysTick_Wait10ms`. The code is as follows:


```

      57 uint32_t startTime = NVIC_ST_CURRENT_R;
      58 do
      59 {
      60     elapsedTime = (startTime - NVIC_ST_CURRENT_R) & 0x00000000;
      61     while(elapsedTime <= delay);
      62 }
      63 // Time delay using busy wait.
      64 // This assumes 50 Mhz system clock.
      65 void SysTick_Wait10ms(uint32_t delay) {
      
```
- Hardware Configuration:** Two windows are open showing the hardware configuration for the **TM4C123** microcontroller. The **Port F Registers** window shows the configuration for the **PF0** pin, which is set to **LOCK: 0x00**, **PDR: 0x00**, and **RCGC2: 0x000000039**. The **Port F Hardware** window shows the configuration for the **PF0** pin, which is set to **LOCK: 0x00**, **PDR: 0x00**, and **RCGC2: 0x000000039**.

The interface also includes a **Command** window at the bottom, which shows the current command being executed: `LA (PORTA & 0x00000080 >> 7 & 0x80) >> 0`. The **Project** window shows the project name **Lab5** and the file **Lab5.uvproj**.



University Of Texas At Austin

Schematic Name: EK-IM4F120XL or EK-TM4C123GXL

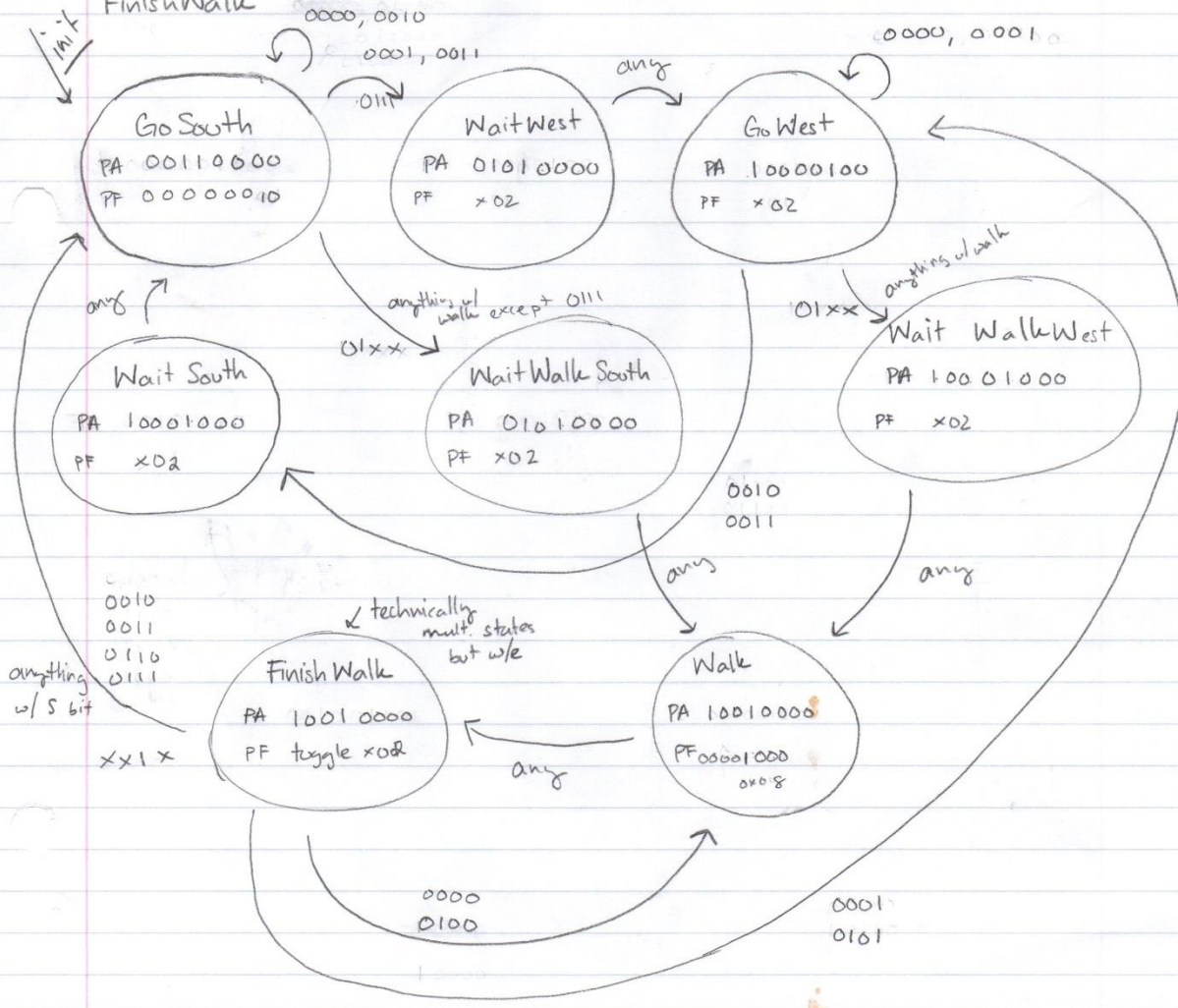
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	South			West			Walk		Sensor		
	G	Y	R	G	Y	R	G	R	South	West	Walk
PA	5	6	7	2	3	4	3	1	1	0	2
	<u>right</u>			<u>left</u>					0010	0001	0100

Go South : 001 1
 Wait South : 000 0
 Go West : 011 3
 Wait West : 010 2
 Wait Walk South : 100 4
 Wait Walk West : 101 5
 Walk : 110 6
 Finish Walk : 111 7

no input: stay same
 Priority: different state above current
 walks above S/W
 South above west



current state	next state	output	wait
① Go South	0000, 0010 Go South 0001, 0011 Wait West 01xx Wait Walk South	PA 00110000 PF 0000 0010	1.5 s
② Wait West	Go West	PA 01010000 PF x02	.25 s
③ Go West	0000, 0001 Go West 0010, 0011 Wait South 01xx Wait Walk West	PA 10000100 PF x02	1.5 s
④ Wait South	Go South	PA 10001000 PF x02	.25 s
⑤ Wait Walk South	Walk	PA 01010000 PF x02	.25 s
⑥ Wait Walk west	Walk	PA 10001000 PF x02	.25 s
⑦ Walk	Finish Walk	PA 10010000 PF x08	.75 s
⑧ Finish Walk	xx1x Go South 0000, 0100 Walk 0101, 0001 Go West	PA 10010000 PF toggle x02	.75 s