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November 2013

FQP30N06L

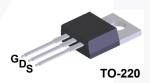
N-Channel QFET[®] MOSFET 60 V, 32 A, 35 m Ω

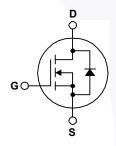
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 32 A, 60 V, $R_{DS(on)}$ = 35 m Ω (Max.) @ V_{GS} = 10 V, I_D = 16 A
- Low Gate Charge (Typ. 15 nC)
- Low Crss (Typ. 50 pF)
- · 100% Avalanche Tested
- · 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQP30N06L	Unit
V_{DSS}	Drain-Source Voltage		60	V
I _D	Drain Current - Continuous (T _C = 25°	C)	32	Α
	- Continuous (T _C = 100)°C)	22.6	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	128	Α
V _{GSS}	Gate-Source Voltage		± 20	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	350	mJ
I _{AR}	Avalanche Current	(Note 1)	32	Α
E _{AR}	Repetitive Avalanche Energy	(Note 1)	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T _C = 25°C)		79	W
	- Derate above 25°C		0.53	W/°C
T _J , T _{STG}	Operating and Storage Temperature Ran	ige	-55 to +175	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP30N06L	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.90	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP30N06L	FQP30N06L	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25$ °C unless otherwise noted.

Parameter	Test Conditions	Min	Тур	Max	Unit
aracteristics					
Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.06		V/°C
Zana Oata Valtana Basin Ourrant	V _{DS} = 60 V, V _{GS} = 0 V			1	μΑ
Zero Gate voltage Drain Current	V _{DS} = 48 V, T _C = 150°C			10	μΑ
Gate-Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	-		100	nA
Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
	Drain-Source Breakdown Voltage Breakdown Voltage Temperature Coefficient Zero Gate Voltage Drain Current Gate-Body Leakage Current, Forward	tracteristics Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25°C Zero Gate Voltage Drain Current $V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$ $V_{DS} = 48 \text{ V}$, $V_{CS} = 150 \text{ C}$ Gate-Body Leakage Current, Forward $V_{GS} = 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	tracteristics Drain-Source Breakdown Voltage $V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ μA}$ 60 Breakdown Voltage Temperature Coefficient $I_D = 250 \text{ μA}$, Referenced to 25°C 0.06 Zero Gate Voltage Drain Current $V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$ $V_{DS} = 48 \text{ V}$, $V_{CS} = 150 \text{ C}$ Gate-Body Leakage Current, Forward $V_{GS} = 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		2.5	V
R _{DS(on)}	Static Drain-Source	V _{GS} = 10 V, I _D = 16 A	-	0.027	0.035	0
	On-Resistance	$V_{GS} = 5 \text{ V}, I_{D} = 16 \text{ A}$		0.035	0.045	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 25 V, I _D = 16 A	-	24		S

Dynamic Characteristics

C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$	 800	1040	pF
Coss	Output Capacitance	f = 1.0 MHz	 270	350	pF
C _{rss}	Reverse Transfer Capacitance		 50	65	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 30 V, I _D = 16 A,		15	40	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		210	430	ns
t _{d(off)}	Turn-Off Delay Time	<u> </u>		60	130	ns
t _f	Turn-Off Fall Time	(Note 4)	/	110	230	ns
Q_g	Total Gate Charge	V _{DS} = 48 V, I _D = 32 A,		15	20	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 5 V	A	3.5		nC
Q_{gd}	Gate-Drain Charge	(Note 4)		8.5		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current				32	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				128	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 32 A			1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 32 A,		60		ns
Q _{rr}	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$		90		nC

- **Notes:** 1. Repetitive Rating : Pulse width limited by maximum junction temperature. 2. L = 400 μ H, I_{AS} = 32 A, V_{DD} = 25 V, R_G = 25 Ω , starting T_J = 25°C. 3. I_{SD} \leq 32 A, di/dt \leq 300 A/us, V_{DD} \leq BV_{DSS}, starting T_J = 25°C. 4.Essentially independent of operating temperature.

Typical Characteristics

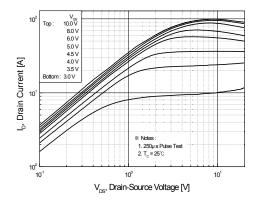


Figure 1. On-Region Characteristics

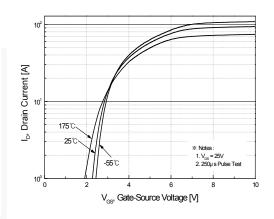


Figure 2. Transfer Characteristics

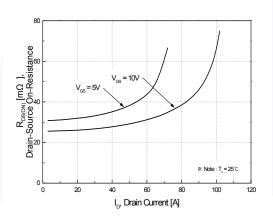


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

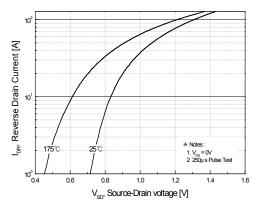


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

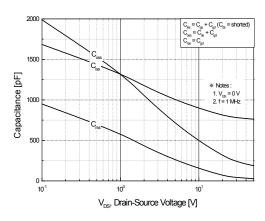


Figure 5. Capacitance Characteristics

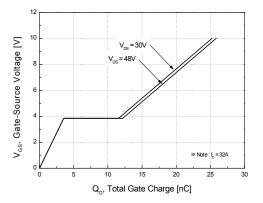


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

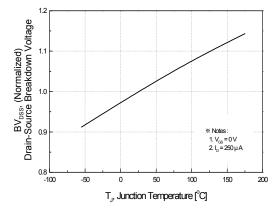


Figure 7. Breakdown Voltage Variation vs. Temperature

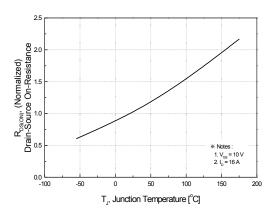


Figure 8. On-Resistance Variation vs. Temperature

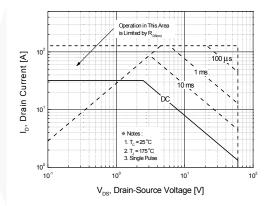


Figure 9. Maximum Safe Operating Area

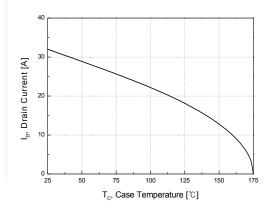


Figure 10. Maximum Drain Current vs. Case Temperature

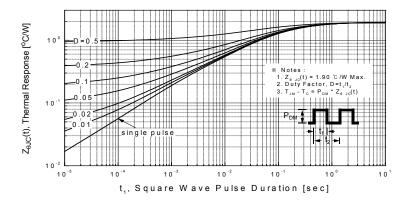


Figure 11. Transient Thermal Response Curve

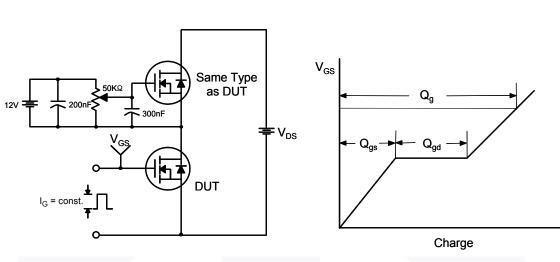


Figure 12. Gate Charge Test Circuit & Waveform

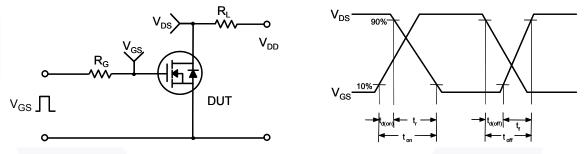


Figure 13. Resistive Switching Test Circuit & Waveforms

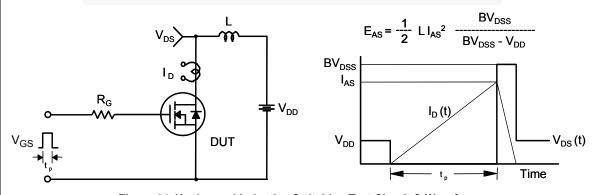
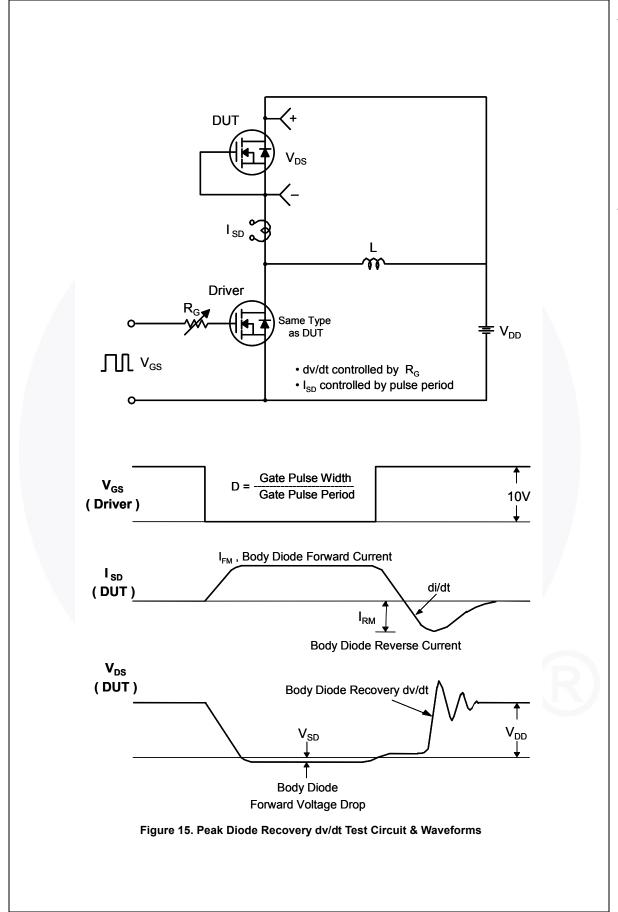


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

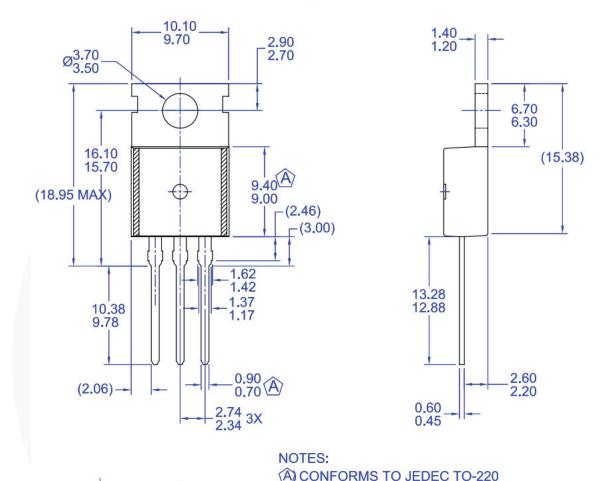


Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

VARIATION AB EXCEPT WHERE NOTED

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

B) ALL DIMENSIONS ARE IN MILLIMETERS.

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