

Switcher

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1 Introduction

Design and build a switch mode power supply (SMPS) which will operate in boost and buck mode. The controller will contain a selection of menu options allowing the user to control as many features as possible of the SMPS operation. The software running on the controlling processor must consist of no more than 1024 bytes.

1.1 Processor selection

The chosen processor is a **Silicon Labs C8051F850-C-GU** which uses the 8051 architecture. An 8051 processor is a good choice for a code size reduction exercise as there are many thoroughly tested compilers available. The Keil c51 compiler will be used to generate assembly for this project.

2 Hardware

2.1 Schematic

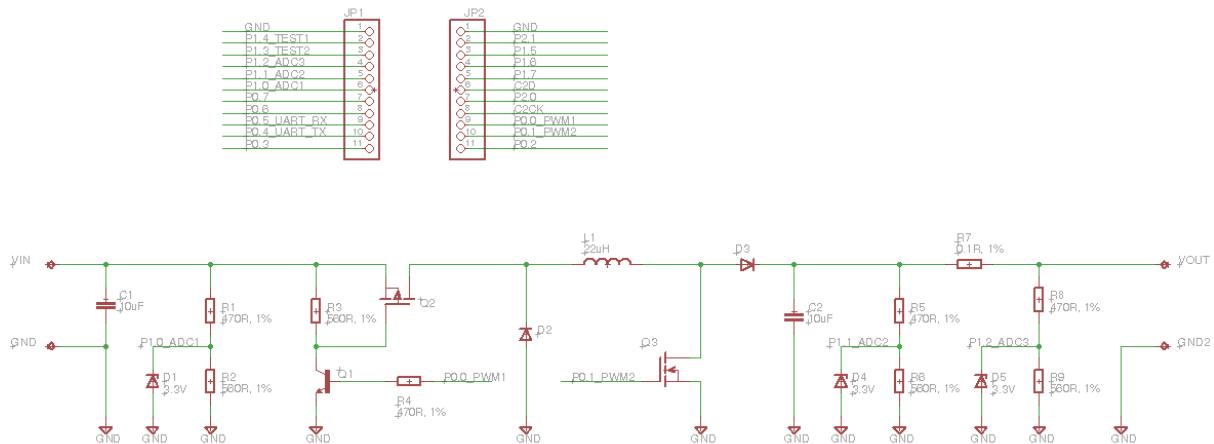


Figure 1: Schematic.

2.2 Bill of Materials (BoM)

Designator	Value	Manufacturer	Manufacturer Number	Part
C1,C2	10uF	MULTICOMP	MCGPR25V106M5X11	
D1,D4,D5	3.3V	ON SEMICONDUCTOR	1N5333BG	
D2,D3		TAIWAN SEMICONDUCTOR	SR1504	
JP1,JP2		AMPHENOL FCI	77311-401-36LF	
L1	22uH	PANASONIC	ELC08D220E	
Q1		MULTICOMP	BC337	
Q2		FAIRCHILD SEMICONDUCTOR	FQP27P06	
Q3		FAIRCHILD SEMICONDUCTOR	FQP30N06L	
R1,R4,R5,R8	470Ω	MULTICOMP	MF12 470R	
R2,R3,R6,R9	560Ω	MULTICOMP	MF12 560R	
R7	0.1Ω	VISHAY	LVR01R1000FE12	
Strip board		KEMO	ELECTRONIC E012	
Dev board		SILICON LABS	LTOOLSTICK850DC-UG	

Table 1: BoM

2.3 Stripboard

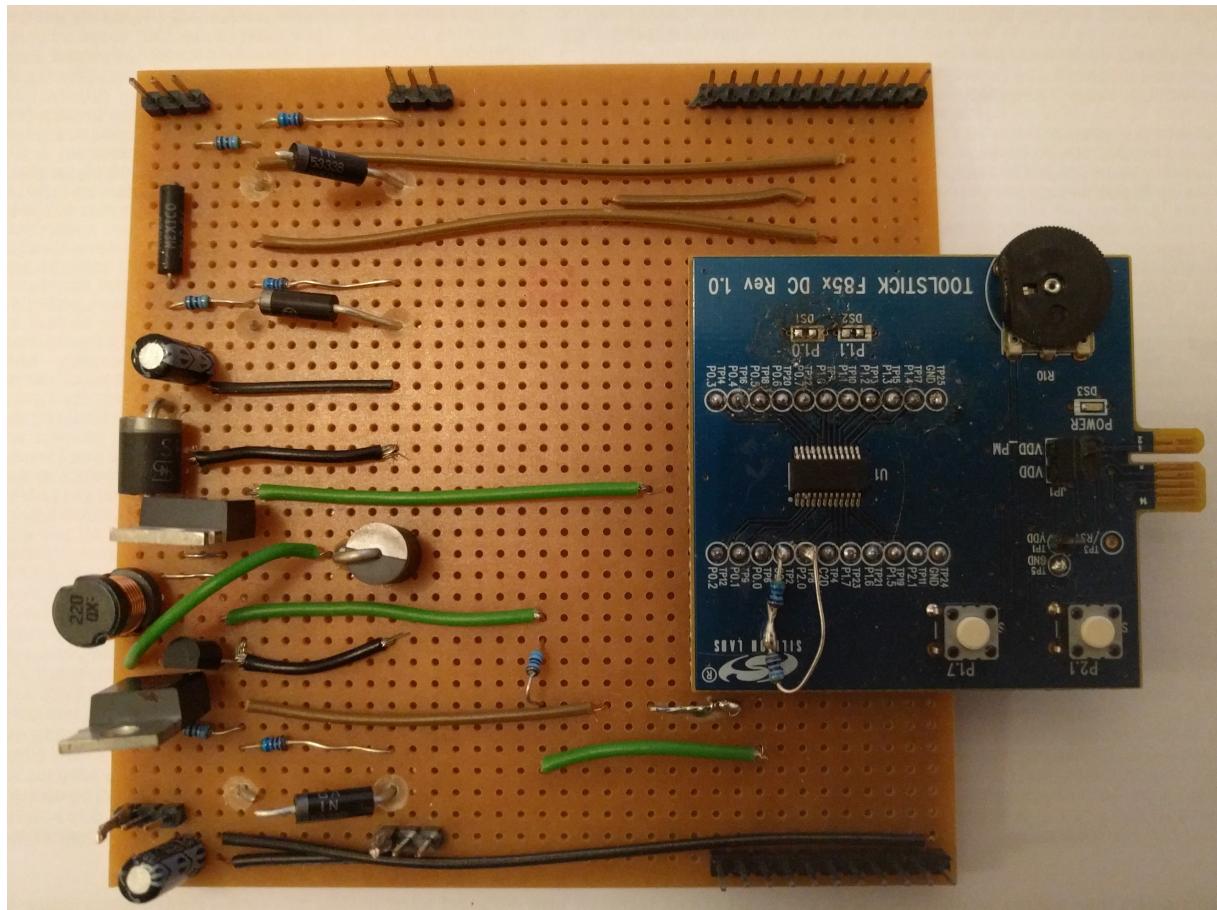


Figure 2: Stripboard top side.

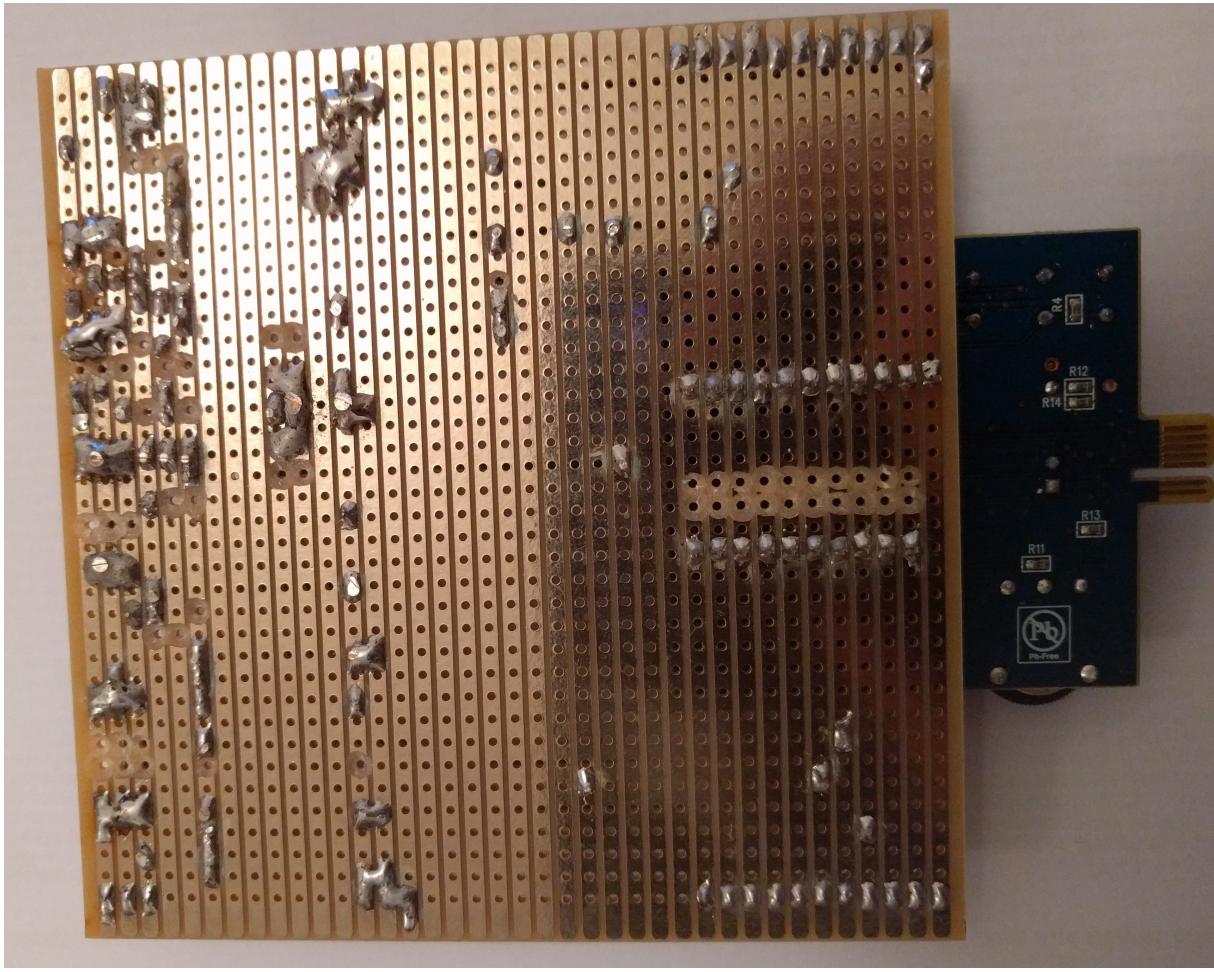


Figure 3: Stripboard bottom side.

3 Software

3.1 Peripherals

3.1.1 Analogue to Digital Convertors (ADCs)

A single ADC is multiplexed to measure three voltages on the board.

3.1.2 Universal Asynchronous/Synchronous Transceiver (UART)

The UART is configured to run at 115200 baud with no control flow with a ring buffer interface. Transmission from the microcontroller happens through `uartLoadOut` which adds to the **8 byte** buffer and is then unloaded from a timer. The input is not interrupt driven and is handled in the main control loop using a **5 byte** buffer that is enough to contain the longest command.

3.1.3 Programmable Counter Array (PCA)

The Pulse Width Modulation (PWM) is controlled from the counter array. The output runs at approximately 96KHz with 8 bits to control the duty cycle. A high resolution for control would be favourable for this application but the frequency achieved in 16-bit mode is far too low for this application.

3.1.4 Timers

Timer 0 is used as baud rate generation for the UART. **Timer 2** is used to trigger an Interrupt Service Routine (ISR) which runs at 4KHz. The ISR controls the UART transmission, sampling of the ADC, running the controller and finally setting the PWM.

3.2 Operation

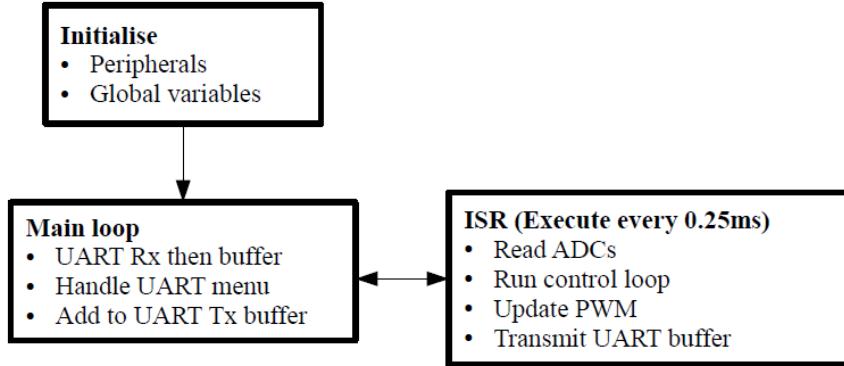


Figure 4: Software overview.

3.3 UART Menu

Command	Char	Send numbers	Return numbers	Notes
Enable	g	0	0	0
Disable	s	0	0	0
Read ADC1	x	0	4	Result in mV
Read ADC2	y	0	4	Result in mV
Read ADC3	z	0	4	Result in mV
Read output current	j	0	4	Result in mA
Set output voltage	v	4	0	Send value in mV
Set output current	c	4	0	Send value in mA
Set controller P	p	4	0	Value is divide by 10
Set controller I	i	4	0	Value is divide by 10
Set input voltage upper limit	u	4	0	Send value in mV
Set input voltage lower limit	l	4	0	Send value in mV

Table 2: UART menu

3.4 Assembly analysis

The following sections of code are library functions inserted by the compiler to facilitate some more complex operations.

3.4.1 ADC scaling

Listing 1 is a line of code operating on a 32 bit signed integer and invokes listing 5 and 6. The purpose of this operation is to cast the voltage recorded by the ADC to a representation in mV. It is possible for the target voltage to be translated instead but this would still require the same piece of code. The 12 bit output but the ADC must be multiplied 5.926 as to represent the voltage at the top of the potential divider. Fixed bit multiplication followed by a shift operation removes the need for a floating point operation but yeilds the same result.

Listing 1: LIMUL

```
return (((U32)ADCO)*SCALE_MUL) >> 10;
```

3.4.2 ADC scaling

3.4.3 Division

Division and modulus operations are contained in 2 invoke the functions contained in 8.

Listing 2: Division

```
scale /= 10;  
num = out / scale;  
out %= scale;
```

3.4.4 Switch

This library function is generated to control large switch statements??

4 Testing

The potential dividers constantly place the power supply under a load of 515Ω . To test both the UART interface and the switch mode functionality a small python script is used to create GUI to plot values in real time. The input and output voltages recorded by the microcontroller are contained in Figure 5 and the actual values are contained in 6.

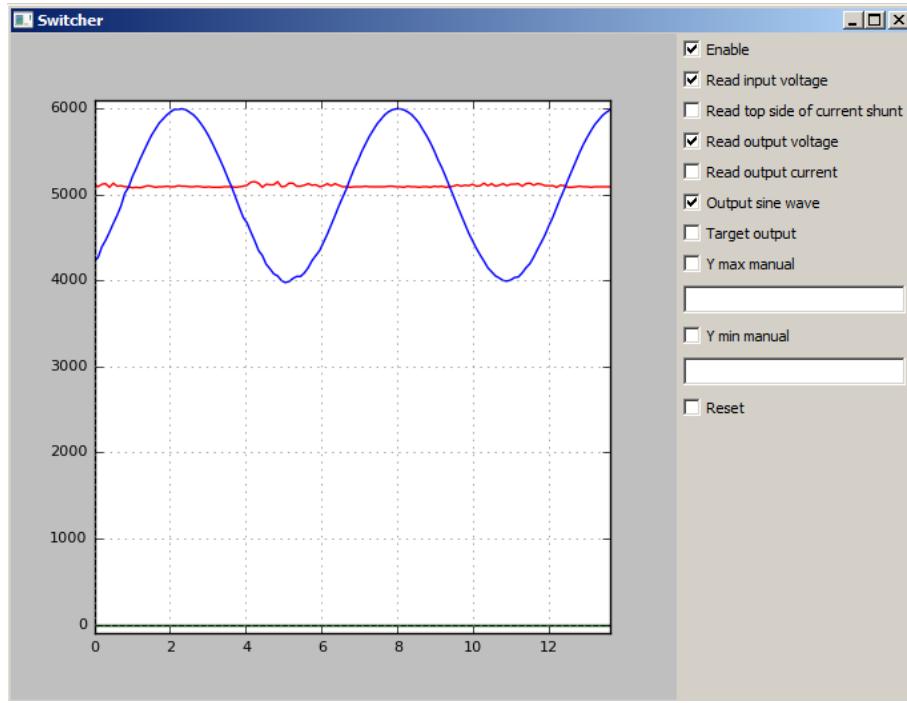


Figure 5: Sine wave output on GUI.

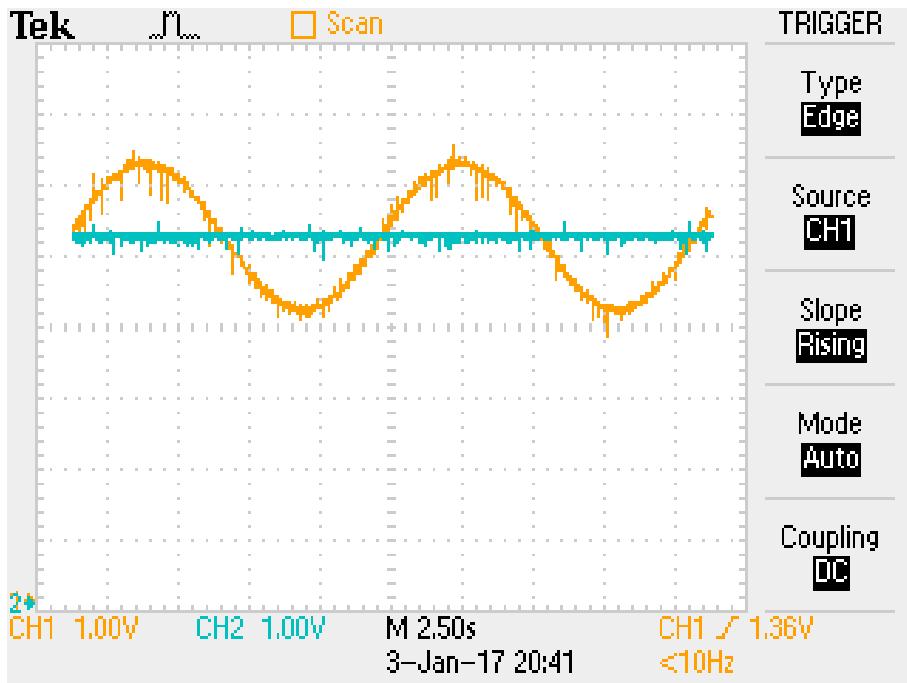


Figure 6: Sine wave output on scope.

5 Conclusion

The complete assembly in listing 4 is generated from the code in listing 3. The C code is contained within a single file and generates 950 lines of assembler with an additional 3 lines contained within the jump table and the jump on reset...

- **0x0000** Jumps straight to 0x0800
- **0x001B** Jump table entry TIMER1_ISR(C:0BB6)
- **0x002B** Jump table entry TIMER2_ISR(C:094C)
- **0x0800** First line of code generated from main.c
- **0x0BB6** Final line of code generated from main.c

The Keil c51 compilier limits machine code generation to 2KB (not a problem) however it also limits the use of memory less than 2KB by always jumping to address 2048 and then continuing with the compiled assembler. Excluding the first 2048 is not completely fair because the jump on reset and the jump table would still exsist. The highest vector used in the jump table is at address 43 so assuming this is not optimised by the compilier the total code size comes to **993 bytes**.

5.1 Further work

- Improve output current
- Replaced protection diodes with sutiable parts
- Improve resolution of ADC to enable constant control

6 Appendix

6.1 Code listings

Listing 3: main.c

```

//-----
// Project: Swticher
// File:    main.c
// Brief:   Single main file containing all code
//-----


//-----
// Includes
//-----


#include "SI_C8051F850_Register.Enums.h"
#include "SI_C8051F850_Defs.h"

//-----
// Defines
//-----


#define SYSCLK          24500000           // SYSCLK frequency in Hz
#define BAUDRATE        115200             // Baud rate of UART in bps

#define P               5
#define I               2

#define UART_SIZE_IN   5
#define UART_SIZE_OUT  8

#define ADC1            0x08
#define ADC2            0x09
#define ADC3            0x0A

#define SCALE_MUL       6068              // When combined with >> 10 will scale by 5.926 to compensate for potential divide

#define DEFAULT_OUT_MV  5000
#define DEFAULT_HIGH_MV 6000
#define DEFAULT_LOW_MV  4000

SBIT(TEST2, SFR_P1, 3);                  // DS5 P1.0 LED
SBIT(TEST1, SFR_P1, 4);                  // DS5 P1.0 LED
//-----
```

```

// Prototypes
//-----
U16 readAdc(U8 sel);
void uartLoadOut(U8 tx);
U16 uartNumbers(U16 toSend,bool transmit);

//-----
// Global Variables
//-----

volatile U8      uart_in[UART_SIZE_IN];
volatile U8      uart_out[UART_SIZE_OUT];
volatile U8      head;
volatile U8      tail;
volatile int     integral;
volatile U8      duty;
volatile U16    high_mV;
volatile U16    low_mV;
volatile U16    target_mV;
volatile bool   enabled;
volatile U16    adc1;
volatile U16    adc2;
volatile U16    adc3;
volatile U16    current;

//-----
// Main Routine
//-----

void main (void){
    // Start of peripheral setup
    U8 TCON_save;
    // Watchdog
    WDTCN = 0xDE;                                // First key
    WDTCN = 0xAD;                                // Second key - Watchdog now disabled
    // Clock
    CLKSEL =
        CLKSEL_CLKSL__HFOSC           | // Use 24.5MHz interal clock
        CLKSEL_CLKDIV__SYSCLK_DIV_1;  | // Do not divide
    // Port 0
    P0MDOUT =
        P0MDOUT_B0__PUSH_PULL         | // PWM1 output
        P0MDOUT_B1__PUSH_PULL         | // PWM2 output
        P0MDOUT_B2__OPEN_DRAIN        |
        P0MDOUT_B3__OPEN_DRAIN        |
        P0MDOUT_B4__PUSH_PULL         | // UART TX
        P0MDOUT_B5__OPEN_DRAIN        | // UART RX
        P0MDOUT_B6__OPEN_DRAIN        |
        P0MDOUT_B7__OPEN_DRAIN        |
    // Port 1
    P1MDOUT =
        P1MDOUT_B0__OPEN_DRAIN        |
        P1MDOUT_B1__OPEN_DRAIN        |
        P1MDOUT_B2__OPEN_DRAIN        |
        P1MDOUT_B3__PUSH_PULL         | // TEST2
        P1MDOUT_B4__PUSH_PULL         | // TEST1
        P1MDOUT_B5__OPEN_DRAIN        |
        P1MDOUT_B6__OPEN_DRAIN        |
        P1MDOUT_B7__OPEN_DRAIN        |
    P1MDIN =
        P1MDIN_B0__ANALOG            | // ADC1
        P1MDIN_B1__ANALOG            | // ADC2
        P1MDIN_B2__ANALOG            | // ADC3
        P1MDIN_B3__DIGITAL           |
        P1MDIN_B4__DIGITAL           |
        P1MDIN_B5__DIGITAL           |
        P1MDIN_B6__DIGITAL           |
        P1MDIN_B7__DIGITAL           |
    // Port crossbar
    XBR0 =
        XBRO_URTOE__ENABLED          | // Route out UART
        XBRO_SPIOE__DISABLED         |
        XBRO_SMBOE__DISABLED         |
        XBRO_CPOE__DISABLED          |
        XBRO_CPOAE__DISABLED         |
        XBRO_CP1E__DISABLED          |
        XBRO_CP1AE__DISABLED         |
        XBRO_SYSCKE__DISABLED         |
    XBR1 =
        XBR1_PCAOME__CEX0_CEX1       | // Route out PCA0 and PCA1
        XBR1_ECIE__DISABLED          |
        XBR1_TOE__DISABLED           |
        XBR1_TIE__DISABLED           |
        XBR1_T2E__DISABLED           |
    XBR2 =
        XBR2_WEAKPUD__PULL_UPS_ENABLED | // Weak pull ups
        XBR2_XBARE__ENABLED          | // Enable cross bar
    // ADC
    //ADCOMX =
    // ADCOMX_ADCOMX__ADCOP10;
    ADCOCF =
        (1 << ADCOCF_ADSC__SHIFT)    | // ADC set to 10 bit
        ADCOCF_AD3BE__NORMAL         |
        ADCOCF_ADGND__GAIN_1          | // ADC gain set to 1
        ADCOCF_ATDM__TRACK_NORMAL;   | // Immediate convert
    ADCOCNO &=
        ~ADCOCNO_ADCM__FMASK;
    ADCOCNO |=

```

```

        ADCOCNO_ADEN__ENABLED
        ADCOCNO_ADCM__ADBUSD;
// Timer 0
    TCON_save = TCON;
    TCON &=
        TCON_TRO__BMASK
        TCON_TR1__BMASK;
    TH1 = (150 << TH1_TH1__SHIFT);
    TL1 = (150 << TL1_TL1__SHIFT);
    TCON =
        TCON_save;
// Timer setup
    CKCON =
        CKCON_SCA__SYSCLK_DIV_12
        CKCON_TOM__PRESCALE
        CKCON_T3MH__EXTERNAL_CLOCK
        CKCON_T3ML__EXTERNAL_CLOCK
        CKCON_T1M__SYSCLK;
    TMOD =
        TMOD_TOM__MODE0
        TMOD_CTO__TIMER
        TMOD_GATE0__DISABLED
        TMOD_TIM__MODE2
        TMOD_CT1__TIMER
        TMOD_GATE1__DISABLED;
    TCON |=
        TCON_TR1__RUN ;
// UART
    SCON0 |=
        SCON0_REN__RECEIVE_ENABLED;
// VREF
    REFOCN =
        REFOCN_REFSL__VDD_PIN
        REFOCN_IREFLVL__1P65
        REFOCN_GNDSL__GND_PIN
        REFOCN_TEMPE__TEMP_DISABLED;
// RSTSRC
    RSTSRC =
        RSTSRC_CORSEF__NOT_SET
        RSTSRC_MCDRSF__SET
        RSTSRC_PORSF__SET
        RSTSRC_SWRSF__NOT_SET;
// Interrupt
    IE =
        IE_EA__ENABLED
        IE_EX0__DISABLED
        IE_EX1__DISABLED
        IE_ESPIO__DISABLED
        IEETO__DISABLED
        IE_ET1__ENABLED
        IE_ET2__ENABLED
        IE_ESO__ENABLED;
    IP =
        IP_PX0__LOW
        IP_PX1__LOW
        IP_PSP10__LOW
        IP_PTO__LOW
        IP_PT1__LOW
        IP_PT2__HIGH
        IP_PSO__LOW;
// PCA
    PCAOCN_CR =
        PCAOCN_CR__STOP;
    PCAOCPM0 =
        PCAOCPM0_CAPN__DISABLED
        PCAOCPM0_ECCF__ENABLED
        PCAOCPM0_MAT__ENABLED
        PCAOCPM0_CAPP__DISABLED
        PCAOCPM0_ECOM__ENABLED
        PCAOCPM0_PWM__ENABLED
        PCAOCPM0_TOG__DISABLED;
    PCAOCPM1 =
        PCAOCPM1_CAPN__DISABLED
        PCAOCPM1_ECCF__ENABLED
        PCAOCPM1_MAT__ENABLED
        PCAOCPM1_CAPP__DISABLED
        PCAOCPM1_ECOM__ENABLED
        PCAOCPM1_PWM__ENABLED
        PCAOCPM1_TOG__DISABLED;
    PCAOMD =
        PCAOMD_CIDL__NORMAL
        PCAOMD_ECF__OVF_INT_DISABLED
        PCAOMD_CPS__SYSCLK;
    PCAOCN |=
        PCAOCN_CR__RUN;
// Timer 2
    TMR2CN |= TMR2CN_TR2__RUN;
// End of peripheral setup

enabled      = false;
integral     = 0;
target_mv    = DEFAULT_OUT_MV;
high_mv      = DEFAULT_HIGH_MV;
low_mv       = DEFAULT_LOW_MV;

SCONO_TI     = 1;
SCONO_RI     = 0;

while (1){

```

```

        if(SCONO_RI){
            SCONO_RI = 0;
            uart_in[4] = uart_in[3];
            uart_in[3] = uart_in[2];
            uart_in[2] = uart_in[1];
            uart_in[1] = uart_in[0];
            uart_in[0] = SBUFO;

            uartLoadOut(uart_in[0]);

            switch(uart_in[0]){
                case 'a':    uartNumbers(target_mV,true);
                break;
                case 'c':    uartNumbers(current,true);
                break;
                case 'd':    uartNumbers(duty,true);
                break;
                case 'g':    enabled      = true;
                integral     = 0;
                break;
                case 's':    enabled      = false;
                break;
                case 'm':    uartNumbers(high_mV,true);
                break;
                case 'n':    uartNumbers(low_mV,true);
                break;
                case 'x':    uartNumbersadc1,true);
                break;
                case 'y':    uartNumbersadc2,true);
                break;
                case 'z':    uartNumbersadc3,true);
                break;
                default:   switch(uart_in[4]){
                    case 'h':    high_mV      = uartNumbers(high_mV,false);
                    break;
                    case 'l':    low_mV       = uartNumbers(low_mV,false);
                    break;
                    case 'v':    target_mV    = uartNumbers(target_mV,false);
                    integral     = 0;
                    break;
                }
                break;
            }
        }
    }

    //-----
    // Routines
    //-----
}

void uartLoadOut(U8 tx){                                // Handle buffering out Tx UART
    uart_out[head] = tx;                               // Buffer outgoing
    head++;
    head %= UART_SIZE_OUT;                           // Wrap around
}

U16 uartNumbers(U16 toSend, bool transmit){           // Tx/Rx up to 4 length numbers over UART
    U16 out = toSend;
    U16 num = 0;
    U16 scale = 10000;
    U8 test;
    U8 i = 4;
    bool bad = false;
    while(i){
        scale /= 10;                                // On zero done
        i--;                                         // Shift
        test = uart_in[i] - 48;                      // Move through UART array
        if(test > 10){                             // ascii to num
            bad = true;                            // check is 0 to 9, unsigned
        }
        num += test*scale;                          // shift in to position
        if(transmit){
            num = out / scale;                     // Put if statement at back of loop to save on jumps
            uartLoadOut(num + 48);                  // 10 powers
            out %= scale;                         // Number to ascii
        }
    }
    uartLoadOut('\n');
    uartLoadOut('\r');
    if(bad){
        num = DEFAULT_OUT_MV;                   // Not all valid numbers so set output as default
    }
    return num;
}

U16 readAdc(U8 sel){                                 // Read the available ADCs
    U8 i;
    ADCOMX = sel;
    for(i=0;i<2;i++){
        ADCOCNO |= ADCOCNO_ADBUSY_SET;
        while(ADCOCNO & ADCOCNO_ADBUSY_SET);      // Wait for sample to complete
    }
    return (((U32)ADCO)*SCALE_MUL) >> 10;          // Scale to mV
}

//-----
// Interrupt Routines
//-----

```

```

INTERRUPT (TIMER1_ISR, TIMER1_IRQn){}                                // Needed for UART timing
INTERRUPT (TIMER2_ISR, TIMER2_IRQn){}                                // One timer handling UART Tx and PID
    int out;
    int error;
    TEST1 = 1;

    adc1 = readAdc(ADC1);
    adc2 = readAdc(ADC2);
    adc3 = readAdc(ADC3);
    current = (adc2 - adc3)*10;

    if((adc1 < low_mV) || (adc1 > high_mV)){           // Watch input voltage
        enabled = false;
    }

    error = (int)target_mV - (int)adc3;                      // PID controller
    integral += error;
    out = ((error*p) + (integral*I)) >> 10;             // Divide by 1024
    if((out < 0) || (!enabled)){
        out = 0;
    }
    duty = out;
    PCAOPH0 = PCAOPH1 = 0xFF - out;

    if(head != tail){
        SBUFO = uart_out[tail];                           // Timer tuned so no need to check
        tail++;                                         // Transmit UART
        tail %= UART_SIZE_OUT;                         // Wrap around
    }

    TMR2H = 255;                                         // Runs at 4KHz
    TMR2CN_TF2H = 0;                                     // Enable interrupt again
    TEST1 = 0;                                           // Timing debug
}

//-----
// END
//-----

```

Listing 4: Swicther.asm

C:0x0000	020BAA	LJMP	C:0BAA
C:0x0003	00	NOP	
C:0x0004	00	NOP	
C:0x0005	00	NOP	
C:0x0006	00	NOP	
C:0x0007	00	NOP	
C:0x0008	00	NOP	
C:0x0009	00	NOP	
C:0x000A	00	NOP	
C:0x000B	00	NOP	
C:0x000C	00	NOP	
C:0x000D	00	NOP	
C:0x000E	00	NOP	
C:0x000F	00	NOP	
C:0x0010	00	NOP	
C:0x0011	00	NOP	
C:0x0012	00	NOP	
C:0x0013	00	NOP	
C:0x0014	00	NOP	
C:0x0015	00	NOP	
C:0x0016	00	NOP	
C:0x0017	00	NOP	
C:0x0018	00	NOP	
C:0x0019	00	NOP	
C:0x001A	00	NOP	
C:0x001B	020BB6	LJMP	TIMER1_ISR(C:0BB6)
C:0x001E	00	NOP	
C:0x001F	00	NOP	
C:0x0020	00	NOP	
C:0x0021	00	NOP	
C:0x0022	00	NOP	
C:0x0023	00	NOP	
C:0x0024	00	NOP	
C:0x0025	00	NOP	
C:0x0026	00	NOP	
C:0x0027	00	NOP	
C:0x0028	00	NOP	
C:0x0029	00	NOP	
C:0x002A	00	NOP	
C:0x002B	02094C	LJMP	TIMER2_ISR(C:094C)
C:0x002E	00	NOP	
C:0x002F	00	NOP	
C:0x0030	00	NOP	
C:0x0031	00	NOP	
C:0x0032	00	NOP	
C:0x0033	00	NOP	
C:0x0034	00	NOP	
C:0x0035	00	NOP	
C:0x0036	00	NOP	

C :0x0037	00	NOP
C :0x0038	00	NOP
C :0x0039	00	NOP
C :0x003A	00	NOP
C :0x003B	00	NOP
C :0x003C	00	NOP
C :0x003D	00	NOP
C :0x003E	00	NOP
C :0x003F	00	NOP
C :0x0040	00	NOP
C :0x0041	00	NOP
C :0x0042	00	NOP
C :0x0043	00	NOP
C :0x0044	00	NOP
C :0x0045	00	NOP
C :0x0046	00	NOP
C :0x0047	00	NOP
C :0x0048	00	NOP
C :0x0049	00	NOP
C :0x004A	00	NOP
C :0x004B	00	NOP
C :0x004C	00	NOP
C :0x004D	00	NOP
C :0x004E	00	NOP
C :0x004F	00	NOP
C :0x0050	00	NOP
C :0x0051	00	NOP
C :0x0052	00	NOP
C :0x0053	00	NOP
C :0x0054	00	NOP
C :0x0055	00	NOP
C :0x0056	00	NOP
C :0x0057	00	NOP
C :0x0058	00	NOP
C :0x0059	00	NOP
C :0x005A	00	NOP
C :0x005B	00	NOP
C :0x005C	00	NOP
C :0x005D	00	NOP
C :0x005E	00	NOP
C :0x005F	00	NOP
C :0x0060	00	NOP
C :0x0061	00	NOP
C :0x0062	00	NOP
C :0x0063	00	NOP
C :0x0064	00	NOP
C :0x0065	00	NOP
C :0x0066	00	NOP
C :0x0067	00	NOP
C :0x0068	00	NOP
C :0x0069	00	NOP
C :0x006A	00	NOP
C :0x006B	00	NOP
C :0x006C	00	NOP
C :0x006D	00	NOP
C :0x006E	00	NOP
C :0x006F	00	NOP
C :0x0070	00	NOP
C :0x0071	00	NOP
C :0x0072	00	NOP
C :0x0073	00	NOP
C :0x0074	00	NOP
C :0x0075	00	NOP
C :0x0076	00	NOP
C :0x0077	00	NOP
C :0x0078	00	NOP
C :0x0079	00	NOP
C :0x007A	00	NOP
C :0x007B	00	NOP
C :0x007C	00	NOP
C :0x007D	00	NOP
C :0x007E	00	NOP
C :0x007F	00	NOP
C :0x0080	00	NOP
C :0x0081	00	NOP
C :0x0082	00	NOP
C :0x0083	00	NOP
C :0x0084	00	NOP
C :0x0085	00	NOP
C :0x0086	00	NOP
C :0x0087	00	NOP
C :0x0088	00	NOP
C :0x0089	00	NOP
C :0x008A	00	NOP
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C :0x0093	00	NOP
C :0x0094	00	NOP
C :0x0095	00	NOP
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C :0x0097	00	NOP
C :0x0098	00	NOP
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C :0x00A8	00	NOP
C :0x00A9	00	NOP
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C :0x00AB	00	NOP
C :0x00AC	00	NOP
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C :0x00AE	00	NOP
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C:0x01C2	00	NOP

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C :0x020E	00	NOP
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C :0x028E	00	NOP
C :0x028F	00	NOP
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C :0x02E2	00	NOP
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C :0x02EF	00	NOP
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C :0x02FB	00	NOP
C :0x02FC	00	NOP
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C :0x07C2	00	NOP
C :0x07C3	00	NOP
C :0x07C4	00	NOP
C :0x07C5	00	NOP
C :0x07C6	00	NOP
C :0x07C7	00	NOP
C :0x07C8	00	NOP
C :0x07C9	00	NOP
C :0x07CA	00	NOP
C :0x07CB	00	NOP
C :0x07CC	00	NOP
C :0x07CD	00	NOP
C :0x07CE	00	NOP
C :0x07CF	00	NOP
C :0x07D0	00	NOP
C :0x07D1	00	NOP
C :0x07D2	00	NOP
C :0x07D3	00	NOP
C :0x07D4	00	NOP
C :0x07D5	00	NOP
C :0x07D6	00	NOP
C :0x07D7	00	NOP
C :0x07D8	00	NOP
C :0x07D9	00	NOP
C :0x07DA	00	NOP
C :0x07DB	00	NOP
C :0x07DC	00	NOP
C :0x07DD	00	NOP
C :0x07DE	00	NOP
C :0x07DF	00	NOP
C :0x07EO	00	NOP
C :0x07E1	00	NOP
C :0x07E2	00	NOP
C :0x07E3	00	NOP
C :0x07E4	00	NOP
C :0x07E5	00	NOP
C :0x07E6	00	NOP
C :0x07E7	00	NOP
C :0x07E8	00	NOP
C :0x07E9	00	NOP
C :0x07EA	00	NOP
C :0x07EB	00	NOP
C :0x07EC	00	NOP
C :0x07ED	00	NOP
C :0x07EE	00	NOP
C :0x07EF	00	NOP
C :0x07F0	00	NOP
C :0x07F1	00	NOP
C :0x07F2	00	NOP

```

C:0x07F3    00      NOP
C:0x07F4    00      NOP
C:0x07F5    00      NOP
C:0x07F6    00      NOP
C:0x07F7    00      NOP
C:0x07F8    00      NOP
C:0x07F9    00      NOP
C:0x07FA    00      NOP
C:0x07FB    00      NOP
C:0x07FC    00      NOP
C:0x07FD    00      NOP
C:0x07FE    00      NOP
C:0x07FF    00      NOP
    71: void main (void){
    72:         // Start of peripheral setup
    73:         U8 TCON_save;
    74:         // Watchdog
    75:             WDTCN = 0xDE;                                // First key
C:0x0800    7597DE  MOV     WDTCN(0x97),#0xDE
    76:             WDTCN = 0xAD;                                // Second key - Watchdog now disabled
    77:         // Clock
C:0x0803    7597AD  MOV     WDTCN(0x97),#0xAD
    78:         CLKSEL =
    79:             CLKSEL_CLKSL__HFOSC                         | // Use 24.5MHz interal clock
    80:             CLKSEL_CLKDIV__SYSCLK_DIV_1;                | // Do not divide
    81:         // Port 0
C:0x0806    E4       CLR     A
C:0x0807    F5A9    MOV     CLKSEL(0xA9),A
    82:         POMDOUT =
    83:             POMDOUT_BO__PUSH_PULL                         | // PWM1 output
    84:             POMDOUT_B1__PUSH_PULL                         | // PWM2 output
    85:             POMDOUT_B2__OPEN_DRAIN
    86:             POMDOUT_B3__OPEN_DRAIN
    87:             POMDOUT_B4__PUSH_PULL                         | // UART TX
    88:             POMDOUT_B5__OPEN_DRAIN                         | // UART RX
    89:             POMDOUT_B6__OPEN_DRAIN
    90:             POMDOUT_B7__OPEN_DRAIN
    91:         // Port 1
C:0x0809    75A413  MOV     POMDOUT(0xA4),#0x13
    92:         P1MDOUT =
    93:             P1MDOUT_BO__OPEN_DRAIN
    94:             P1MDOUT_B1__OPEN_DRAIN
    95:             P1MDOUT_B2__OPEN_DRAIN
    96:             P1MDOUT_B3__PUSH_PULL                         | // TEST2
    97:             P1MDOUT_B4__PUSH_PULL                         | // TEST1
    98:             P1MDOUT_B5__OPEN_DRAIN
    99:             P1MDOUT_B6__OPEN_DRAIN
    100:            P1MDOUT_B7__OPEN_DRAIN
C:0x080C    75A518  MOV     P1MDOUT(0xA5),#0x18
    101:        P1MDIN =
    102:            P1MDIN_BO__ANALOG
    | // ADC1
    103:            P1MDIN_B1__ANALOG
    | // ADC2
    104:            P1MDIN_B2__ANALOG
    | // ADC3
    105:            P1MDIN_B3__DIGITAL
    | 
    106:            P1MDIN_B4__DIGITAL
    | 
    107:            P1MDIN_B5__DIGITAL
    | 
    108:            P1MDIN_B6__DIGITAL
    | 
    109:            P1MDIN_B7__DIGITAL;
    110:        // Port crossbar
C:0x080F    75F2F8  MOV     P1MDIN(0xF2),#0xF8
    111:        XBRO =
    112:            XBRO_UROUTOE__ENABLED                         | // Route out UART
    113:            XBRO_SPIOE__DISABLED
    114:            XBRO_SMBOE__DISABLED
    115:            XBRO_CPOE__DISABLED
    116:            XBRO_CPOAE__DISABLED
    117:            XBRO_CPIE__DISABLED
    | 
    118:            XBRO_CPIAE__DISABLED
    119:            XBRO_SYSCKE__DISABLED;
C:0x0812    75E101  MOV     XBRO(0xE1),#0x01
    120:        XBR1 =
    121:            XBR1_PCAOME__CEXO_CEX1                         | // Route out PCA0 and PCA1
    122:            XBR1_ECIE__DISABLED
    123:            XBR1_TOE__DISABLED
    | 
    124:            XBR1_T1E__DISABLED
    | 
    125:            XBR1_T2E__DISABLED;
C:0x0815    75E202  MOV     XBR1(0xE2),#0x02
    126:        XBR2 =
    127:            XBR2_WEAKPUD__PULL_UPS_ENABLED               | // Weak pull ups
    128:            XBR2_XBARE__ENABLED                         // Enable cross bar
    129:        // ADC
    130:        //ADCOMX =
// Mux set in application
    131:        //      ADCOMX_ADCOMX__ADCOP10;
C:0x0818    75E340  MOV     XBR2(0xE3),#0x40
    132:        ADCOCF =
    133:            (1 << ADCOCF_ADSC__SHIFT)
    | 
    134:        ADCOCF_AD8BE__NORMAL                          | // ADC set to 10 bit

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135:                                ADCOCF_ADGND_GAIN_1
136:                                ADCOCF_ADTM_TRACK_NORMAL; | // ADC gain set to 1
// Immediate covert
C:0x081B    75BC09  MOV     ADCOCF(0xBC),#0x09
137:                                ADCOCNO &=
138:                                ~ADCOCN0_ADM_FMASK;
C:0x081E    53E8F8  ANL     ADCOCN0(0xE8),#0xF8
139:                                ADCOCN0 |=
140:                                ADCOCN0_ADEN_ENABLED
141:                                ADCOCN0_ADM_ADBUSY;
142:                                // Timer 0
C:0x0821    43E880  ORL     ADCOCN0(0xE8),#0x80
143:                                TCON_save = TCON;
C:0x0824    AF88    MOV     R7,TCON(0x88)
144:                                TCON &=
145:                                TCON_TRO_BMASK
&
146:                                TCON_TR1_BMASK;
C:0x0826    F588    MOV     TCON(0x88),A
147:                                TH1 = (150 << TH1_TH1_SHIFT);
C:0x0828    758D96  MOV     TH1(0x8D),#0x96
148:                                TL1 = (150 << TL1_TL1_SHIFT);
C:0x082B    758B96  MOV     TL1(0x8B),#0x96
149:                                TCON =
150:                                TCON_save;
151:                                // Timer setup
C:0x082E    8F88    MOV     TCON(0x88),R7
152:                                CKCON =
153:                                CKCON_SCA_SYSCLK_DIV_12
|
154:                                CKCON_TOM_PRESCALE
155:                                CKCON_T3MH_EXTERNAL_CLOCK
156:                                CKCON_T3ML_EXTERNAL_CLOCK
|
157:                                CKCON_T1M_SYSCLK;
C:0x0830    758E08  MOV     CKCON(0x8E),#0x08
158:                                TMOD =
159:                                TMOD_TOM_MODE0
|
160:                                TMOD_CTO_TIMER
|
161:                                TMOD_GATE0_DISABLED
162:                                TMOD_T1M_MODE2
|
163:                                TMOD_CT1_TIMER
|
164:                                TMOD_GATE1_DISABLED;
C:0x0833    758920  MOV     TMOD(0x89),#0x20
165:                                TCON |=
166:                                TCON_TR1_RUN ;
167:                                // UART
C:0x0836    438840  ORL     TCON(0x88),#0x40
168:                                SCON0 |=
169:                                SCON0_REN_RECEIVE_ENABLED;
170:                                // VREF
C:0x0839    439810  ORL     SCON0(0x98),#0x10
171:                                REFOCN =
172:                                REFOCN_REFSL_VDD_PIN
173:                                REFOCN_IREFLVL_1P65
174:                                REFOCN_GNDSEL_GND_PIN
175:                                REFOCN_TEMPE_TEMP_DISABLED;
176:                                // RSTSRC
C:0x083C    75D108  MOV     REFOCN(0xD1),#0x08
177:                                RSTSRC =
178:                                RSTSRC_CORSEF_NOT_SET
179:                                RSTSRC_MCDRSF_SET
|
180:                                RSTSRC_PORSF_SET
|
181:                                RSTSRC_SWRSF_NOT_SET;
182:                                // Interrupt
C:0x083F    75EF06  MOV     RSTSRC(0xEF),#0x06
183:                                IE =
184:                                IE_EA_ENABLED
185:                                IE_EXO_DISABLED
|
186:                                IE_EX1_DISABLED
|
187:                                IE_ESPIO_DISABLED
|
188:                                IE_ETO_DISABLED
|
189:                                IE_ET1_ENABLED
190:                                IE_ET2_ENABLED | // Timer 1 enabled
|
191:                                // Timer 2 enabled
192:                                IE_ESO_ENABLED;
C:0x0842    75A8B8  MOV     IE(0xA8),#IP(0xB8)
193:                                IP =
194:                                IP_PX0_LOW
195:                                IP_PX1_LOW
196:                                IP_PSPIO_LOW
197:                                IP_PTO_LOW
|
198:                                IP_PT2_HIGH | // Timer 2 highest priority
199:                                IP_PSO_LOW;
200:                                // PCA
C:0x0845    75B820  MOV     IP(0xB8),#0x20
201:                                PCAOCN_CR =

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202:          PCAOCN_CR__STOP;
C:0x0848    C2DE    CLR     PCAOCN_CR(0xD8.6)
203:          PCAOCPMO =
204:          PCAOCPMO_CAPN__DISABLED
|
205:          PCAOCPMO_ECCF__ENABLED   |
206:          PCAOCPMO_MAT__ENABLED   |
207:          PCAOCPMO_CAPP__DISABLED |
|
208:          PCAOCPMO_ECOM__ENABLED   |
209:          PCAOCPMO_PWM__ENABLED   |
210:          PCAOCPMO_TOG__DISABLED; |
C:0x084A    75DA4B    MOV     PCAOCPMO(0xDA),#0x4B
211:          PCAOCPM1 =
212:          PCAOCPM1_CAPN__DISABLED
|
213:          PCAOCPM1_ECCF__ENABLED   |
214:          PCAOCPM1_MAT__ENABLED   |
215:          PCAOCPM1_CAPP__DISABLED |
|
216:          PCAOCPM1_ECOM__ENABLED   |
217:          PCAOCPM1_PWM__ENABLED   |
218:          PCAOCPM1_TOG__DISABLED; |
C:0x084D    75DB4B    MOV     PCAOCPM1(0xDB),#0x4B
219:          PCAOMD =
220:          PCAOMD_CIDL__NORMAL      |
221:          PCAOMD_ECF__OVF_INT_DISABLED |
222:          PCAOMD_CPS__SYCLK;       |
C:0x0850    75D908    MOV     PCAOMD(0xD9),#0x08
223:          PCAOCN |=
224:          PCAOCN_CR__RUN;
225:          // Timer 2
C:0x0853    43D840    ORL     PCAOCN(0xD8),#0x40
226:          TMR2CN |= TMR2CN_TR2__RUN;
227:          // End of peripheral setup
228:
C:0x0856    43C804    ORL     TMR2CN(0xC8),#0x04
229:          enabled = false;
C:0x0859    C202    CLR     enabled(0x20.2)
230:          integral = 0;
C:0x085B    F52E    MOV     integral(0x2E),A
C:0x085D    F52F    MOV     0x2F,A
231:          target_mV = DEFAULT_OUT_MV;
C:0x085F    752513    MOV     target_mV(0x25),#0x13
C:0x0862    752688    MOV     0x26,#TCON(0x88)
232:          high_mV = DEFAULT_HIGH_MV;
C:0x0865    752717    MOV     high_mV(0x27),#0x17
C:0x0868    752870    MOV     0x28,#0x70
233:          low_mV = DEFAULT_LOW_MV;
234:
C:0x086B    75370F    MOV     low_mV(0x37),#0x0F
C:0x086E    7538A0    MOV     0x38,#0xA0
235:          SCON0_TI = 1;
C:0x0871    D299    SETB   SCON0_TI(0x98.1)
236:          SCON0_RI = 0;
237:
C:0x0873    C298    CLR     SCON0_RI(0x98.0)
238:          while (1){
239:              if(SCON0_RI){
C:0x0875    3098FD    JNB     SCON0_RI(0x98.0),C:0875
240:              SCON0_RI = 0;
C:0x0878    C298    CLR     SCON0_RI(0x98.0)
241:              uart_in[4] = uart_in[3];
// Small buffer, less code not to use loop
C:0x087A    853536    MOV     0x36,0x35
242:              uart_in[3] = uart_in[2];
C:0x087D    853435    MOV     0x35,0x34
243:              uart_in[2] = uart_in[1];
C:0x0880    853334    MOV     0x34,0x33
244:              uart_in[1] = uart_in[0];
C:0x0883    853233    MOV     0x33,uart_in(0x32)
245:              uart_in[0] = SBUFO;
246:
C:0x0886    859932    MOV     uart_in(0x32),SBUFO(0x99)
247:              uartLoadOut(uart_in[0]);
248:
C:0x0889    AF32    MOV     R7,uart_in(0x32)
C:0x088B    120B9C    LCALL  uartLoadOut(C:0B9C)
249:              switch(uart_in[0]){
C:0x088E    E532    MOV     A,uart_in(0x32)
C:0x0890    120AA6    LCALL  C?CCASE(C:0AA6)
C:0x0893    08      INC     R0
C:0x0894    B56108   CJNE   A,0x61,C:089F
C:0x0897    BD6308   CJNE   R5,#0x63,C:08A2
C:0x089A    C564    XCH    A,0x64
C:0x089C    08      INC     R0
C:0x089D    CD      XCH    A,R5
C:0x089E    67      XRL    A,@R1
C:0x089F    08      INC     R0
C:0x08A0    DA6D    DJNZ   R2,C:090F
C:0x08A2    08      INC     R0
C:0x08A3    E2      MOVX   A,@R0
C:0x08A4    6E      XRL    A,R6
C:0x08A5    08      INC     R0
C:0x08A6    D6      XCHD   A,@R0
C:0x08A7    73      JMP    @A+DPTR
C:0x08A8    08      INC     R0
C:0x08A9    EA      MOV    A,R2
C:0x08AA    7808    MOV    R0,#0x08

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C:0x08AC    F2      MOVX    @R0,A
C:0x08AD    7908    MOV     R1,#0x08
C:0x08AF    FA      MOV     R2,A
C:0x08B0    7A00    MOV     R2,#0x00
C:0x08B2    00      NOP
C:0x08B3    09      INC     R1
C:0x08B4    06      INC     @R0
250:           case 'a':   uartNumbers(target_mV,true);
C:0x08B5    D200    SETB    0x20.0
C:0x08B7    AF26    MOV     R7,0x26
C:0x08B9    AE25    MOV     R6,target_mV(0x25)
251:           break;
C:0x08BB    8043    SJMP   C:0900
252:           case 'c':   uartNumbers(current,true);
C:0x08BD    D200    SETB    0x20.0
C:0x08BF    AF22    MOV     R7,0x22
C:0x08C1    AE21    MOV     R6,current(0x21)
253:           break;
C:0x08C3    803B    SJMP   C:0900
254:           case 'd':   uartNumbers(duty,true);
C:0x08C5    AF29    MOV     R7,duty(0x29)
C:0x08C7    7E00    MOV     R6,#0x00
C:0x08C9    D200    SETB    0x20.0
255:           break;
C:0x08CB    8033    SJMP   C:0900
256:           case 'g':   enabled = true;
C:0x08CD    D202    SETB    enabled(0x20.2)
257:           integral
= 0;
C:0x08CF    E4      CLR     A
C:0x08D0    F52E    MOV     integral(0x2E),A
C:0x08D2    F52F    MOV     0x2F,A
258:           break;
C:0x08D4    809F    SJMP   C:0875
259:           case 's':   enabled = false;
C:0x08D6    C202    CLR     enabled(0x20.2)
260:           break;
C:0x08D8    809B    SJMP   C:0875
261:           case 'm':   uartNumbers(high_mV,true);
C:0x08DA    D200    SETB    0x20.0
C:0x08DC    AF28    MOV     R7,0x28
C:0x08DE    AE27    MOV     R6,high_mV(0x27)
262:           break;
C:0x08E0    801E    SJMP   C:0900
263:           case 'n':   uartNumbers(low_mV,true);
C:0x08E2    D200    SETB    0x20.0
C:0x08E4    AF38    MOV     R7,0x38
C:0x08E6    AE37    MOV     R6,low_mV(0x37)
264:           break;
C:0x08E8    8016    SJMP   C:0900
265:           case 'x':   uartNumbersadc1(true);
C:0x08EA    D200    SETB    0x20.0
C:0x08EC    AF2B    MOV     R7,0x2B
C:0x08EE    AE2A    MOV     R6,adc1(0x2A)
266:           break;
C:0x08F0    800E    SJMP   C:0900
267:           case 'y':   uartNumbersadc2(true);
C:0x08F2    D200    SETB    0x20.0
C:0x08F4    AF2D    MOV     R7,0x2D
C:0x08F6    AE2C    MOV     R6,adc2(0x2C)
268:           break;
C:0x08F8    8006    SJMP   C:0900
269:           case 'z':   uartNumbersadc3(true);
C:0x08FA    D200    SETB    0x20.0
C:0x08FC    AF31    MOV     R7,0x31
C:0x08FE    AE30    MOV     R6,adc3(0x30)
C:0x0900    120AF9  LCALL  uartNumbers(C:0AF9)
270:           break;
C:0x0903    020875  LJMP   C:0875
271:           default:  switch(uart_in[4]){
C:0x0906    E536    MOV     A,0x36
C:0x0908    2494    ADD     A,#0x94
C:0x090A    601B    JZ     C:0927
C:0x090C    24F6    ADD     A,#0xF6
C:0x090E    6027    JZ     C:0937
C:0x0910    240E    ADD     A,#0x0E
C:0x0912    6003    JZ     C:0917
C:0x0914    020875  LJMP   C:0875
272:           case 'h':
high_mV = uartNumbers(high_mV,false);
C:0x0917    C200    CLR     0x20.0
C:0x0919    AF28    MOV     R7,0x28
C:0x091B    AE27    MOV     R6,high_mV(0x27)
C:0x091D    120AF9  LCALL  uartNumbers(C:0AF9)
C:0x0920    8E27    MOV     high_mV(0x27),R6
C:0x0922    8F28    MOV     0x28,R7
273:           break;
C:0x0924    020875  LJMP   C:0875
274:           case 'l':
low_mV = uartNumbers(low_mV,false);
C:0x0927    C200    CLR     0x20.0
C:0x0929    AF38    MOV     R7,0x38
C:0x092B    AE37    MOV     R6,low_mV(0x37)
C:0x092D    120AF9  LCALL  uartNumbers(C:0AF9)
C:0x0930    8E37    MOV     low_mV(0x37),R6
C:0x0932    8F38    MOV     0x38,R7
275:           break;

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C:0x0934    020875    LJMP    C:0875
276:
target_mV      = uartNumbers(target_mV, false);
C:0x0937    C200    CLR     0x20.0
C:0x0939    AF26    MOV     R7, 0x26
C:0x093B    AE25    MOV     R6, target_mV(0x25)
C:0x093D    120AF9    LCALL   uartNumbers(C:0AF9)
C:0x0940    8E25    MOV     target_mV(0x25), R6
C:0x0942    8F26    MOV     0x26, R7
277:
integral      = 0;
C:0x0944    E4      CLR     A
C:0x0945    F52E    MOV     integral(0x2E), A
C:0x0947    F52F    MOV     0x2F, A
278:
break;
C:0x0949    020875    LJMP    C:0875
341: INTERRUPT (TIMER2_ISR, TIMER2_IRQn){           // One timer handling UART Tx and PID
342:         int out;
343:         int error;
C:0x094C    COEO    PUSH    0xE0
C:0x094E    COFO    PUSH    0xF0
C:0x0950    CODO    PUSH    0xD0
C:0x0952    75D000    MOV     0xD0, #0x00
C:0x0955    C000    PUSH    0x00
C:0x0957    C004    PUSH    0x04
C:0x0959    C005    PUSH    0x05
C:0x095B    C006    PUSH    0x06
C:0x095D    C007    PUSH    0x07
344:         TEST1 = 1;
345:
346:
C:0x095F    D294    SETB    TEST1(0x90.4)
347:         adc1 = readAdc(ADC1);
C:0x0961    7F08    MOV     R7, #0x08
C:0x0963    120B7B    LCALL   readAdc(C:0B7B)
C:0x0966    8E2A    MOV     adc1(0x2A), R6
C:0x0968    8F2B    MOV     0x2B, R7
348:         adc2 = readAdc(ADC2);
C:0x096A    7F09    MOV     R7, #0x09
C:0x096C    120B7B    LCALL   readAdc(C:0B7B)
C:0x096F    8E2C    MOV     adc2(0x2C), R6
C:0x0971    8F2D    MOV     0x2D, R7
349:         adc3 = readAdc(ADC3);
C:0x0973    7F0A    MOV     R7, #0x0A
C:0x0975    120B7B    LCALL   readAdc(C:0B7B)
C:0x0978    8E30    MOV     adc3(0x30), R6
C:0x097A    8F31    MOV     0x31, R7
350:         current = (adc2 - adc3)*10;
351:
C:0x097C    C3      CLR     C
C:0x097D    E52D    MOV     A, 0x2D
C:0x097F    9531    SUBB   A, 0x31
C:0x0981    FF      MOV     R7, A
C:0x0982    E52C    MOV     A, adc2(0x2C)
C:0x0984    9530    SUBB   A, adc3(0x30)
C:0x0986    FE      MOV     R6, A
C:0x0987    7C00    MOV     R4, #0x00
C:0x0989    7D0A    MOV     R5, #0x0A
C:0x098B    120A2C    LCALL   C7IMUL(C:0A2C)
C:0x098E    8E21    MOV     current(0x21), R6
C:0x0990    8F22    MOV     0x22, R7
352:         if((adc1 < low_mV) || (adc1 > high_mV)){           // Watch input voltage
C:0x0992    C3      CLR     C
C:0x0993    E52B    MOV     A, 0x2B
C:0x0995    9538    SUBB   A, 0x38
C:0x0997    E52A    MOV     A, adc1(0x2A)
C:0x0999    9537    SUBB   A, low_mV(0x37)
C:0x099B    400B    JC     C:09A8
C:0x099D    D3      SETB   C
C:0x099E    E52B    MOV     A, 0x2B
C:0x09A0    9528    SUBB   A, 0x28
C:0x09A2    E52A    MOV     A, adc1(0x2A)
C:0x09A4    9527    SUBB   A, high_mV(0x27)
C:0x09A6    4002    JC     C:09AA
353:         enabled = false;
C:0x09A8    C202    CLR     enabled(0x20.2)
354:     }
355:
356:
357:         error = (int)target_mV - (int)adc3;           // PID controller
C:0x09AA    AE30    MOV     R6, adc3(0x30)
C:0x09AC    AF31    MOV     R7, 0x31
C:0x09AE    AC25    MOV     R4, target_mV(0x25)
C:0x09B0    AD26    MOV     R5, 0x26
C:0x09B2    C3      CLR     C
C:0x09B3    ED      MOV     A, R5
C:0x09B4    9F      SUBB   A, R7
C:0x09B5    FF      MOV     R7, A
C:0x09B6    EC      MOV     A, R4
C:0x09B7    9E      SUBB   A, R6
C:0x09B8    FE      MOV     R6, A
358:         integral += error;
C:0x09B9    EF      MOV     A, R7
C:0x09BA    252F    ADD     A, 0x2F
C:0x09BC    F52F    MOV     0x2F, A
C:0x09BE    EE      MOV     A, R6
C:0x09BF    352E    ADDC   A, integral(0x2E)
C:0x09C1    F52E    MOV     integral(0x2E), A

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      out = ((error*P) + (integral*I)) >> 10; // Divide by 1024
C:0x09C3    7C00    MOV     R4,#0x00
C:0x09C5    7D05    MOV     R5,#0x05
C:0x09C7    120A2C  LCALL   C?IMUL(C:0A2C)
C:0x09CA    AC06    MOV     R4,0x06
C:0x09CC    AD07    MOV     R5,0x07
C:0x09CE    E52F    MOV     A,0x2F
C:0x09D0    25E0    ADD     A,0xE0
C:0x09D2    FF      MOV     R7,A
C:0x09D3    E52E    MOV     A,integral(0x2E)
C:0x09D5    33      RLC     A
C:0x09D6    FE      MOV     R6,A
C:0x09D7    ED      MOV     A,R5
C:0x09D8    2F      ADD     A,R7
C:0x09D9    FF      MOV     R7,A
C:0x09DA    EC      MOV     A,R4
C:0x09DB    3E      ADDC   A,R6
C:0x09DC    FE      MOV     R6,A
C:0x09DD    EF      MOV     A,R7
C:0x09DE    780A    MOV     R0,#0xA
C:0x09E0    CE      XCH     A,R6
C:0x09E1    A2E7    MOV     C,0xE0.7
C:0x09E3    13      RRC     A
C:0x09E4    CE      XCH     A,R6
C:0x09E5    13      RRC     A
C:0x09E6    D8F8    DJNZ   R0,C:09E0
C:0x09E8    FF      MOV     R7,A
360:         if((out < 0) || (!enabled)){
C:0x09E9    C3      CLR     C
C:0x09EA    EE      MOV     A,R6
C:0x09EB    6480    XRL     A,#0x80
C:0x09ED    9480    SUBB   A,#0x80
C:0x09EF    4003    JC     C:09F4
C:0x09F1    200202  JB     enabled(0x20.2),C:09F6
361:         out = 0;
C:0x09F4    7F00    MOV     R7,#0x00
362:     }
363:     duty = out;
C:0x09F6    8F29    MOV     duty(0x29),R7
364:     PCAOCPH0 = PCAOCPH1 = 0xFF - out;
365:
366:
367:
C:0x09F8    C3      CLR     C
C:0x09F9    74FF    MOV     A,#0xFF
C:0x09FB    9F      SUBB   A,R7
C:0x09FC    F5EA    MOV     PCAOCPH1(0xEA),A
C:0x09FE    F5FC    MOV     PCAOCPH0(0xFC),A
368:         if(head != tail){
C:0x0A00    E523    MOV     A,head(0x23)
C:0x0A02    6524    XRL     A,tail(0x24)
C:0x0A04    600E    JZ     C:0A14
369:         SBUFO = uart_out[tail]; // Timer tuned so no need to check
C:0x0A06    AF24    MOV     R7,tail(0x24)
C:0x0A08    7439    MOV     A,uart_out(0x39)
C:0x0A0A    2F      ADD     A,R7
C:0x0A0B    F8      MOV     R0,A
C:0x0A0C    E6      MOV     A,@R0
C:0x0A0D    F599    MOV     SBUFO(0x99),A
370:         tail++; // Transmit UART
C:0x0A0F    0524    INC     tail(0x24)
371:         tail %= UART_SIZE_OUT; // Wrap around
C:0x0A11    532407  ANL     tail(0x24),#0x07
372:     }
373:
374:
375:         TMR2H = 255; // Runs at 4KHz
C:0x0A14    75CDFF  MOV     TMR2H(0xCD),#0xFF
376:         TMR2CN_TF2H = 0;
// Enable interrupt again
C:0x0A17    C2CF    CLR     TMR2CN_TF2H(0xC8.7)
377:         TEST1 = 0;
// Timing debug
C:0x0A19    C294    CLR     TEST1(0x90.4)
378: }
C:0x0A1B    D007    POP    0x07
C:0x0A1D    D006    POP    0x06
C:0x0A1F    D005    POP    0x05
C:0x0A21    D004    POP    0x04
C:0x0A23    D000    POP    0x00
C:0x0A25    D0D0    POP    0xD0
C:0x0A27    D0F0    POP    0xF0
C:0x0A29    D0E0    POP    0xE0
C:0x0A2B    32      RETI
            C?IMUL:
C:0x0A2C    EF      MOV     A,R7
C:0x0A2D    8DFO    MOV     0xF0,R5
C:0x0A2F    A4      MUL     AB
C:0x0A30    A8F0    MOV     R0,0xF0
C:0x0A32    CF      XCH     A,R7
C:0x0A33    8CFO    MOV     0xF0,R4
C:0x0A35    A4      MUL     AB
C:0x0A36    28      ADD     A,R0
C:0x0A37    CE      XCH     A,R6
C:0x0A38    8DF0    MOV     0xF0,R5
C:0x0A3A    A4      MUL     AB
C:0x0A3B    2E      ADD     A,R6
C:0x0A3C    FE      MOV     R6,A
C:0x0A3D    22      RET

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C?UIDIV:
C:0x0A3E BC000B CJNE R4,#0x00,C:0A4C
C:0x0A41 BE0029 CJNE R6,#0x00,C:0A6D
C:0x0A44 EF MOV A,R7
C:0x0A45 8DFO MOV 0xF0,R5
C:0x0A47 84 DIV AB
C:0x0A48 FF MOV R7,A
C:0x0A49 ADFO MOV R5,0xF0
C:0x0A4B 22 RET
C:0x0A4C E4 CLR A
C:0x0A4D CC XCH A,R4
C:0x0A4E F8 MOV R0,A
C:0x0A4F 75F008 MOV 0xF0,#0x08
C:0x0A52 EF MOV A,R7
C:0x0A53 2F ADD A,R7
C:0x0A54 FF MOV R7,A
C:0x0A55 EE MOV A,R6
C:0x0A56 33 RLC A
C:0x0A57 FE MOV R6,A
C:0x0A58 EC MOV A,R4
C:0x0A59 33 RLC A
C:0x0A5A FC MOV R4,A
C:0x0A5B EE MOV A,R6
C:0x0A5C 9D SUBB A,R5
C:0x0A5D EC MOV A,R4
C:0x0A5E 98 SUBB A,R0
C:0x0A5F 4005 JC C:0A66
C:0x0A61 FC MOV R4,A
C:0x0A62 EE MOV A,R6
C:0x0A63 9D SUBB A,R5
C:0x0A64 FE MOV R6,A
C:0x0A65 OF INC R7
C:0x0A66 D5FOE9 DJNZ 0xF0,C:0A52
C:0x0A69 E4 CLR A
C:0x0A6A CE XCH A,R6
C:0x0A6B FD MOV R5,A
C:0x0A6C 22 RET
C:0x0A6D ED MOV A,R5
C:0x0A6E F8 MOV R0,A
C:0x0A6F F5F0 MOV 0xF0,A
C:0x0A71 EE MOV A,R6
C:0x0A72 84 DIV AB
C:0x0A73 20D21C JB 0xD0.2,C:0A92
C:0x0A76 FE MOV R6,A
C:0x0A77 ADFO MOV R5,0xF0
C:0x0A79 75F008 MOV 0xF0,#0x08
C:0x0A7C EF MOV A,R7
C:0x0A7D 2F ADD A,R7
C:0x0A7E FF MOV R7,A
C:0x0A7F ED MOV A,R5
C:0x0A80 33 RLC A
C:0x0A81 FD MOV R5,A
C:0x0A82 4007 JC C:0A8B
C:0x0A84 98 SUBB A,R0
C:0x0A85 5006 JNC C:0A8D
C:0x0A87 D5FOF2 DJNZ 0xF0,C:0A7C
C:0x0A8A 22 RET
C:0x0A8B C3 CLR C
C:0x0A8C 98 SUBB A,R0
C:0x0A8D FD MOV R5,A
C:0x0A8E OF INC R7
C:0x0A8F D5FOEA DJNZ 0xF0,C:0A7C
C:0x0A92 22 RET

C?ULSHR:
C:0x0A93 E8 MOV A,R0
C:0x0A94 600F JZ C:0AA5
C:0x0A96 EC MOV A,R4
C:0x0A97 C3 CLR C
C:0x0A98 13 RRC A
C:0x0A99 FC MOV R4,A
C:0x0A9A ED MOV A,R5
C:0x0A9B 13 RRC A
C:0x0A9C FD MOV R5,A
C:0x0A9D EE MOV A,R6
C:0x0A9E 13 RRC A
C:0x0A9F FE MOV R6,A
C:0x0AA0 EF MOV A,R7
C:0x0AA1 13 RRC A
C:0x0AA2 FF MOV R7,A
C:0x0AA3 D8F1 DJNZ R0,C:0A96
C:0x0AA5 22 RET

C?CCASE:
C:0x0AA6 D083 POP 0x83
C:0x0AA8 D082 POP 0x82
C:0x0AAA F8 MOV R0,A
C:0x0AAB E4 CLR A
C:0x0AAC 93 MOVC A,@A+DPTR
C:0x0AAD 7012 JNZ C:0AC1
C:0x0AAF 7401 MOV A,#0x01
C:0x0AB1 93 MOVC A,@A+DPTR
C:0x0AB2 700D JNZ C:0AC1
C:0x0AB4 A3 INC DPTR
C:0x0AB5 A3 INC DPTR
C:0x0AB6 93 MOVC A,@A+DPTR
C:0x0AB7 F8 MOV R0,A
C:0x0AB8 7401 MOV A,#0x01
C:0x0ABA 93 MOVC A,@A+DPTR
C:0x0ABB F582 MOV 0x82,A
C:0x0ABD 8883 MOV 0x83,R0

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C:0x0ABF    E4      CLR     A
C:0x0AC0    73      JMP     @A+DPTR
C:0x0AC1    7402   MOV     A,#0x02
C:0x0AC3    93      MOVC    A,@A+DPTR
C:0x0AC4    68      XRL    A,R0
C:0x0AC5    60EF   JZ     C:0AB6
C:0x0AC7    A3      INC     DPTR
C:0x0AC8    A3      INC     DPTR
C:0x0AC9    A3      INC     DPTR
C:0x0ACA    80DF   SJMP   C:0AAB
C?LIMUL:
C:0x0ACC    EC      MOV     A,R4
C:0x0ACD    8EFO   MOV     @FO,R6
C:0x0ACF    A4      MUL     AB
C:0x0ADO    CC      XCH    A,R4
C:0x0AD1    C5FO   XCH    A,0xF0
C:0x0AD3    CC      XCH    A,R4
C:0x0AD4    CD      XCH    A,R5
C:0x0AD5    F8      MOV     R0,A
C:0x0AD6    EF      MOV     A,R7
C:0x0AD7    A4      MUL     AB
C:0x0AD8    CE      XCH    A,R6
C:0x0AD9    C5FO   XCH    A,0xF0
C:0x0ADB    2D      ADD     A,R5
C:0x0ADC    FD      MOV     R5,A
C:0x0ADD    E4      CLR     A
C:0x0ADE    3C      ADDC   A,R4
C:0x0ADF    FC      MOV     R4,A
C:0x0AE0    E8      MOV     A,R0
C:0x0AE1    A4      MUL     AB
C:0x0AE2    2E      ADD     A,R6
C:0x0AE3    C8      XCH    A,R0
C:0x0AE4    C5FO   XCH    A,0xF0
C:0x0AE6    3D      ADDC   A,R5
C:0x0AE7    FD      MOV     R5,A
C:0x0AE8    E4      CLR     A
C:0x0AE9    3C      ADDC   A,R4
C:0x0AEA    FC      MOV     R4,A
C:0x0AEB    EF      MOV     A,R7
C:0x0AEC    A4      MUL     AB
C:0x0AED    FF      MOV     R7,A
C:0x0AEE    E5FO   MOV     A,0xF0
C:0x0AF0    28      ADD     A,R0
C:0x0AF1    FE      MOV     R6,A
C:0x0AF2    E4      CLR     A
C:0x0AF3    3D      ADDC   A,R5
C:0x0AF4    FD      MOV     R5,A
C:0x0AF5    E4      CLR     A
C:0x0AF6    3C      ADDC   A,R4
C:0x0AF7    FC      MOV     R4,A
C:0x0AF8    22      RET
296: U16 uartNumbers(U16 toSend, bool transmit){           // Tx/Rx up to 4 length numbers over UART
297:     U16 out = toSend;
C:0x0AF9    8E08   MOV     0x08,R6
C:0x0AFB    8F09   MOV     0x09,R7
298:     U16 num = 0;
C:0x0AFD    E4      CLR     A
C:0x0AFE    FB      MOV     R3,A
C:0x0AFF    FA      MOV     R2,A
299:     U16 scale = 10000;
300:     U8 test;
C:0x0B00    902710 MOV     DPTR,#0x2710
301:     U8 i = 4;
C:0x0B03    750B04 MOV     0xB,#0x04
302:     bool bad = false;
C:0x0B06    C201   CLR     0x20.1
303:     while(i){
// On zero done
C:0x0B08    E50B   MOV     A,0XB
C:0x0B0A    6059   JZ     C:0B65
304:         scale /= 10;                                // Shift
C:0x0B0C    7C00   MOV     R4,#0X00
C:0x0B0E    7DOA   MOV     R5,#0XA
C:0x0B10    AF82   MOV     R7,0X82
C:0x0B12    AE83   MOV     R6,0X83
C:0x0B14    120A3E LCALL  C7UIDIV(C:0A3E)
C:0x0B17    8E83   MOV     0x83,R6
C:0x0B19    8F82   MOV     0x82,R7
305:         i--;
C:0x0B1B    150B   DEC     0XB                                // Move through UART array
306:         test = uart_in[i] - 48;                  // ascii to num
C:0x0B1D    7432   MOV     A,#uart_in(0x32)
C:0x0B1F    250B   ADD     A,0XB
C:0x0B21    F8      MOV     R0,A
C:0x0B22    E6      MOV     A,@R0
C:0x0B23    24D0   ADD     A,#0XD0
C:0x0B25    F50A   MOV     0XA,A
307:         if(test > 10){                           // check is 0 to 9, unsigned
C:0x0B27    D3      SETB   C
C:0x0B28    940A   SUBB   A,#0XA
C:0x0B2A    4002   JC     C:0B2E
308:             bad = true;
C:0x0B2C    D201   SETB   0x20.1
309:         }
310:         num += test*scale;
// shift in to position
C:0x0B2E    AF0A   MOV     R7,0XA
C:0x0B30    7E00   MOV     R6,#0X00
C:0x0B32    AD82   MOV     R5,0X82

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C:0x0B34    AC83    MOV     R4,0x83
C:0x0B36    120A2C  LCALL   C?IMUL(C:0A2C)
C:0x0B39    EF      MOV     A,R7
C:0x0B3A    2B      ADD     A,R3
C:0x0B3B    FB      MOV     R3,A
C:0x0B3C    EE      MOV     A,R6
C:0x0B3D    3A      ADDC   A,R2
C:0x0B3E    FA      MOV     R2,A
311:           if(transmit){                                // Put if statement at back of loop to save on jumps
C:0x0B3F    3000C6  JNB    0x20.0,C:0B08
312:           num = out / scale;
// 10 powers
C:0x0B42    AE08    MOV     R6,0x08
C:0x0B44    AF09    MOV     R7,0x09
C:0x0B46    120A3E  LCALL   C?UIDIV(C:0A3E)
C:0x0B49    AA06    MOV     R2,0x06
C:0x0B4B    AB07    MOV     R3,0x07
313:           uartLoadOut(num + 48);                  // Number to ascii
C:0x0B4D    EF      MOV     A,R7
C:0x0B4E    2430    ADD     A,#adc3(0x30)
C:0x0B50    FF      MOV     R7,A
C:0x0B51    120B9C  LCALL   uartLoadOut(C:0B9C)
314:           out %= scale;                         // Remainder for next time
C:0x0B54    AE08    MOV     R6,0x08
C:0x0B56    AF09    MOV     R7,0x09
C:0x0B58    AD82    MOV     R5,0x82
C:0x0B5A    AC83    MOV     R4,0x83
C:0x0B5C    120A3E  LCALL   C?UIDIV(C:0A3E)
C:0x0B5F    8C08    MOV     0x08,R4
C:0x0B61    8D09    MOV     0x09,R5
315:           }
316:           }
C:0x0B63    80A3    SJMP   C:0B08
317:           uartLoadOut('\n');
C:0x0B65    7FOA    MOV     R7,#0x0A
C:0x0B67    120B9C  LCALL   uartLoadOut(C:0B9C)
318:           uartLoadOut('\r');
C:0x0B6A    7FD0    MOV     R7,#0x0D
C:0x0B6C    120B9C  LCALL   uartLoadOut(C:0B9C)
319:           if(bad){
C:0x0B6F    300104  JNB    0x20.1,C:0B76
320:           num = DEFAULT_OUT_MV;                  // Not all valid numbers so set output as default
C:0x0B72    7A13    MOV     R2,#0x13
C:0x0B74    7B88    MOV     R3,#TCON(0x88)
321:           }
322:           return num;
C:0x0B76    AE02    MOV     R6,0x02
C:0x0B78    AF03    MOV     R7,0x03
323:   }
324:
C:0x0B7A    22      RET
325: U16 readAdc(U8 sel){                                // Read the available ADCs
326:   U8 i;
327:   ADCOMX = sel;
C:0x0B7B    8FB8    MOV     ADCOMX(0xBB),R7
328:   for(i=0;i<2;i++){
C:0x0B7D    E4      CLR     A
C:0x0B7E    FF      MOV     R7,A
329:   ADCOCNO |= ADCOCNO_ADBUSY__SET;
C:0x0B7F    43E810  ORL    ADCOCNO(0xE8),#0x10
330:   while(ADCOENO & ADCOCNO_ADBUSY__SET);        // Wait for sample to complete
C:0x0B82    E5E8    MOV     A,ADCOENO(0xE8)
C:0x0B84    20E4FB  JB     0xE0.4,C:0B82
331:   }
C:0x0B87    0F      INC     R7
C:0x0B88    BF02F4  CJNE   R7,#0x02,C:0B7F
332:   return (((U32)ADCO)*SCALE_MUL) >> 10;          // Scale to mV
C:0x0B8B    AFBD    MOV     R7,ADCO(0xBD)
C:0x0B8D    AEBE    MOV     R6,0xBE
C:0x0B8F    7C17    MOV     R4,#0x17
C:0x0B91    7DB4    MOV     R5,#0xB4
C:0x0B93    120ACC  LCALL   C?LIMUL(C:0ACC)
C:0x0B96    780A    MOV     R0,#0xA
C:0x0B98    120A93  LCALL   C?ULSHR(C:0A93)
333:   }
334:
335: //-----
336: // Interrupt Routines
337: //-----
338:
C:0x0B9B    22      RET
290: void uartLoadOut(U8 tx){                           // Handle buffering out Tx UART
291:   uart_out[head] = tx;                            // Buffer outgoing
C:0x0B9C    AE23    MOV     R6,head(0x23)
C:0x0B9E    7439    MOV     A,#uart_out(0x39)
C:0x0BA0    2E      ADD     A,R6
C:0x0BA1    F8      MOV     R0,A
C:0x0BA2    A607    MOV     @R0,0x07
292:   head++;
C:0x0BA4    0523    INC     head(0x23)
293:   head %= UART_SIZE_OUT;                      // Wrap around
C:0x0BA6    532307  ANL    head(0x23),#0x07
294:   }
C:0x0BA9    22      RET
C:0x0BAA    787F    MOV     R0,#0x7F
C:0x0BAC    E4      CLR     A
C:0x0BAD    F6      MOV     @R0,A
C:0x0BAE    D8FD    DJNZ   R0,C:0BAD

```

```

C:0x0BB0    758140  MOV      0x81,#0x40
C:0x0BB3    020800  LJMP     main(C:0800)
339: INTERRUPT (TIMER1_ISR, TIMER1_IRQn{})           // Needed for UART timing
C:0x0BB6    32      RETI

```

Listing 5: LIMUL

```

C?LIMUL:
C:0x0ACC    EC      MOV      A,R4
C:0x0ACD    8EF0    MOV      0xF0,R6
C:0x0ACF    A4      MUL      AB
C:0x0ADO    CC      XCH      A,R4
C:0x0AD1    C5F0    XCH      A,0xF0
C:0x0AD3    CC      XCH      A,R4
C:0x0AD4    CD      XCH      A,R5
C:0x0AD5    F8      MOV      R0,A
C:0x0AD6    EF      MOV      A,R7
C:0x0AD7    A4      MUL      AB
C:0x0AD8    CE      XCH      A,R6
C:0x0AD9    C5F0    XCH      A,0xF0
C:0x0ADB    2D      ADD      A,R5
C:0x0ADC    FD      MOV      R5,A
C:0x0ADD    E4      CLR      A
C:0x0ADE    3C      ADDC     A,R4
C:0x0ADF    FC      MOV      R4,A
C:0x0AE0    E8      MOV      A,R0
C:0x0AE1    A4      MUL      AB
C:0x0AE2    2E      ADD      A,R6
C:0x0AE3    C8      XCH      A,R0
C:0x0AE4    C5F0    XCH      A,0xF0
C:0x0AE6    3D      ADDC     A,R5
C:0x0AE7    FD      MOV      R5,A
C:0x0AE8    E4      CLR      A
C:0x0AE9    3C      ADDC     A,R4
C:0x0AEA    FC      MOV      R4,A
C:0x0AEB    EF      MOV      A,R7
C:0x0AEC    A4      MUL      AB
C:0x0AED    FF      MOV      R7,A
C:0x0AEE    E5F0    MOV      A,0xF0
C:0x0AF0    28      ADD      A,R0
C:0x0AF1    FE      MOV      R6,A
C:0x0AF2    E4      CLR      A
C:0x0AF3    3D      ADDC     A,R5
C:0x0AF4    FD      MOV      R5,A
C:0x0AF5    E4      CLR      A
C:0x0AF6    3C      ADDC     A,R4
C:0x0AF7    FC      MOV      R4,A
C:0x0AF8    22      RET

```

Listing 6: ULSHR

```

C?ULSHR:
C:0x0A93    E8      MOV      A,R0
C:0x0A94    600F    JZ      C:0AA5
C:0x0A96    EC      MOV      A,R4
C:0x0A97    C3      CLR      C
C:0x0A98    13      RRC      A
C:0x0A99    FC      MOV      R4,A
C:0x0A9A    ED      MOV      A,R5
C:0x0A9B    13      RRC      A
C:0x0A9C    FD      MOV      R5,A
C:0x0A9D    EE      MOV      A,R6
C:0x0A9E    13      RRC      A
C:0x0A9F    FE      MOV      R6,A
C:0x0AA0    EF      MOV      A,R7
C:0x0AA1    13      RRC      A
C:0x0AA2    FF      MOV      R7,A
C:0x0AA3    D8F1    DJNZ   R0,C:0A96
C:0x0AA5    22      RET

```

Listing 7: IMUL

```

C?IMUL:
C:0x0A2C    EF      MOV      A,R7
C:0x0A2D    8DF0    MOV      0xF0,R5
C:0x0A2F    A4      MUL      AB
C:0x0A30    A8F0    MOV      R0,0xF0
C:0x0A32    CF      XCH      A,R7
C:0x0A33    8CFO    MOV      0xF0,R4
C:0x0A35    A4      MUL      AB
C:0x0A36    28      ADD      A,R0
C:0x0A37    CE      XCH      A,R6
C:0x0A38    8DF0    MOV      0xF0,R5
C:0x0A3A    A4      MUL      AB
C:0x0A3B    2E      ADD      A,R6
C:0x0A3C    FE      MOV      R6,A
C:0x0A3D    22      RET

```

Listing 8: UDIV

```

C?UDIV:

```

C : 0xA3E	B000B	CJNE	R4 ,#0x00 ,C : 0A4C
C : 0xA41	B0029	CJNE	R6 ,#0x00 ,C : 0A6D
C : 0xA44	EF	MOV	A ,R7
C : 0xA45	8DF0	MOV	0xF0 ,R5
C : 0xA47	84	DIV	AB
C : 0xA48	FF	MOV	R7 ,A
C : 0xA49	ADFO	MOV	R5 ,0xF0
C : 0xA4B	22	RET	
C : 0xA4C	E4	CLR	A
C : 0xA4D	CC	XCH	A ,R4
C : 0xA4E	F8	MOV	R0 ,A
C : 0xA4F	75F008	MOV	0xF0 ,#0x08
C : 0xA52	EF	MOV	A ,R7
C : 0xA53	2F	ADD	A ,R7
C : 0xA54	FF	MOV	R7 ,A
C : 0xA55	EE	MOV	A ,R6
C : 0xA56	33	RLC	A
C : 0xA57	FE	MOV	R6 ,A
C : 0xA58	EC	MOV	A ,R4
C : 0xA59	33	RLC	A
C : 0xA5A	FC	MOV	R4 ,A
C : 0xA5B	EE	MOV	A ,R6
C : 0xA5C	9D	SUBB	A ,R5
C : 0xA5D	EC	MOV	A ,R4
C : 0xA5E	98	SUBB	A ,R0
C : 0xA5F	4005	JC	C : 0A66
C : 0xA61	FC	MOV	R4 ,A
C : 0xA62	EE	MOV	A ,R6
C : 0xA63	9D	SUBB	A ,R5
C : 0xA64	FE	MOV	R6 ,A
C : 0xA65	0F	INC	R7
C : 0xA66	D5FOE9	DJNZ	0xF0 ,C : 0A52
C : 0xA69	E4	CLR	A
C : 0xA6A	CE	XCH	A ,R6
C : 0xA6B	FD	MOV	R5 ,A
C : 0xA6C	22	RET	
C : 0xA6D	ED	MOV	A ,R5
C : 0xA6E	F8	MOV	R0 ,A
C : 0xA6F	F5FO	MOV	0xF0 ,A
C : 0xA71	EE	MOV	A ,R6
C : 0xA72	84	DIV	AB
C : 0xA73	20D21C	JB	0xD0 .2 ,C : 0A92
C : 0xA76	FE	MOV	R6 ,A
C : 0xA77	ADFO	MOV	R5 ,0xF0
C : 0xA79	75F008	MOV	0xF0 ,#0x08
C : 0xA7C	EF	MOV	A ,R7
C : 0xA7D	2F	ADD	A ,R7
C : 0xA7E	FF	MOV	R7 ,A
C : 0xA7F	ED	MOV	A ,R5
C : 0xA80	33	RLC	A
C : 0xA81	FD	MOV	R5 ,A
C : 0xA82	4007	JC	C : 0A8B
C : 0xA84	98	SUBB	A ,R0
C : 0xA85	5006	JNC	C : 0A8D
C : 0xA87	D5FOF2	DJNZ	0xF0 ,C : 0A7C
C : 0xA88	22	RET	
C : 0xA8B	C3	CLR	C
C : 0xA8C	98	SUBB	A ,R0
C : 0xA8D	FD	MOV	R5 ,A
C : 0xA8E	0F	INC	R7
C : 0xA8F	D5FOEA	DJNZ	0xF0 ,C : 0A7C
C : 0xA92	22	RET	

Listing 9: CCASE

C ?CCASE :			
C : 0xAA6	D083	POP	0x83
C : 0xAA8	D082	POP	0x82
C : 0AAA	F8	MOV	R0 ,A
C : 0AAB	E4	CLR	A
C : 0AAC	93	MOVC	A ,@A+DPTR
C : 0AAD	7012	JNZ	C : 0AC1
C : 0AAF	7401	MOV	A ,#0x01
C : 0AB1	93	MOVC	A ,@A+DPTR
C : 0AB2	700D	JNZ	C : 0AC1
C : 0AB4	A3	INC	DPTR
C : 0AB5	A3	INC	DPTR
C : 0AB6	93	MOVC	A ,@A+DPTR
C : 0AB7	F8	MOV	R0 ,A
C : 0AB8	7401	MOV	A ,#0x01
C : 0ABA	93	MOVC	A ,@A+DPTR
C : 0ABB	F582	MOV	0x82 ,A
C : 0ABD	8883	MOV	0x83 ,R0
C : 0ABF	E4	CLR	A
C : 0AC0	73	JMP	@A+DPTR
C : 0AC1	7402	MOV	A ,#0x02
C : 0AC3	93	MOVC	A ,@A+DPTR
C : 0AC4	68	XRL	A ,R0
C : 0AC5	60EF	JZ	C : 0AB6
C : 0AC7	A3	INC	DPTR
C : 0AC8	A3	INC	DPTR
C : 0AC9	A3	INC	DPTR
C : 0ACA	80DF	SJMP	C : 0AAB
