FAST NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES
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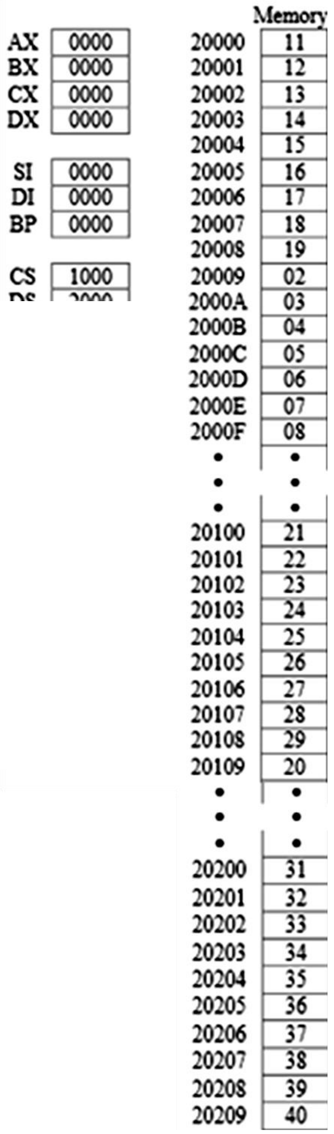
Quiz 1 Fall 2018

Section E & F

Computer Organization & Assembly Language (EE 213)

Student Roll No: ________________ Max. Marks: 2 Marks

Q No. 1 Determine the values of the indicated registers or memory locations (show working) after executing the following instructions:



AX	0000
BX	0000
CX	0000
DX	0000
SI	0000
DI	0000
BP	0000
CS	1000
DS	2000

	Memory
20000	11
20001	12
20002	13
20003	14
20004	15
20005	16
20006	17
20007	18
20008	19
20009	02
2000A	03
2000B	04
2000C	05
2000D	06
2000E	07
2000F	08
•	•
•	•
•	•
20100	21
20101	22
20102	23
20103	24
20104	25
20105	26
20106	27
20107	28
20108	29
20109	20
•	•
•	•
•	•
20200	31
20201	32
20202	33
20203	34
20204	35
20205	36
20206	37
20207	38
20208	39
20209	40

(i)

```
MOV  EBX, 20104H
INC  EBX
SUB  EBX, 4
MOV  EAX, [EBX]   ; EAX= ........................
                  ; EBX= ........................
```

(ii)

```
MOV ECX, 20007H
INC [ECX]
ADD CH, CL        ; ECX= ........................
```

(iii)

```
MOV EDI, 20109H
MOV EAX, 0304
MOV AH, [EDI]
MOV [2000h], EAX
```

[2000H]= ....

[2000H]= ....

(iv) Suppose an integer array stores in its first element the sum of its elements. Write x86 assembly code snippet that adds element 1 to 5 of this array and places the sum in element 0. Assume each element of size 2 bytes and array starting from memory location 0F345H. ***Note: Drawing a memory map of this array help you understanding the problem more clearly. Only write assembly instructions, do not declare variables or write assembler directives.***

Q. No. 2 Explain the roles of Compiler and OS in executing a HLL program from a text file. Why the process of Linking is performed? ***Note: Your answer should not be more than three (3) sentences.***

Q. No. 3 Why two micro-architectures can be completely different but implements the same ISA? Define ISA and Micro-architecture before answering the question. ***Note: Your answer should not be more than three (3) sentences.***

Q1

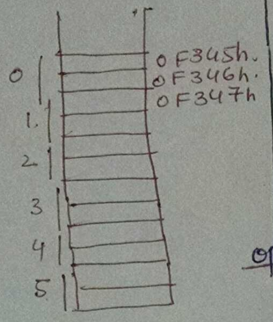
	EAX				EBX			
(i)	25	24	23	22	00	02	01	01

(ii) 0002 07 07h.
00 02 00 07

(iii) 04. 0 0 00 03 04
04. 00 00 20 04.

(iv) (sol #1)

```
    MOV DL,
    MOV ~~E~~CX, 0.
    MOV. EBX, [0F345h+2]
HERE: ADD ~~E~~CX, [EBX].
      ADD EBX, 2.
      INC DL.
      CMP DL, 5
      JNE HERE.
    MOV. [0F345h], CX.
```



sol #2.

→ array word 6 DUP(20).

```
   MOV DX, 0.
   MOV CX, 5
L1: ADD DX, [array + ECX * TYPE array].
   LOOP L1.
   MOV array, DX
```

array: Base (Fixed).
ECX: offset (changed by loop)
TYPE array: opread size. (adjust BYTE, WORD, DWORD). elelem size)

Loop instruction and ~~[illegible]~~ operand addressing help redue code to few lines. Less instruction → less change of error → less debuging time//.

Q2

- Compiler converts HLL code into machine code but doesn't resolve references to external function calls. It creates object code files given one or more HLL files.
- Linker ~~[illegible]~~ resolves. library calls in object code. with library files and create an executable file.
- OS component called loader load executable files from filesystem into memory (population code, data and stacks portions) and start executions.

Q3.

- Instruction Set Architecture (ISA) specifies processor design to the programer (assembly programer, compiler writer, etc). It contain all instructions, operand access to/from memory, data represtation, syntax of allowed instruction, etc.
- Micro-architecture implements an ISA as a complex digital Circuit.
- Two diffent teams of computer Engineers can implement the same ISA differently by designing ~~a~~ two differet microarchitecures. The differences could be (i) diffent clock speeds, (ii) cache sizes (even no. of caches), (iii) diffent design of control unit, (iv) efficient design of ~~[illegible]~~ Datapath, etc.