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## Thapar Institute of Engineering & Technology, Patiala Department of Computer Science and Engineering MID SEMESTER EXAMINATION

B. E. (Third Year): Semester-V (2023/24) (COE)		Course Code: UCS510 Course Name: Computer Architecture and Organization
Date: September 28, 2023		Time: 3:00 PM – 5:00 PM
Duration: 2 Hours, M. Marks: 35		Name of Faculty: ANJ, MJU, SOL, YAS

Note:	Attempt all questions in a proper sequence with justification. Assume missing data, if any, suitably.	
Q1(a)	A seven-segment display decoder takes a 4-bit data input, $D_3$ , $D_2$ , $D_1$ , $D_0$ and produces seven outputs to control light-emitting diodes to display a digit from 0 to 9. The seven outputs are often called segments a through $g$ , or $S_a$ - $S_g$ , as defined in Fig 1. The digits are shown in Fig 2. Write a truth table for the outputs. Find simplified Boolean equations for outputs $S_a$ and $S_b$ .	(5)
	7-segment display decoder s 7/-  a f g b e c d 0 1 2 3 4 5 6 7 8 9	
	Fig 1. Fig 2.	
Q1(b)	Design a combinational circuit with three inputs A, B, C and three outputs X, Y, Z. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Give simplified solution and justify your answer by giving Boolean equations.	(4)
Q2(a)	Design an arithmetic circuit with one selection variable S and two 4-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry $C_{in}$ .  S $C_{in}=0$ $C_{in}=1$	(4)
	S C <sub>tn</sub> =0 C <sub>tn</sub> =1 0 D=A+B D=A+1 1 D=A-1 D=A-B	
Q2(b)	Design a 4-bit shift circuit and find the value of output H, if input A is 1101, at S = 0: Shift Left, at S=1: Shift Right operation, assume missing bits as zero only.	(5)
Q3(a)	Discuss and design the Control unit of Basic Computer by taking Memory size 4096x16.	(5)
Q3(b)	An output program resides in memory starting from address 8FFF (hexadecimal). It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1).  i. What instruction must be placed at address 1 and Explain the reason?  ii. What must be the last two instructions of the output program along with explanation?	(4)
Q4(a)	Show the contents in hexadecimal of registers PC, AR, AC, DR, IR, and SC, E of the basic computer when an instruction is fetched from memory and executed. The initial content of PC is 9FF. The content of memory at address 9FF is 9A9F. The content of memory at address A9F is 0D36. The content of memory at address D36 is EEEE. The content of AC is 8BBB, Assume initial bit of E as 0. Give the answer in a table at each clock pulse with seven columns, one for each register and a row for each timing signal.	(4)
Q4(b)	A computer uses a memory unit with 2K words of 24 bits. A binary instruction code is stored in one word of memory. The instruction has four parts namely a mode bit, an operation code, a register code part to specify one of 60 registers and a signed immediate operand.  i. How many bits are there in operation code and register code field?  ii. What would be the maximum and minimum value of immediate operand?  iii. How many bits are there in the data and address inputs of the memory?	(4)