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CS 3350B: Assignment 4

Solution 1: Determining the minimum size in bits of each of the four inter-stage registers in a MIPS Datapath:

- IF/ID (Instruction Fetch/Instruction Decode): This register typically needs to hold at least the instruction that has been fetched from memory. MIPS instructions are 32 bits, so we need 32 bits to store the instruction. However, we also need to consider additional control signals and possibly the incremented program counter (PC) that will also be stored. The PC is also 32 bits wide.

  IF/ID: 32 bits for the instruction + 32 bits for the incremented PC = 64 bits

- ID/EX (Instruction Decode/Execution): This register must hold the information necessary for the execution stage. This includes:
  - The opcode and the function code, which are part of the instruction (already 32 bits).
  - Two register values to be used by the ALU (each 32 bits, so 64 bits in total).
  - Instruction [20-16], 5 bits (Rs)
  - Instruction [15-11], 5 bits (Rt)
  - The sign-extended immediate value (32 bits).
  - control signals: It would be 2 bits for WB (MemToReg, RegWrite), 3 bits for M (MemRead, MemWrite, Branch) and 5 bits for EX (ALUOp, ALUSrc, RegDst).

  ID/EX: 5 (Rs) + 5 (Rt) + 32 (Sign-extend) + 64 (Two register data outputs) + 32 (PC+4) + 2 + 3 + 5 (Control signals) = 148 bits

- EX/MEM (Execution/Memory Access): This stage must pass along the results of the execution, which may include:
    - The ALU result (32 bits).
    - Branch address (32 bits).
    - A second operand for memory write-back (32 bits).
    - The destination register number for write-back (5 bits).
    - Control signals: 2 bits for WB (MemToReg, RegWrite), 3 bits for M (MemRead, MemWrite, Branch).
    - Zero-flag bit: The ALU result is zero, and so it is 1 bit.

  EX/MEM: 32 (ALU result) +32 (branch address) + 32 (second operand) + 5 (destination register ID) + 2 + 3 (Control signals) + 1(zero flag) = 107 bits

- MEM/WB (Memory Access/Write Back): This register is between the memory access and the write-back stage. It needs to carry:
    - The ALU result or the address for the memory access (32 bits).
    - The data read from memory(32 bits).
    - The destination register number (5 bits).
    - Control signals: 2 bits for the (WB) write-back stage (MemToReg, RegWrite).

  MEM/WB: 32 (ALU result) + 5 (destination register ID) + 32 (Read Data) + 2 (control signals) = 71 bits

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Solution 2:

Explanation:

- **P1 Read**: P1 reads from main memory and the block is in Exclusive state in P1's cache.
- **P1 Write**: P1 modifies the block, so it's in Modified state in P1's cache.
- **P2 Read**: P2 reads the block from P1's cache, so the block is in Shared state in both P1 and P2's caches.
- **P3 Write**: P3 writes to the block, so it's in Modified state in P3's cache and Invalid in others.
- **P1 Read**: P1 reads the block from P3's cache, so the block is in Shared state in P1 and P3's caches.
- **P4 Read**: P4 reads the block, so it's in Shared state in P1, P3, and P4's caches.
- **P3 Read**: No change, as P3 already has the block in Shared state.
- **P2 Read**: P2 reads the block, so it's in Shared state in all caches.

- **P3 Write**: P3 writes to the block, so it's in Modified state in P3's cache and Invalid in others.
- **P4 Write**: P4 writes to the block, so it's in Modified state in P4's cache and Invalid in others.
- **P2 Read**: P2 reads the block from P4's cache, so it's in Shared state in P2 and P4's caches.
- **P4 Write**: Modified state in P4's cache and Invalid in others.

Op	P1	P2	P3	P4	Data Supplier
P1 Read	E	-	-	-	Main Memory
P1 Write	M	-	-	-	None
P2 Read	S	S	-	-	P1
P3 Write	I	I	M	-	None
P1 Read	S	I	S	-	P3
P4 Read	S	I	S	S	P1, P3
P3 Read	S	I	S	S	None
P2 Read	S	S	S	S	P1, P3, P4
P3 Write	I	I	M	I	None
P4 Write	I	I	I	M	None
P2 Read	I	S	I	S	P4
P4 Write	I	I	I	M	None

Solution 3:

(a) The pipeline execution diagram for one iteration of the loop: from the first lw, up to and including the bne (with no data forwarding) can be found on the page below:

(b) The pipeline execution diagram for one iteration of the loop: from the first lw, up to and including the bne (with data forwarding) can be found on the page below:

	Clock 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
lw	IF	ID	EX	ME	WB																	
lw		IF	ID	EX	ME	WB																
nop			–	–	–	–	–															
nop				–	–	–	–	–														
sw					IF	ID	EX	ME	WB													
addi						IF	ID	EX	ME	WB												
nop							–	–	–	–	–											
nop								–	–	–	–	–										
sw									IF	ID	EX	ME	WB									
addi										IF	ID	EX	ME	WB								
addi											IF	ID	EX	ME	WB							
addi												IF	ID	EX	ME	WB						
nop													–	–	–	–	–					
nop														–	–	–	–	–				
slt															IF	ID	EX	ME	WB			
nop																–	–	–	–	–		
nop																	–	–	–	–	–	
bne																		IF	ID	EX	ME	WB

3A

	Clock 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
lw	IF	ID	EX	ME	WB																	
lw		IF	ID	EX	ME	WB																
sw			IF	ID	EX	ME	WB															
addi				IF	ID	EX	ME	WB														
sw					IF	ID	EX	ME	WB													
addi						IF	ID	EX	ME	WB												
addi							IF	ID	EX	ME	WB											
addi								IF	ID	EX	ME	WB										
slt									IF	ID	EX	ME	WB									
bne										IF	ID	EX	ME	WB								

3B

Solution 4:

(a) The access results are:

Time	Memory Access	Hit/Miss type	Time	Memory Access	Hit/Miss type
1	P1 Reads 5	Cold Miss	11	P2 Writes 9	Hit
2	P2 Writes 8	Cold Miss	12	P2 Writes 10	Cold Miss
3	P1 Reads 9	Cold Miss	13	P2 Reads 2	Cold Miss
4	P1 Writes 14	Cold Miss	14	P1 Writes 7	Cold Miss
5	P1 Reads 3	Cold Miss	15	P1 Reads 8	False Share
6	P1 Writes 12	Cold Miss	16	P1 Reads 4	Conflict Miss
7	P2 Reads 6	Cold Miss	17	P2 Reads 12	Cold Miss
8	P2 Reads 17	Cold Miss	18	P2 Reads 7	True Share
9	P1 Reads 20	Cold Miss	19	P1 Writes 2	Hit
10	P2 Reads 4	Cold Miss	20	P1 Reads 11	Cold Miss

(b), (c) The data stored and the MESI state of each cache block after all addresses in the list have been accessed is:

P1 Cache				P2 Cache			
Set	Cache Block Data		State	Set	Cache Block Data		State
0	8	9	S	0	8	9	S
					16	17	E
1	2	3	M	1	10	11	S
	10	11	S		2	3	I
2	20	21	E	2	4	5	S
	~~12~~ 4	~~13~~ 5	S		12	13	E
3	14	15	M	3	6	7	S
	6	7	S				