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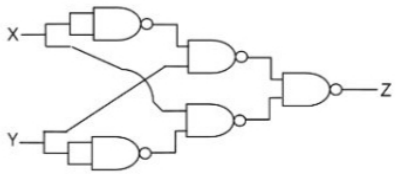
GATE Question Paper 2010, IN Question Number 42

Question 42 Analysis

Question:

The logic gate circuit shown in the figure realizes the function



(A) XOR (B) XNOR (C) Half adder (D) Full adder

Step-by-step Analysis of the Circuit

Let the inputs be:

- **X** and **Y** (two binary inputs)

Now examine the circuit:

1. **Top-left gate (AND):** Input: X, Y
   Output $= X \cdot Y$
2. **Bottom-left gate (NOR):** Input: X, Y
   Output $= \overline{X + Y}$
3. **Middle gate (NAND):** Input: X, Y
   Output $= \overline{X \cdot Y}$
4. **Final gate (OR):** Input: outputs from NOR and NAND gates
   Output $= \overline{X + Y} + \overline{X \cdot Y}$

Truth Table

X	Y	$\overline{X+Y}$	$\overline{X \cdot Y}$	$Z = \overline{X+Y} + \overline{X \cdot Y}$
0	0	1	1	1
0	1	0	1	1
1	0	0	1	1
1	1	0	0	0

This is the **truth table for XOR**.

Final Answer

(A) XOR

Brief Discussion

The circuit implements:

$$Z = \overline{X + Y} + \overline{X \cdot Y}$$

This matches the behavior of the XOR gate, which outputs 1 only when exactly one of the inputs is 1. Therefore, the circuit realizes the XOR logic function.