On Chip Clock Multiplier using PLL for 40-100MHz @1.8V in 130nm CMOS

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***Abstract*—A 40-100MHz phase locked loop designed in a Sky water 130-nm CMOS technology to be used as an analog IP to compensate PVT variations is discussed in this paper. PLL is an important sub-system in the analog/mixed signal IC design. PLL converts a low-frequency clock to high-frequency clock in multiples of the reference clock. VCO is the main block of PLL that is more prone to the PVT variations. A special compensation circuitry is developed to maintain stability of the PLL.**

Keywords—PLL, Sky Water 130-nm, PVT corners, frequency divider, Voltage Controlled Oscillator.

I. Introduction

A Phase Locked Loop is the most demanded in on-chip clock synthesis. Stability of the frequency i.e., low jitter that is synthesized from the PLL is the main concern. PLL is used in the demodulation of FSK and FM and mainly as a Clock multiplier in microprocessors. It has been built as monolithic IC's.[1]

PLL can be used to generate new frequencies that are stable and are the multiples of the input reference frequency. It is mainly for the conversion of Low input frequency from Off-chip Peripherals to High frequency for the microprocessor.[1]

II. Basic Blocks of Pll

A. Phase Frequency Detector

The PFD is the most widely used type of phase detector. A sequential PFD is used along with Charge Pump configuration for the effective charge and discharge of the output of PFD.[2]

B. Loop Filter

To remove the high frequency component from the output of phase/frequency detector, a Low pass filter is used to present DC level to the VCO(i.e., constant input control voltage). A typical loop filter produces a control voltage that is proportional to both the phase error and the integral of the phase error.[1,2]

C. Voltage Controlled Oscillator

Based on the input control voltage from the loop filter the output frequency of the PLL can be varied. It is the central block of a PLL. Along with the input control voltage the PVT corners are also responsible for the variation of frequency of the VCO. Thereby influencing gain and stability of the VCO. [3,4]

III. Impact of PVT Corners on PLL

PVT corners will have effect on two parameters. They are the power consumption high jitter at the output frequency. Power consumption is extremely varied in fast technology processes (FF) and low temperatures, variations in the input voltage also results in power increase. Whereas in the case of slow PVT corners in order to maintain functionality the circuit properly, it has to be reshaped, so that the circuit requires necessary current. This leads to an increase in the currents in typical and fast PVT corners. [3,4]

IV. Self Compensating Pll

For the detections of the PVT variations, the output frequency of the VCO is compared with the input reference clock. This variation in frequency is given as an input to RTL-block. This block generates a count that will be used as the deciding parameter for the frequency deviation. Fig.1 shows the block-diagram of a self-compensating PLL.[3]

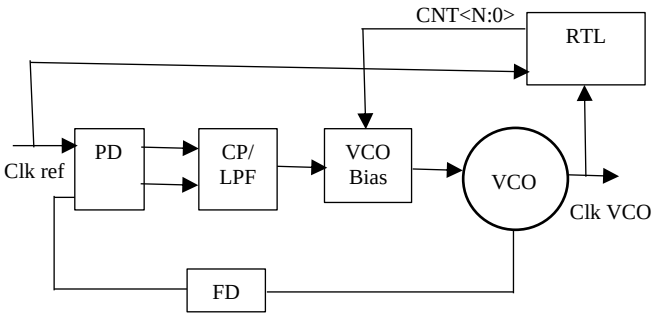

Fig.1 PVT Compensation in PLL

V.Conclusion

The PVT variations will degrade the PLL in terms of power consumption and output clock jitter. A compensated method may be designed which does not require any other off chip parameters but the input reference clock itself. A Compensated PLL is to be designed to reduce the overall power consumption and synthesized clock jitter.[3,4]

References

[1] N. H. E. Weste and D. M. Harris, CMOS VLSI design: a circuits and systems perspective. Pearson, 2015.

[2] Design of CMOS Phase Locked Loop:from circuit level to architecture level.Behzad Razhavi, University of California, Los Angeles.

[3] Melikyan, V., Durgaryan, A., Khachatryan, A., Hayk, M., & Musaelyan, E. (2013). *Self compensating low noise low power PLL design. East-West Design & Test Symposium (EWDTS 2013).* doi:10.1109/ewdts.2013.6673187

[4] "*K.Chong, L.Siek, B. Lau „A PLL with a VCO of improved PVT tolerance*" in Proc. IEEE International symposium on Intgrated Circuits , 2011, pp. -464-467