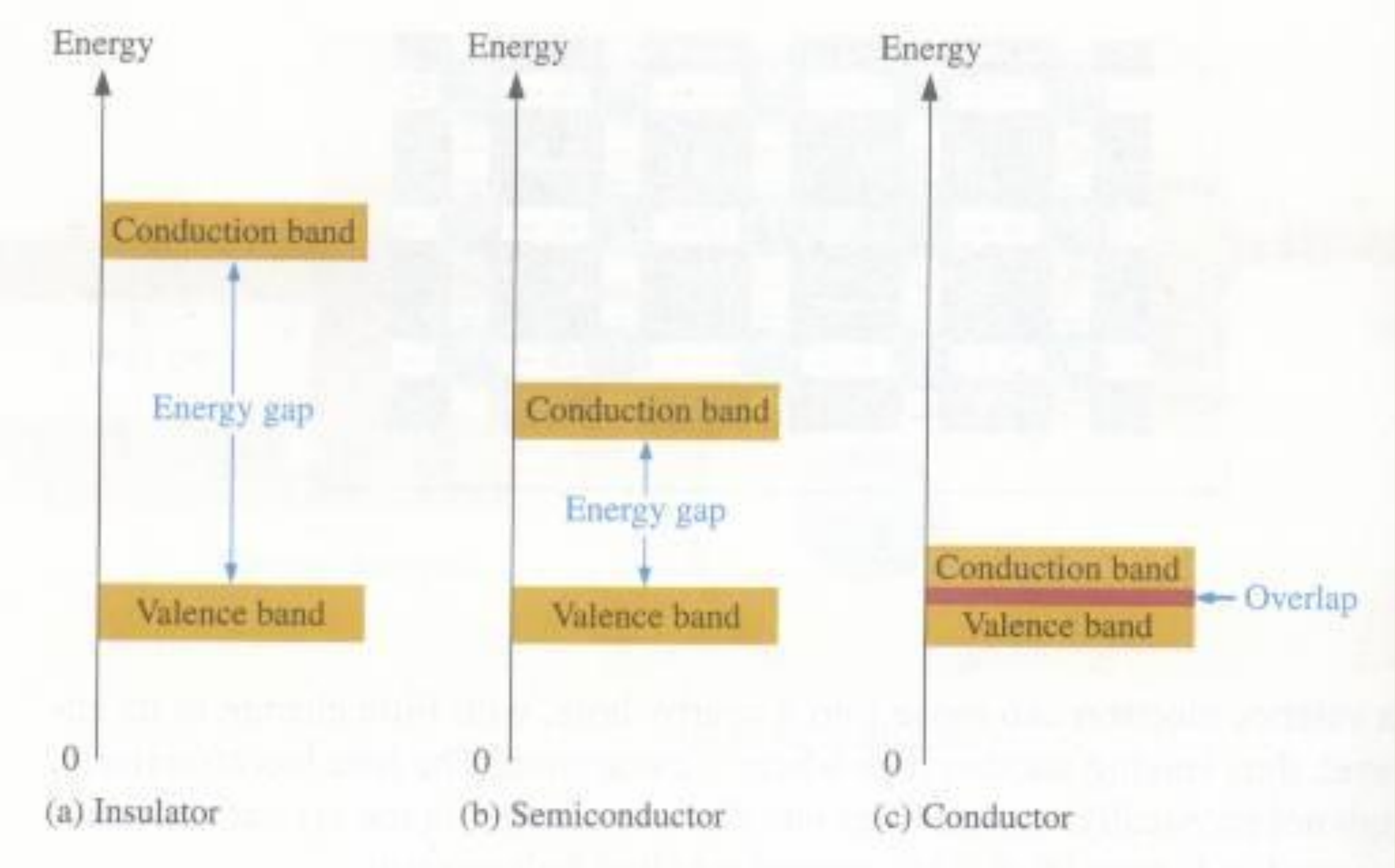
Unit-2

PN junction diode and its applications

Basic Diode Concepts

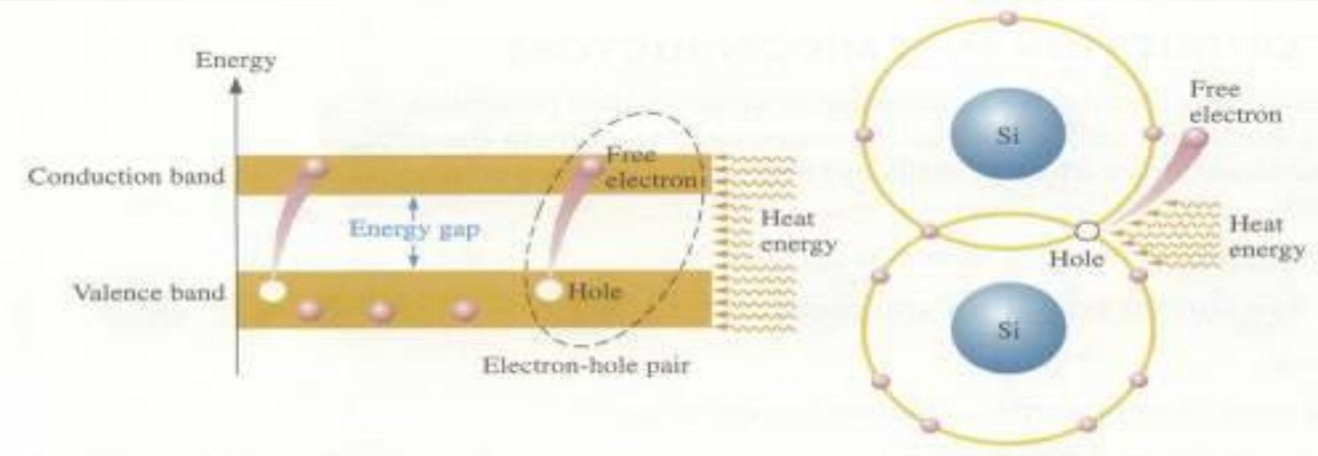
* Energy Diagrams – *Insulator, Semiconductor, and Conductor*

the energy diagram for the three types of solids

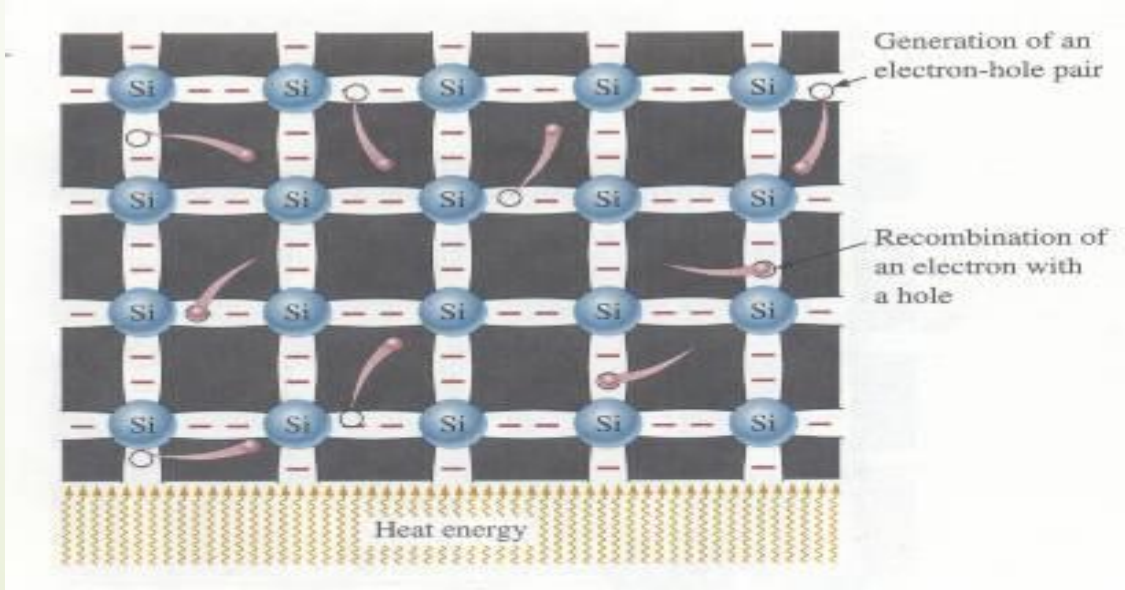


Intrinsic Semiconductors

* Intrinsic (pure) *Si* Semiconductor:



(a) Energy diagram
(b) Bonding diagram

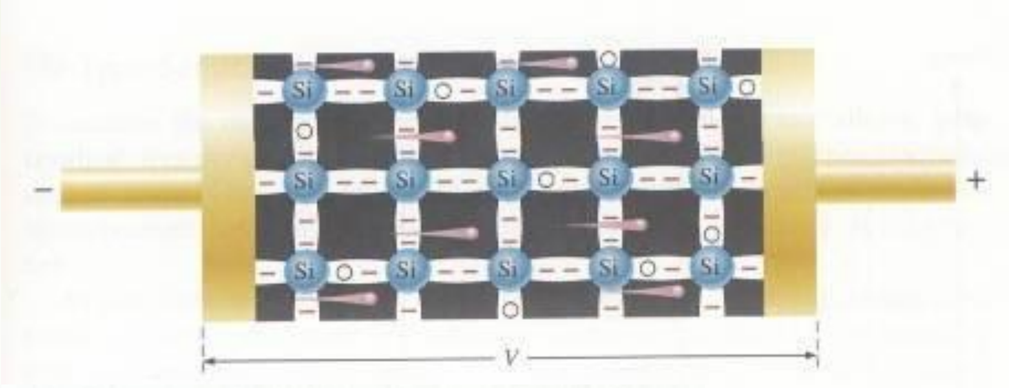


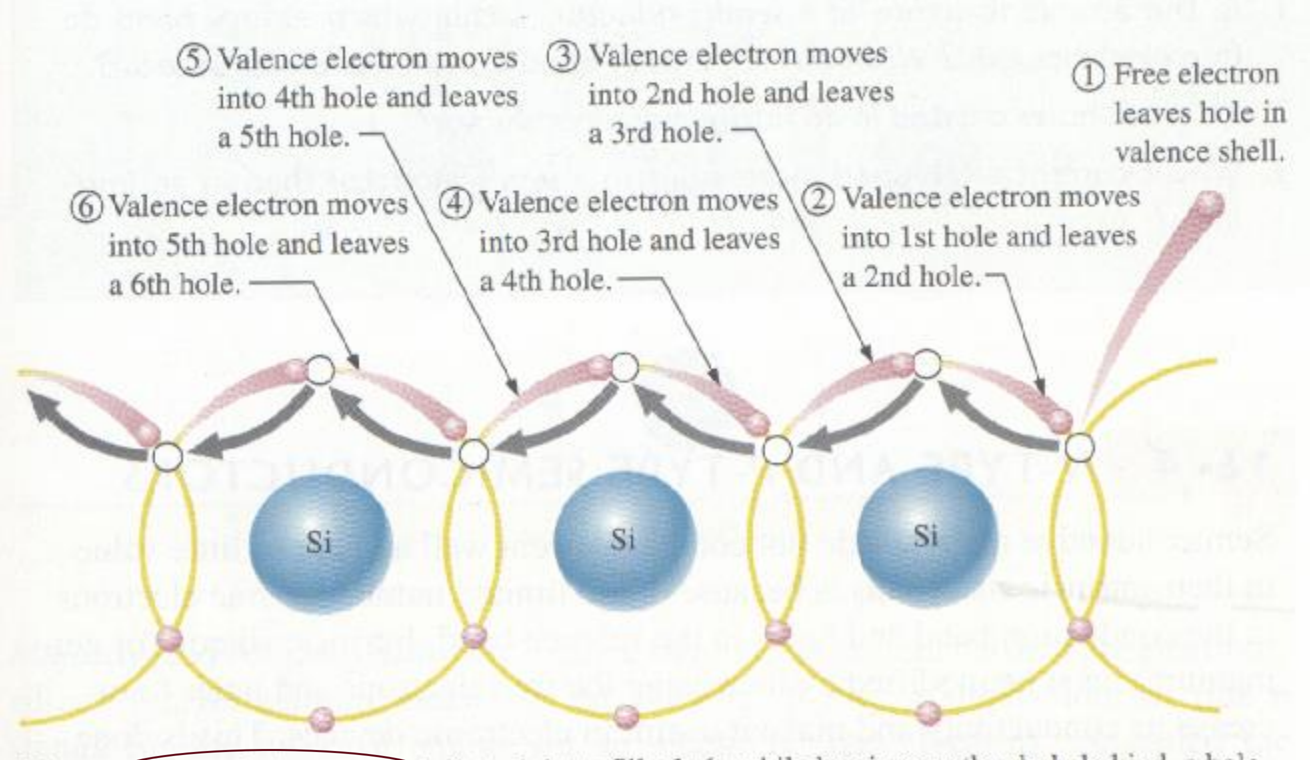
Intrinsic Semiconductors

*Apply a voltage across a piece of *Si:*

electron current

and hole current



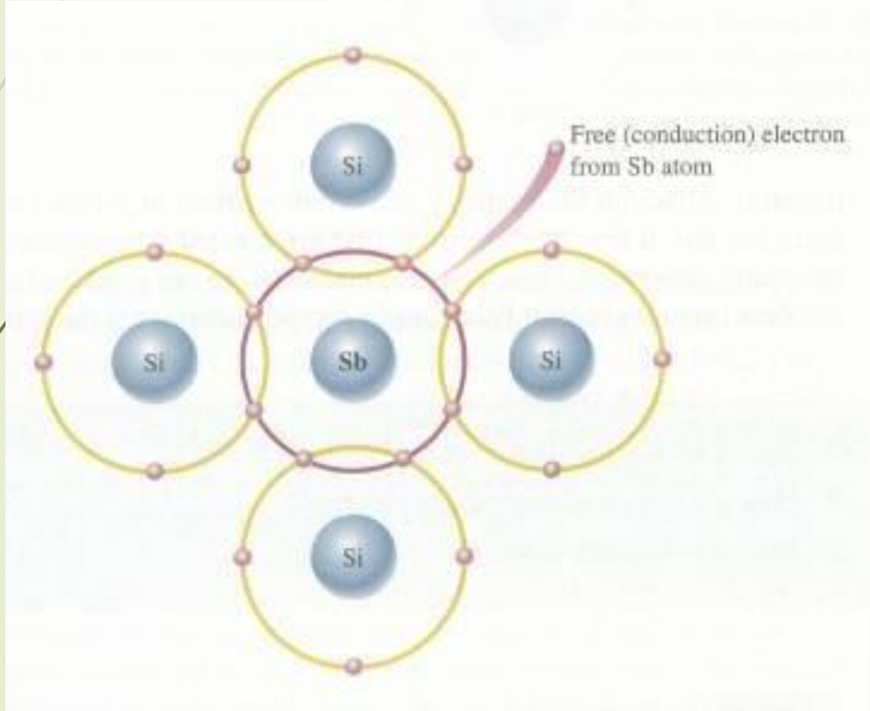


When a valence electron moves left to right to fill a hole while leaving another hole behind, a hole has effectively moved from right to left. Gray arrows indicate effective movement of a hole.

N- and P- Type Semiconductors

* *Doping*: adding of impurities (i.e., dopants) to the intrinsic semi-conductor material.

* *N-type*: adding Group V dopant (or donor) such as Phosphorus(P), Arsenic(As), Antimony(Sb),…

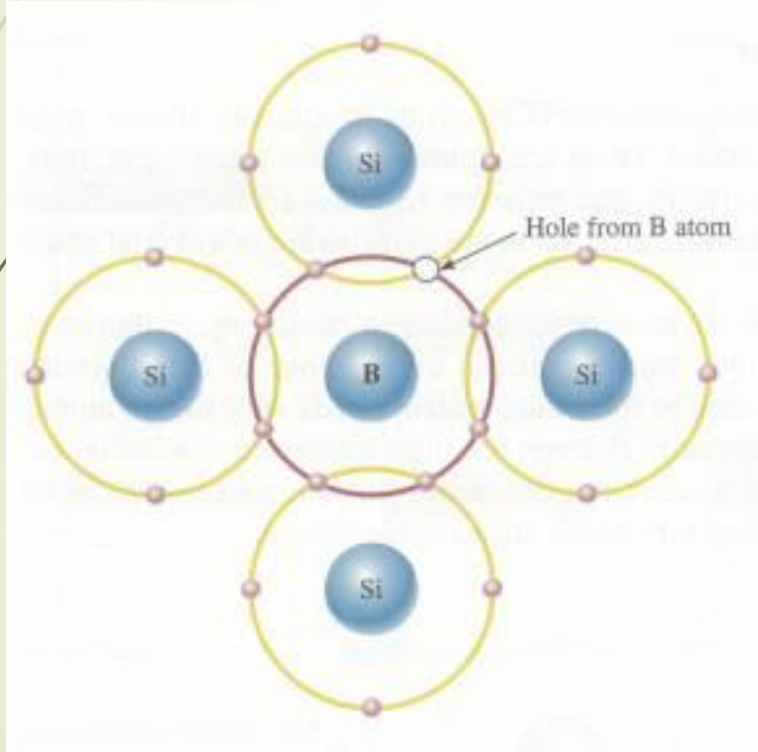


Electrons as majority charge carriers
Holes as minority charge carriers

N- and P- Type Semiconductors

* *Doping*: adding of impurities (i.e., dopants) to the intrinsic semi-conductor material.

* *P-type*: adding Group III dopant (or acceptor) such as Aluminum(Al), Boron(B), Gallium(Ga),…

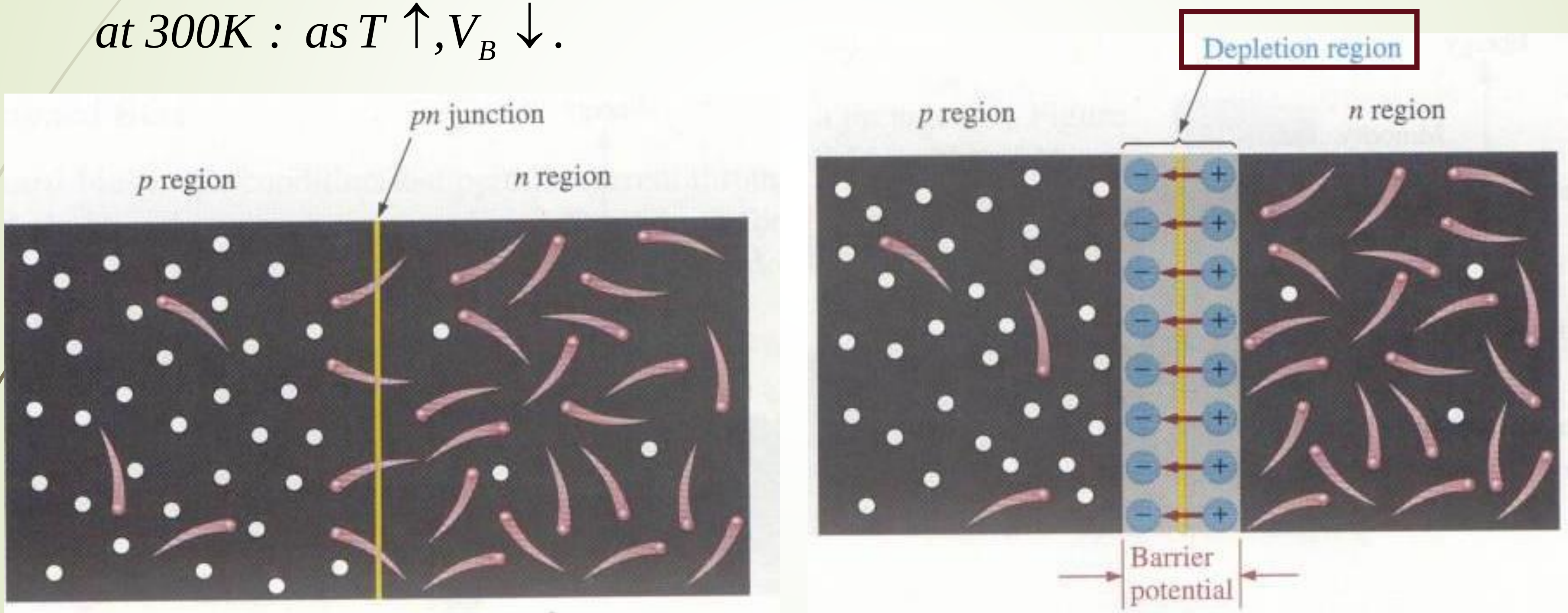


Holes as majority charge carriers
Electrons as minority charge carriers

The PN-Junction

* The interface in-between p-type and n-type material is called a *pn-junction*.

The barrier potential $V_B \cong 0.6 - 0.7V$ for Si and $0.3V$ for Ge at $300K$: as $T \uparrow, V_B \downarrow$.



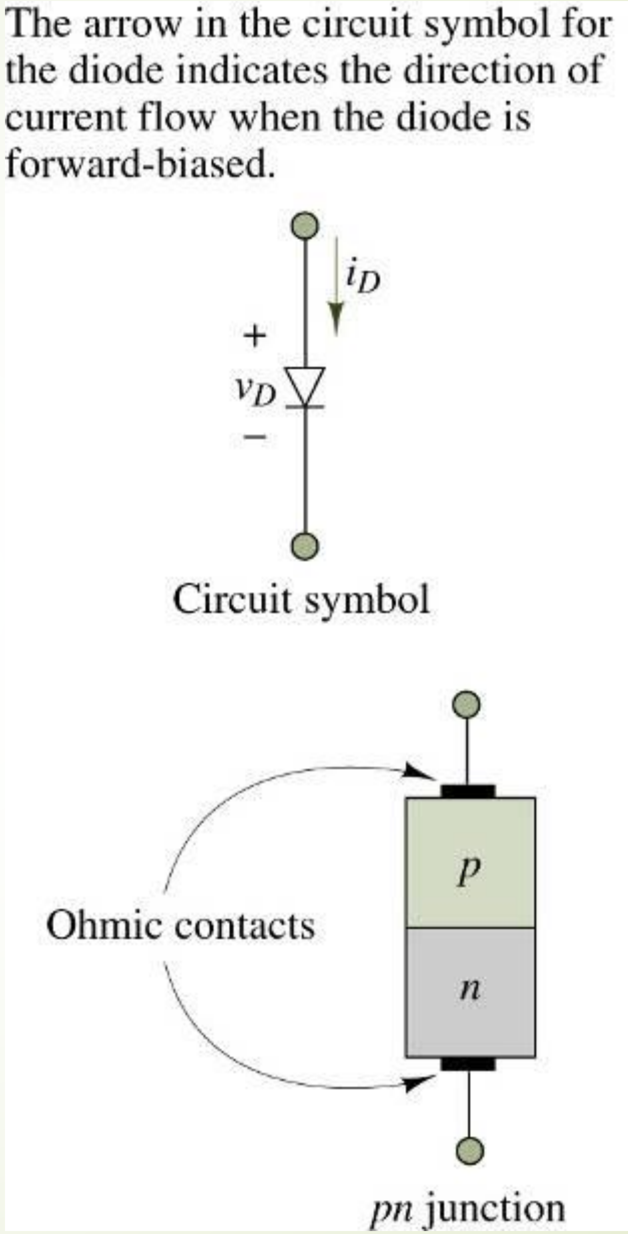
(a) At the instant of junction formation, free electrons in the *n* region near the *pn* junction begin to diffuse across the junction and fall into holes near the junction in the *p* region.

(b) For every electron that diffuses across the junction and combines with a hole, a positive charge is left in the *n* region and a negative charge is created in the *p* region, forming a barrier potential. This action continues until the voltage of the barrier repels further diffusion.

Biasing the PN-Junction

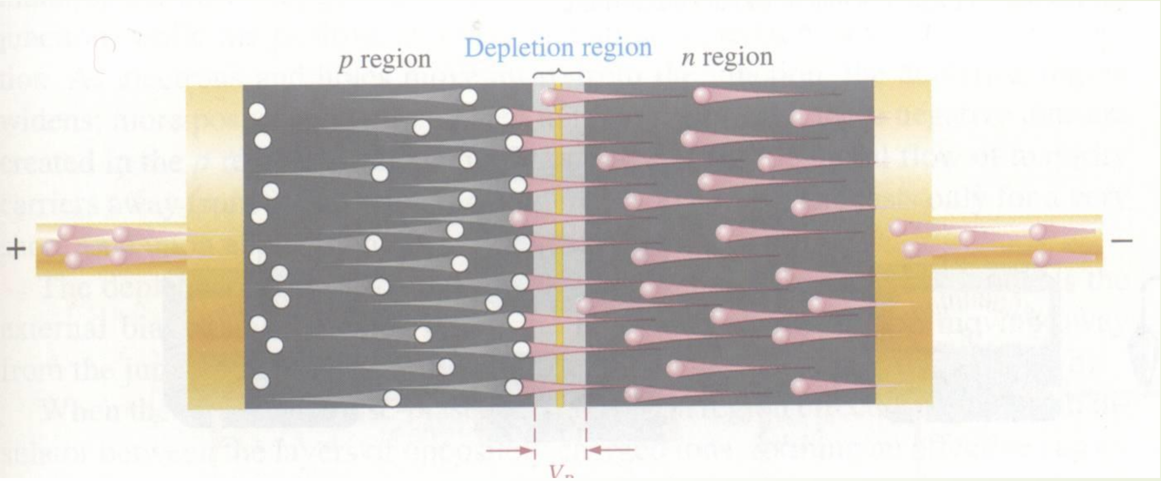
* There is no movement of charge through a PN-junction at equilibrium.

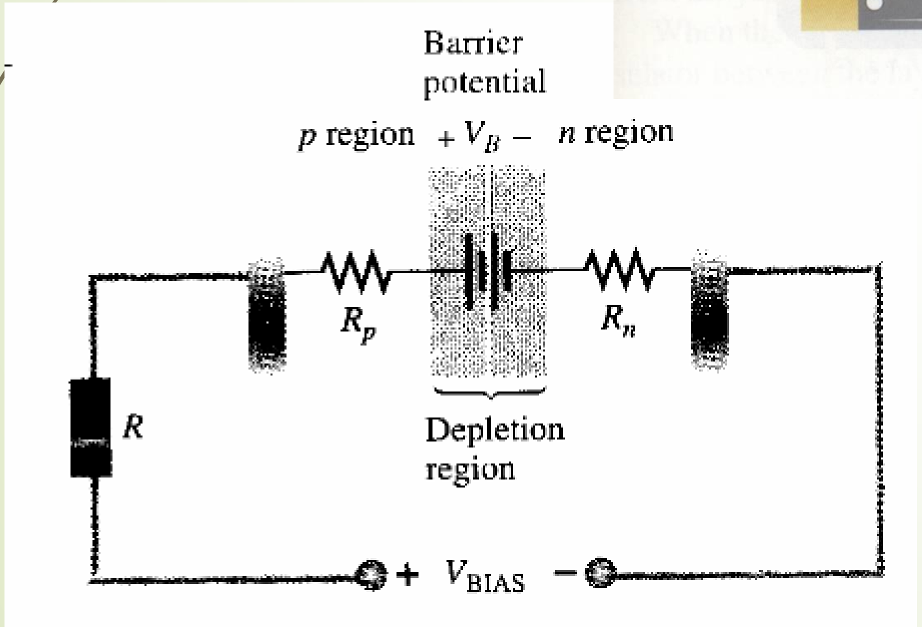
* The PN-junction form a *diode* which allows current in only one direction and prevent the current in the other direction as determined by the *bias*.

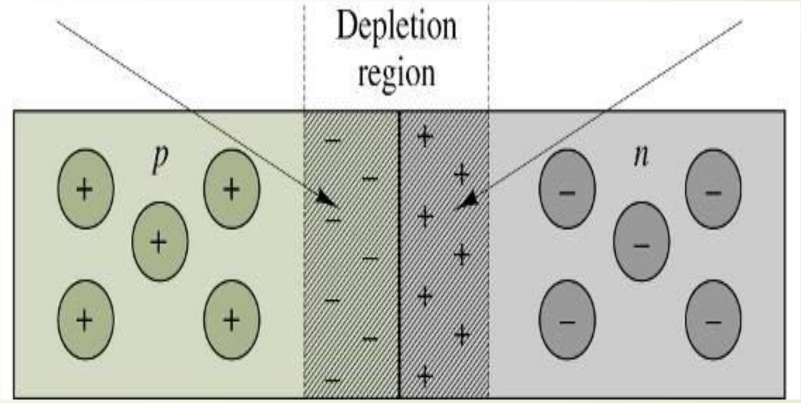


Biasing the PN-Junction

*__Forward Bias__: *dc voltage positive terminal connected to the p region and negative to the n region*. It is the condition that permits current through the pn-junction of a diode.

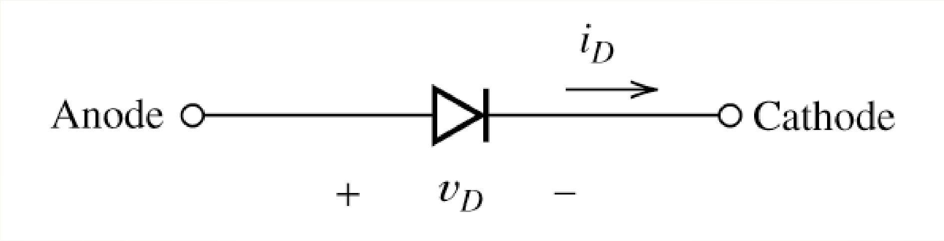


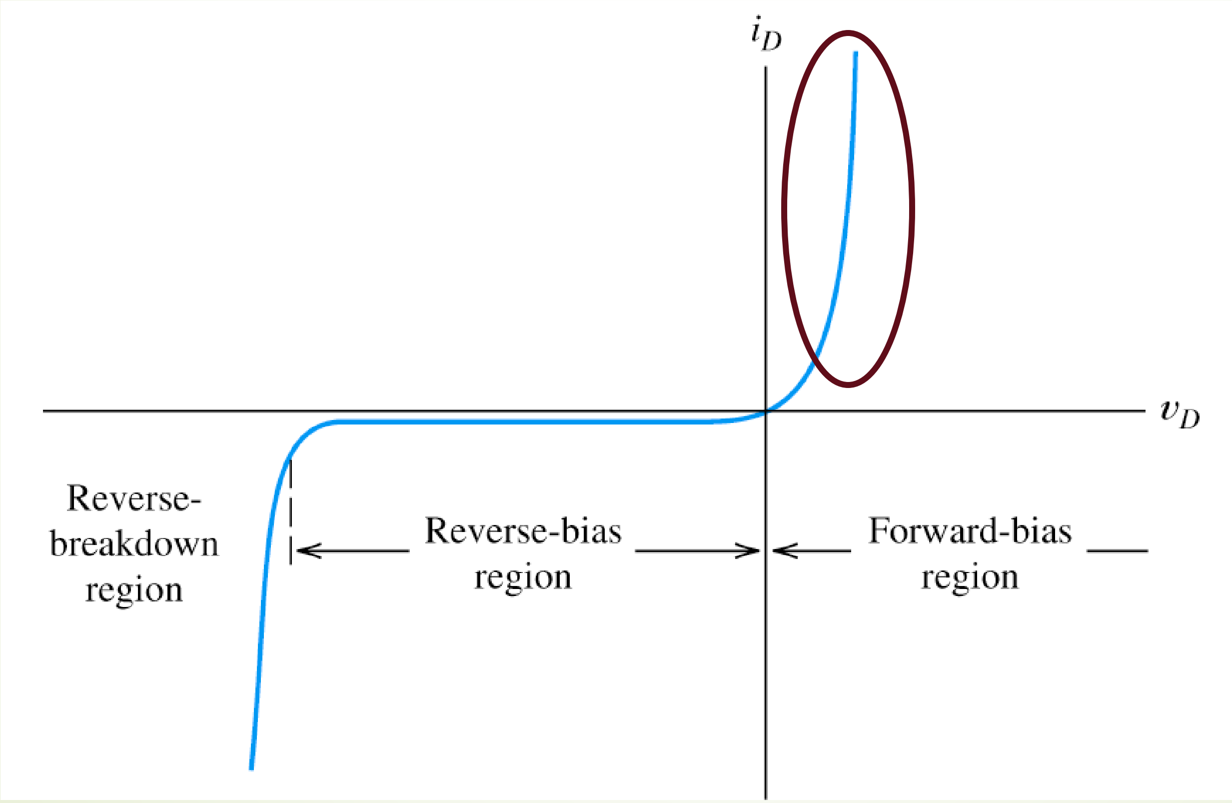




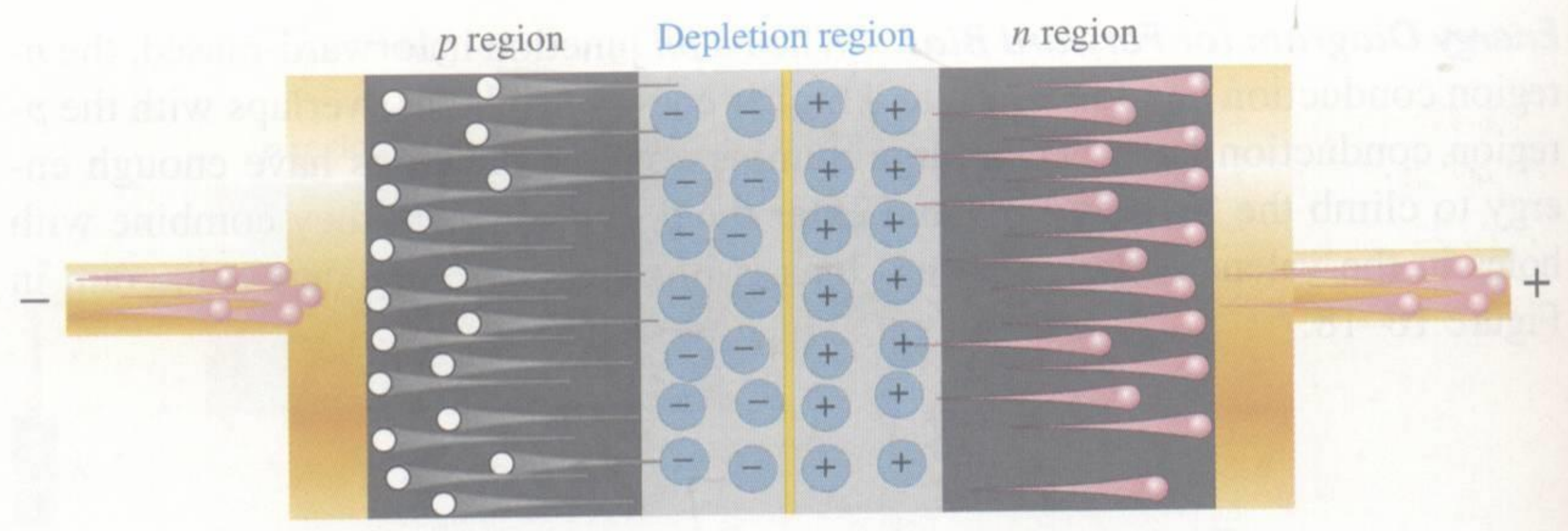
Biasing the PN-Junction

*****Forward Bias****:*





****Reverse Bias***: *dc voltage negative terminal connected to the p region and positive to the n region. Depletion region widens* until its potential difference equals the bias voltage, *majority-carrier current ceases*.

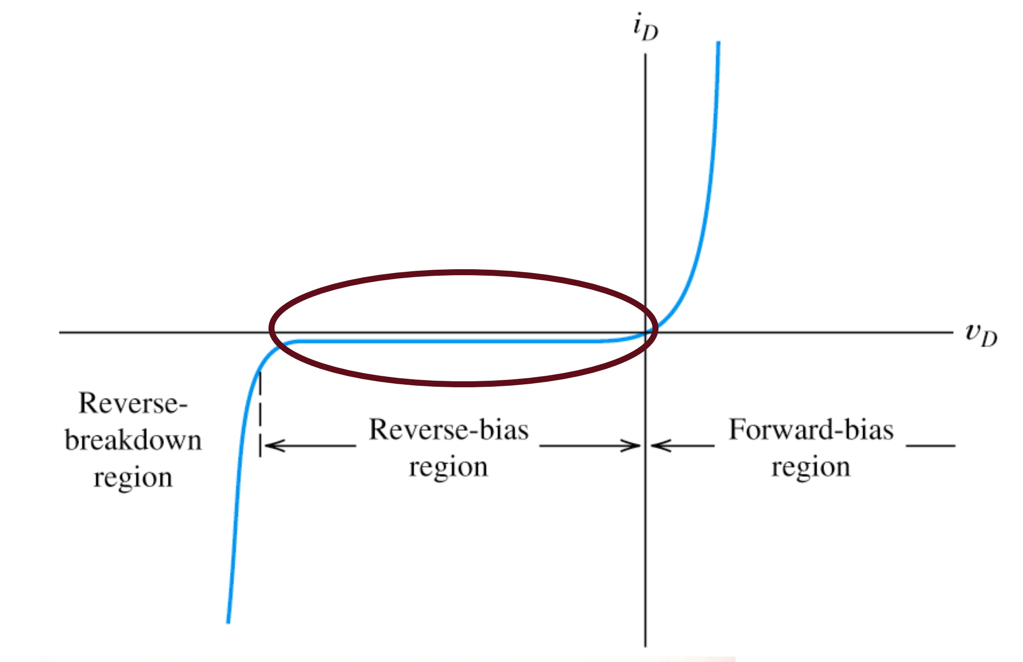


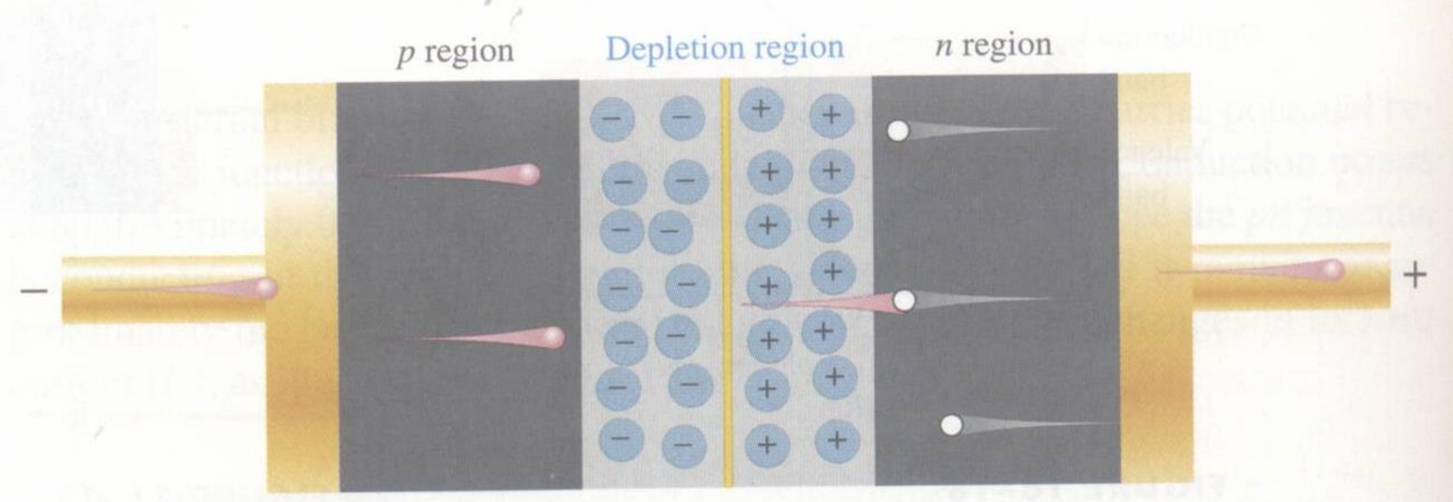
(a) There is transient current as depletion region widens.

***Reverse Bias**:

majority-carrier current ceases.

* However, there is still a very small current produced by minority carriers.



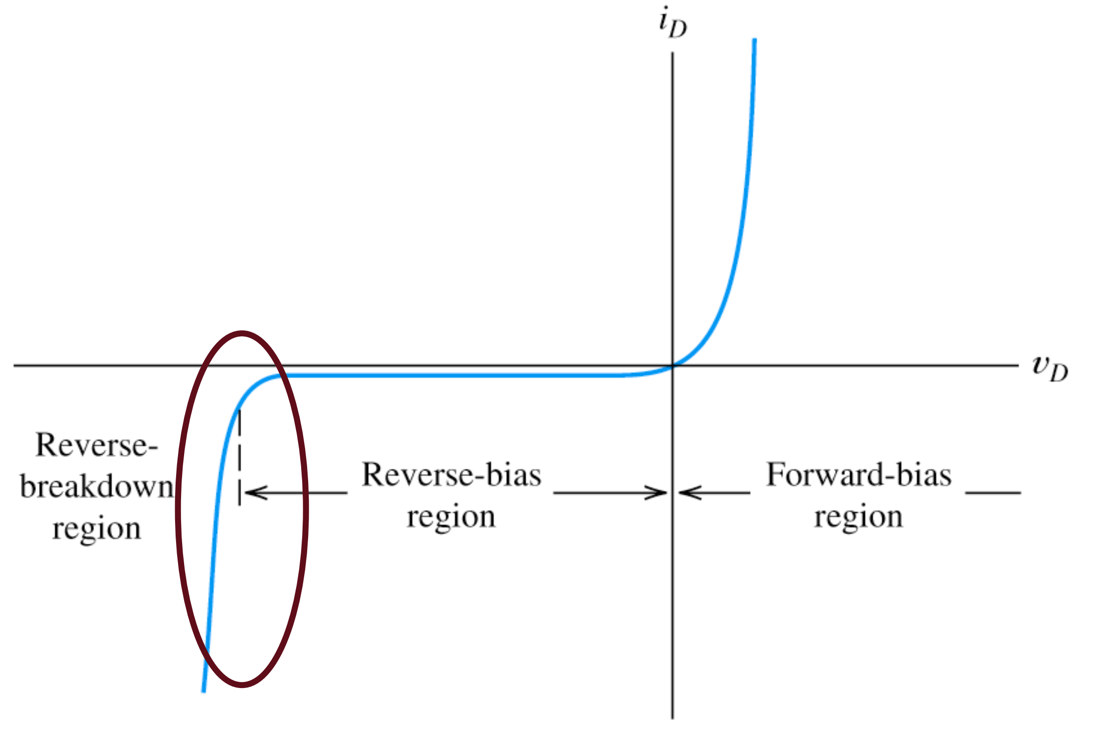


(b) Majority current ceases when barrier potential equals bias voltage. There is an extremely small reverse current due to minority carriers.

Biasing the PN-Junction

* **Reverse Breakdown:** As reverse voltage reach certain value, avalanche occurs and generates large current.

Diode Characteristic I-V Curve



(b) Volt–ampere characteristic

Shockley Equation

* The Shockley equation is a theoretical result under certain simplification:

$$\boxed{i_D = I_s\left[\exp\left(\frac{v_D}{nV_T}\right) - 1\right]}$$

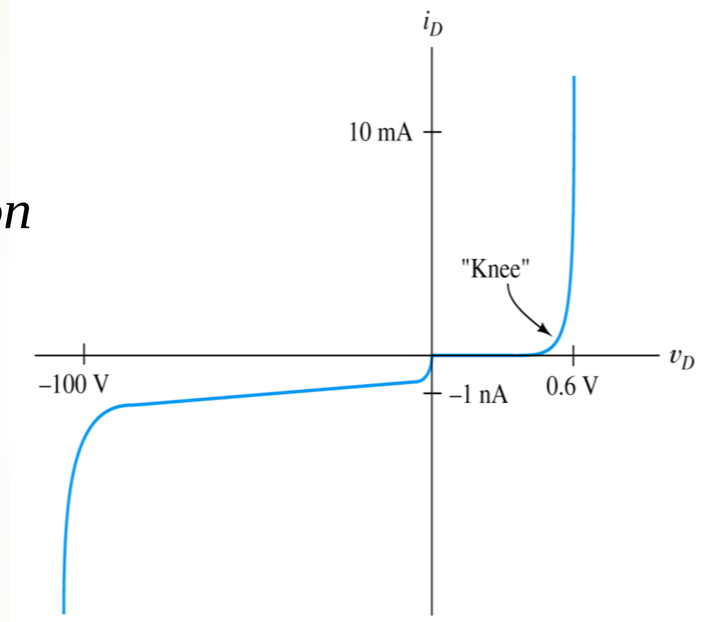
where $I_s \cong 10^{-14}$ A at 300K is the (reverse) saturation current, $n \cong 1$ to 2 is the emission coefficient,

$$V_T = \frac{kT}{q} \cong 0.026V \text{ at } 300K \text{ is the thermal voltage}$$

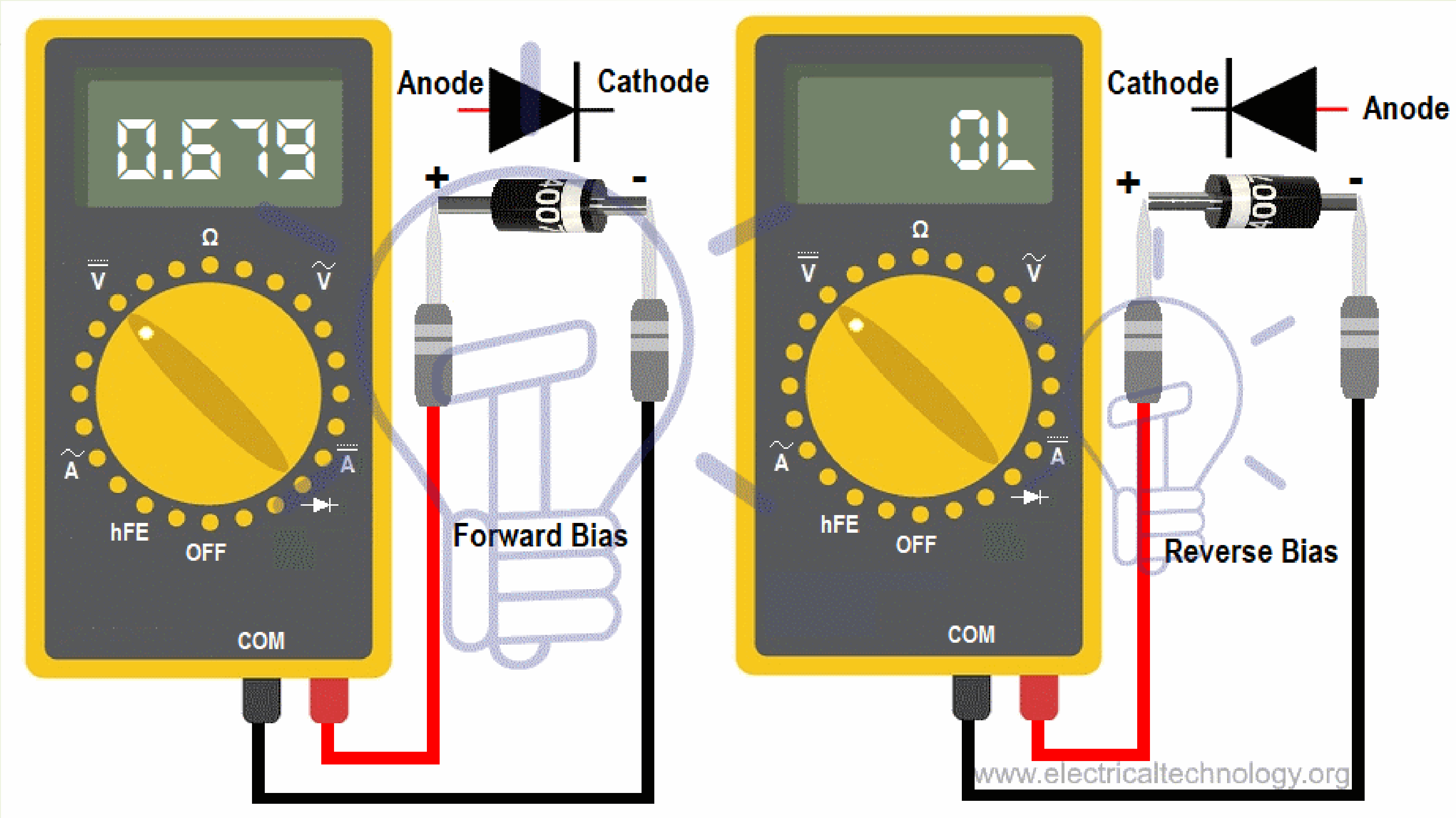
k is the Boltzman's constant, $q = 1.60 \times 10^{-19}$ C

when $\boxed{v_D \geq\approx 0.1V,\ i_D \cong I_s \exp\left(\frac{v_D}{nV_T}\right)}$

This equation is not applicable when $v_D < 0$



Diode Testing



Ideal-Diode Model

* We may apply "*Ideal-Diode Model*" to simplify the analysis:

(1) in forward direction: *short-circuit assumption*, zero voltage drop;

(2) in reverse direction: *open-circuit assumption*.

* The ideal-diode model can be used when the forward voltage drop and reverse currents are negligible.

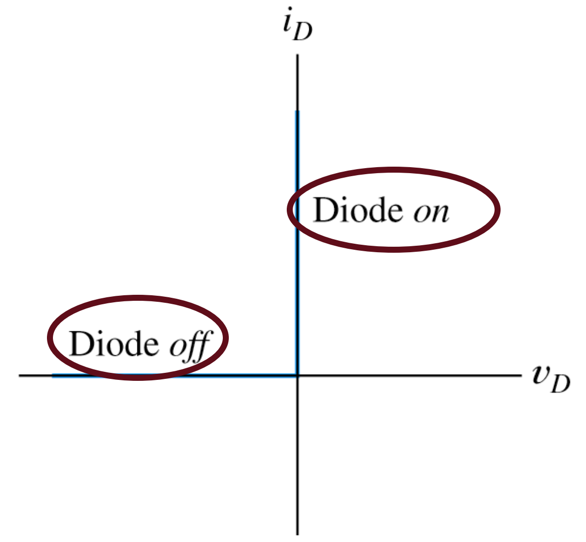


Figure 10.15 Ideal-diode volt–ampere characteristic.

Application

Rectifier Circuits

* Rectifiers convert ac power to dc power.

* Rectifiers form the basis for electronic power suppliers and battery charging circuits.

Half-Wave Rectifier

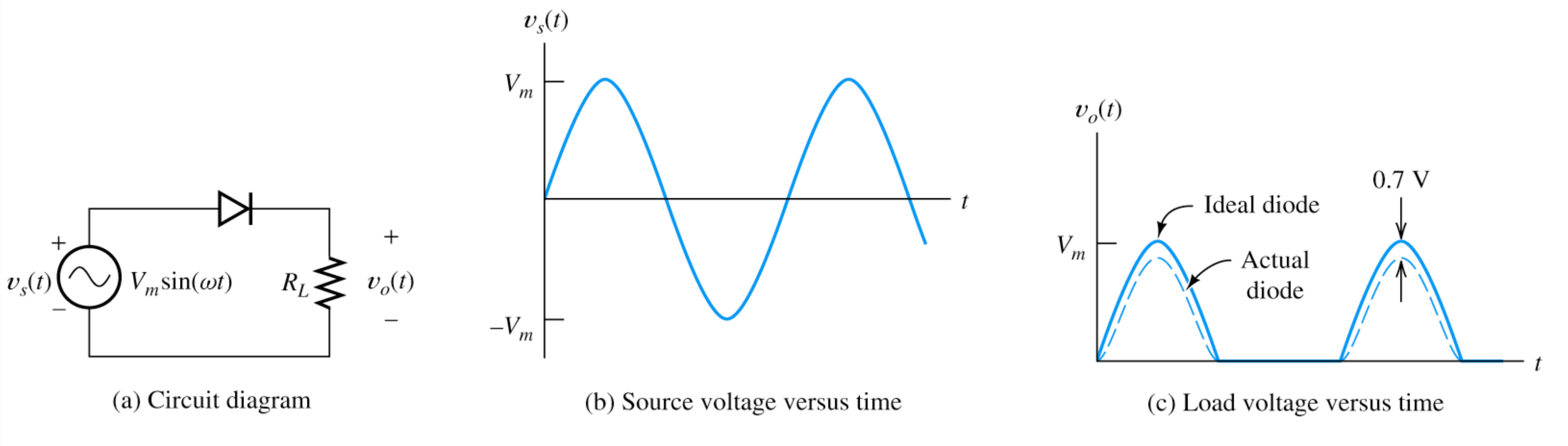
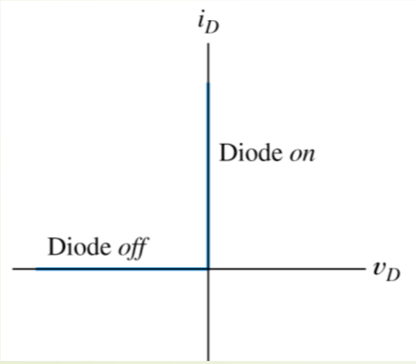
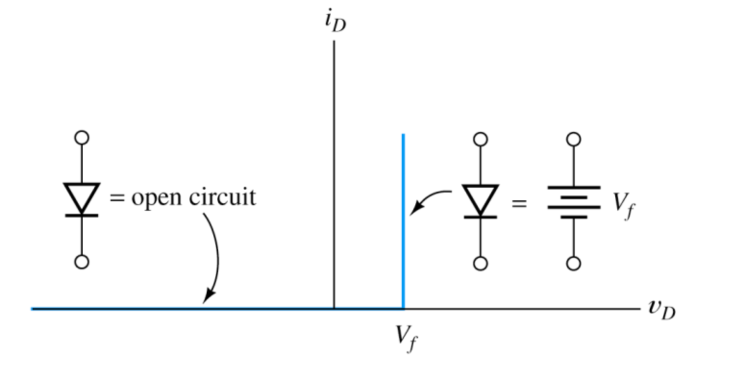


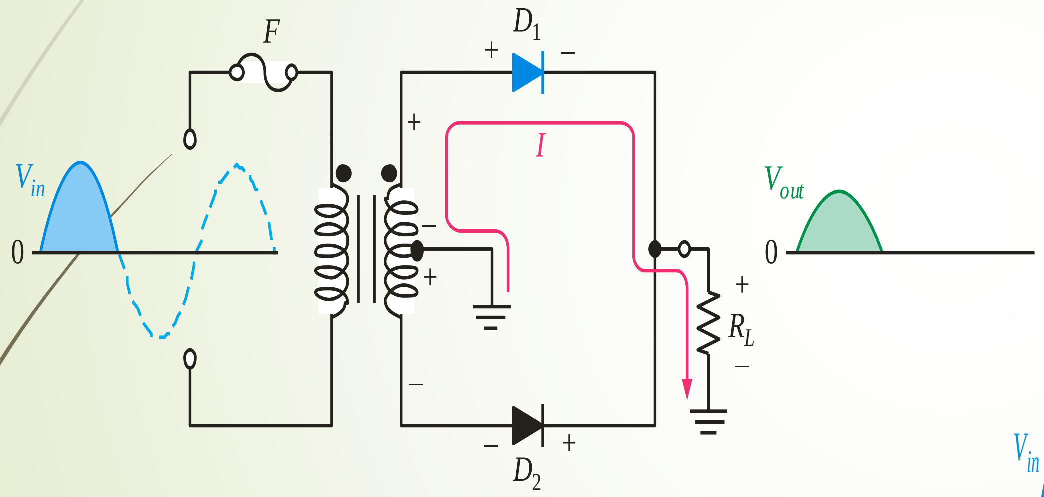
Figure 10.24 Half-wave rectifier with resistive load.





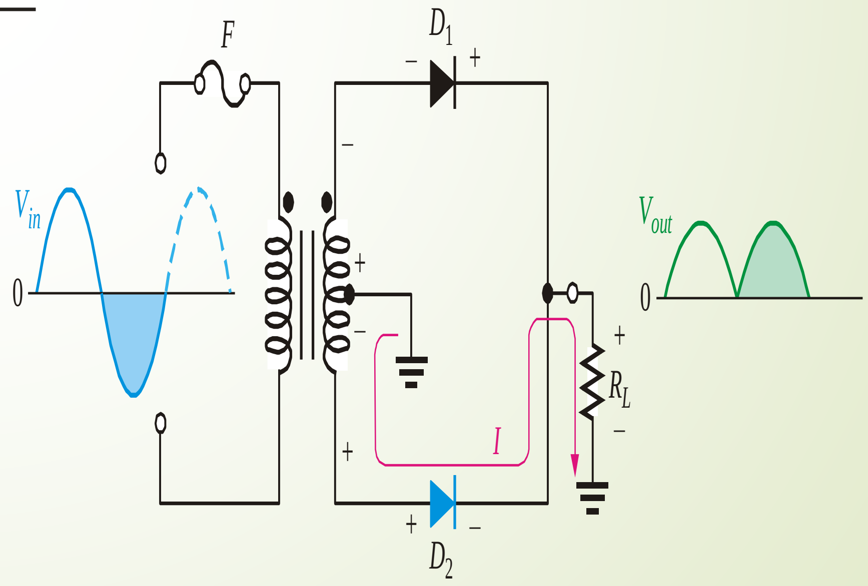
Center-Tapped Full wave rectifiers

- A center-tapped transformer is used with two diodes that conduct on alternating half-cycles.



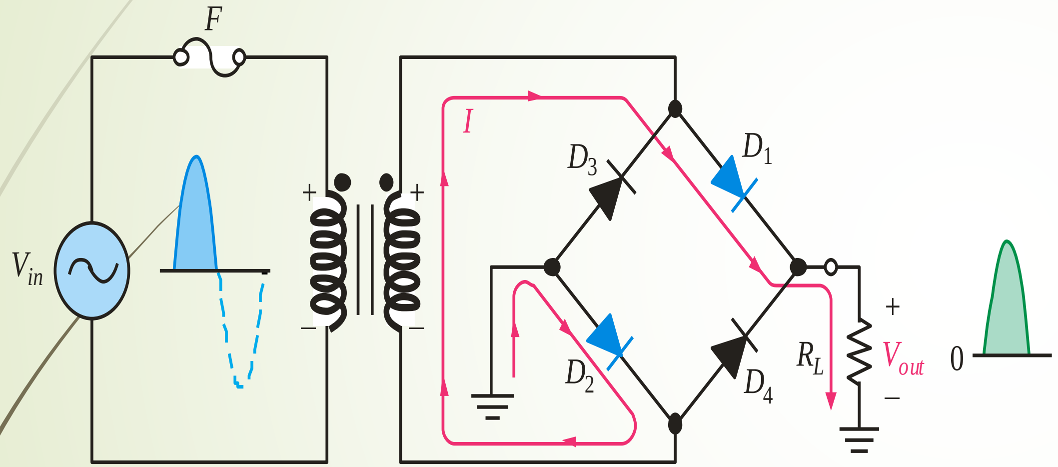
During the positive half-cycle, the upper diode is forward-biased and the lower diode is reverse-biased.

During the negative half-cycle, the lower diode is forward-biased and the upper diode is reverse-biased.



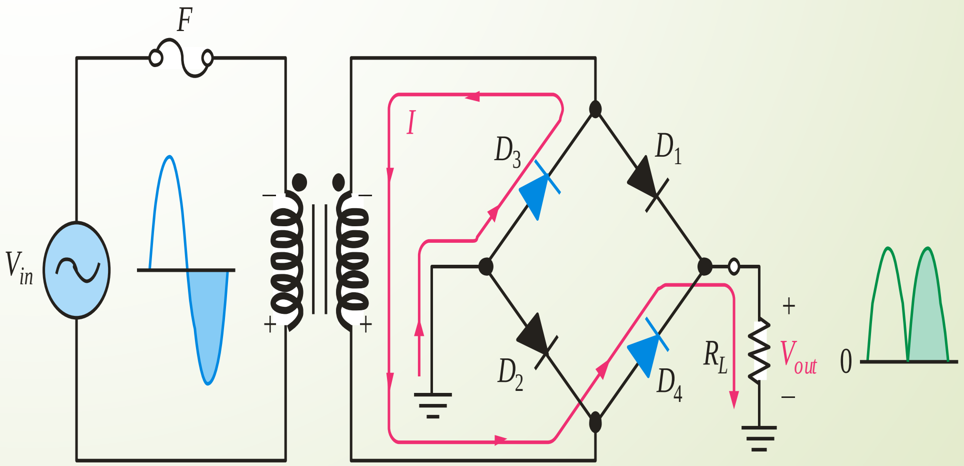
Bridge Full-wave rectifiers

- The Bridge Full-Wave rectifier uses four diodes connected across the entire secondary as shown.



Conduction path for the positive half-cycle.

Conduction path for the negative half-cycle.



MCQ

The forward voltage drop across a silicon diode is about …………………

(a) 0.3 V

(b) 3 V

(C) 7 V

(d) 0.7 V

MCQ

The forward voltage drop across a silicon diode is about …………………

(a) 0.3 V

(b) 3 V

(C) 7 V

(d) **0.7 V**

MCQ

The leakage current in a crystal diode is due to …………….

(a) minority carriers

(b) majority carriers

(C)junction capacitance

(d) none of the above

MCQ

The leakage current in a crystal diode is due to …………….

(a) minority carriers

(b) majority carriers

(C)junction capacitance

(d) none of the above

Unit-2

Bipolar Junction Transistor (BJT)

Introduction

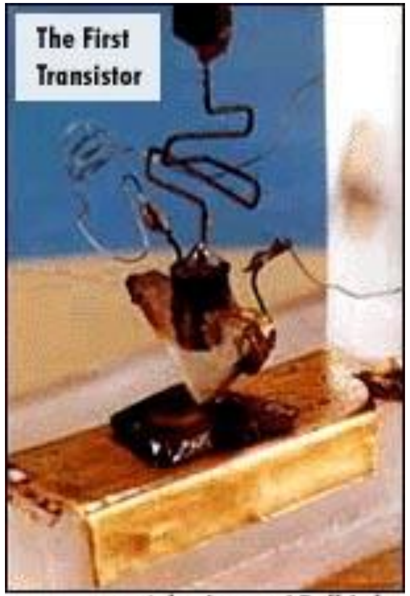
- Beside diodes, the most popular semiconductor devices is transistors. Eg: Bipolar Junction Transistor (BJT)
- If **cells are the building blocks of life**, **transistors are the building blocks of the digital revolution**.
- Transistors are more complex and can be used in many ways
- Most important feature:
  - can amplify signals (Gain)
  - Can act like a switch

Who Invented the Transistor?

John Bardeen, Walter Brattain, and William Shockley

- In the mid 1940's a team of scientists working for Bell Telephone Labs in Murray Hill, New Jersey, were working to discover a device to replace the then present vacuum tube technology.
- Vacuum tubes were the only technology available at the time to amplify signals or serve as switching devices in electronics. The problem was that they were **expensive, consumed a lot of power, gave off too much heat, and were unreliable**, causing a great deal of maintenance.


vacuum tube



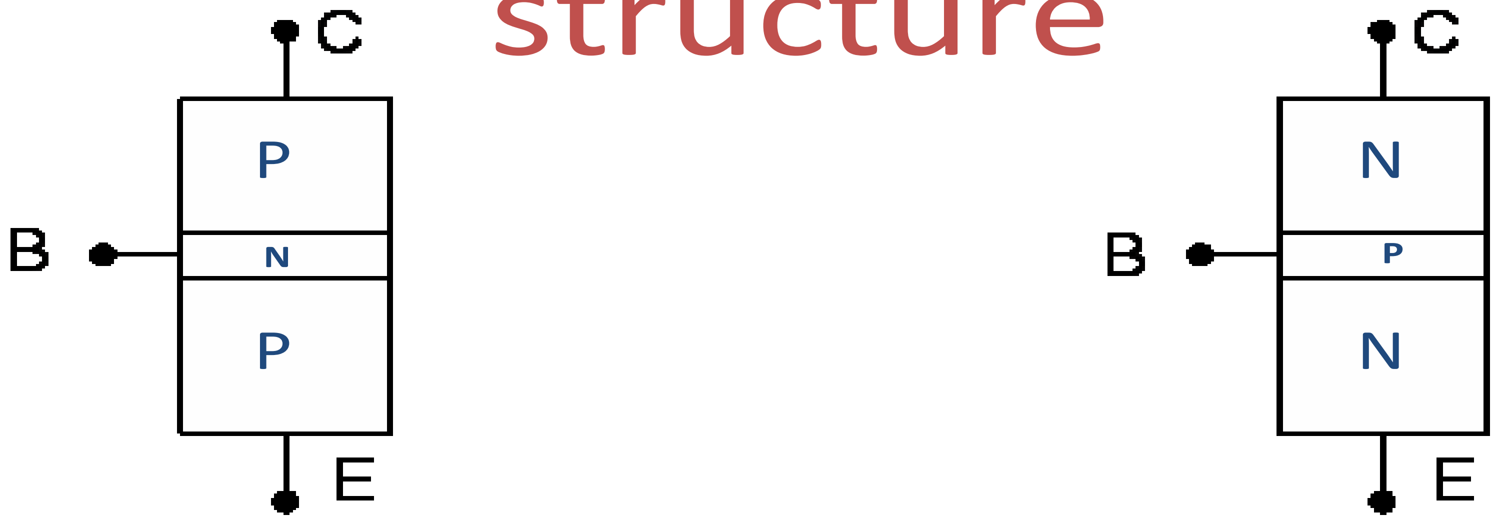
copyright: Lucent / Bell Labs

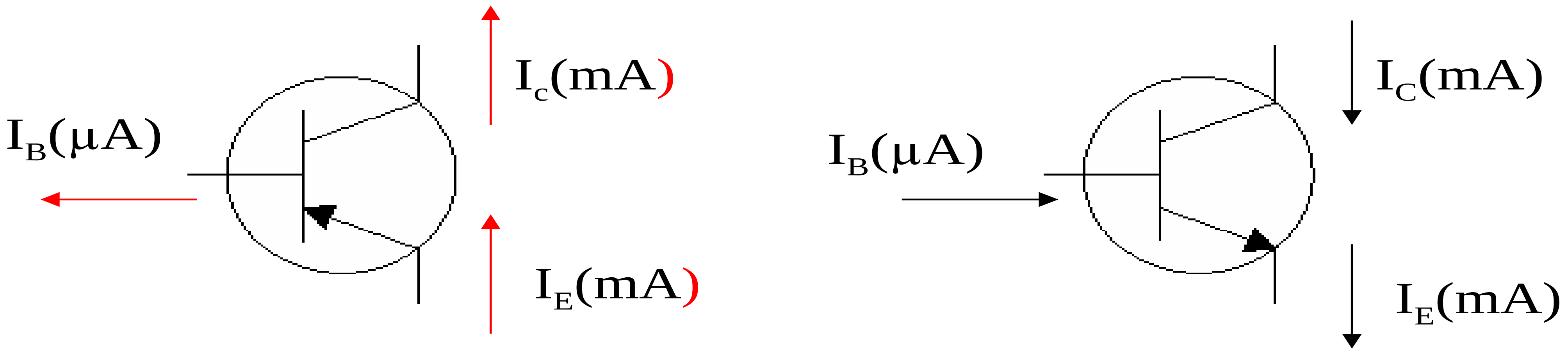

copyright: Lucent / Bell Labs

Transistor Structure

- Both holes (+) and electrons (-) will take part in the current flow – **Bipolar**
  - N – type regions contains free electrons(negative carriers)
  - P – type regions contains free holes (positive carriers)
- Two types of BJT
  - NPN transistor
  - PNP transistor
- The transistor regions are:
  - Emitter(E) – send the carriers into the base region and then on to the collector
  - Base(B) – acts as control region. It can allow none, some or many carriers to flow
  - Collector(C) – collects the carriers

PNP and NPN transistor structure

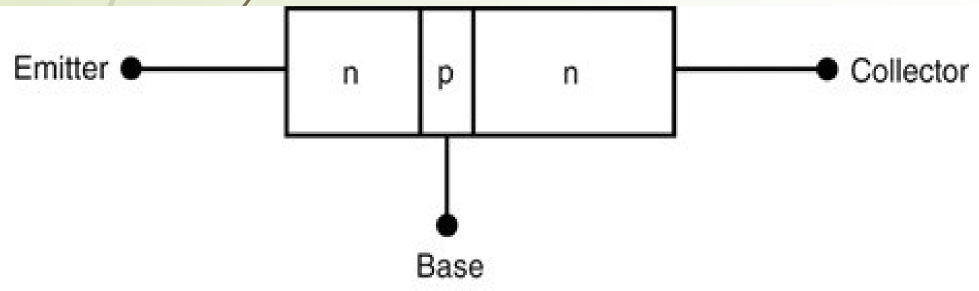




Arrow shows the current flows

Transistor Construction

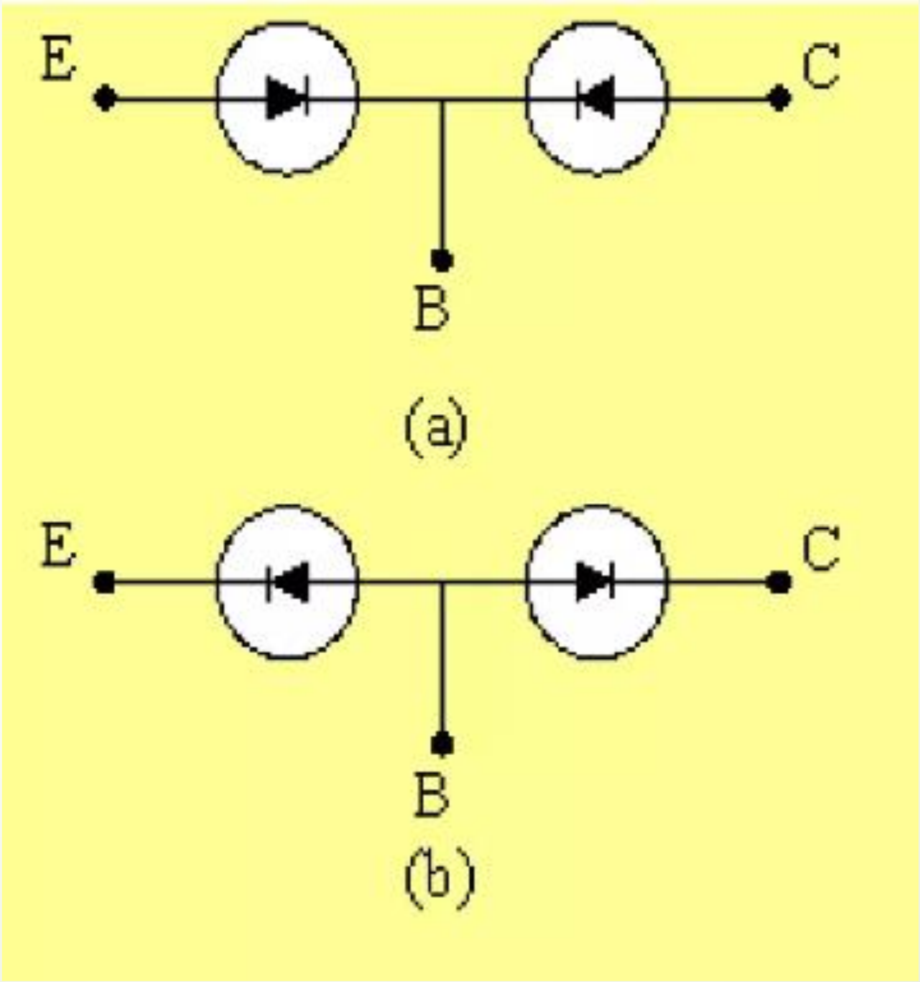
- Three doped regions (Emitter, Base and Collector)
- For both types (NPN and PNP), the base is a narrow region sandwiched between the larger collector and emitter regions



(*a*)

- Emitter region – **heavily doped**
  - and its job is to **emit carriers into the base**.
- Base region – is **very thin and lightly doped**
  - Most of the current carriers injected into the **base pass on to the collector.**
- Collector region – is **moderately doped**
  - is the **largest of all three regions**.

Back to Back Connected Diode

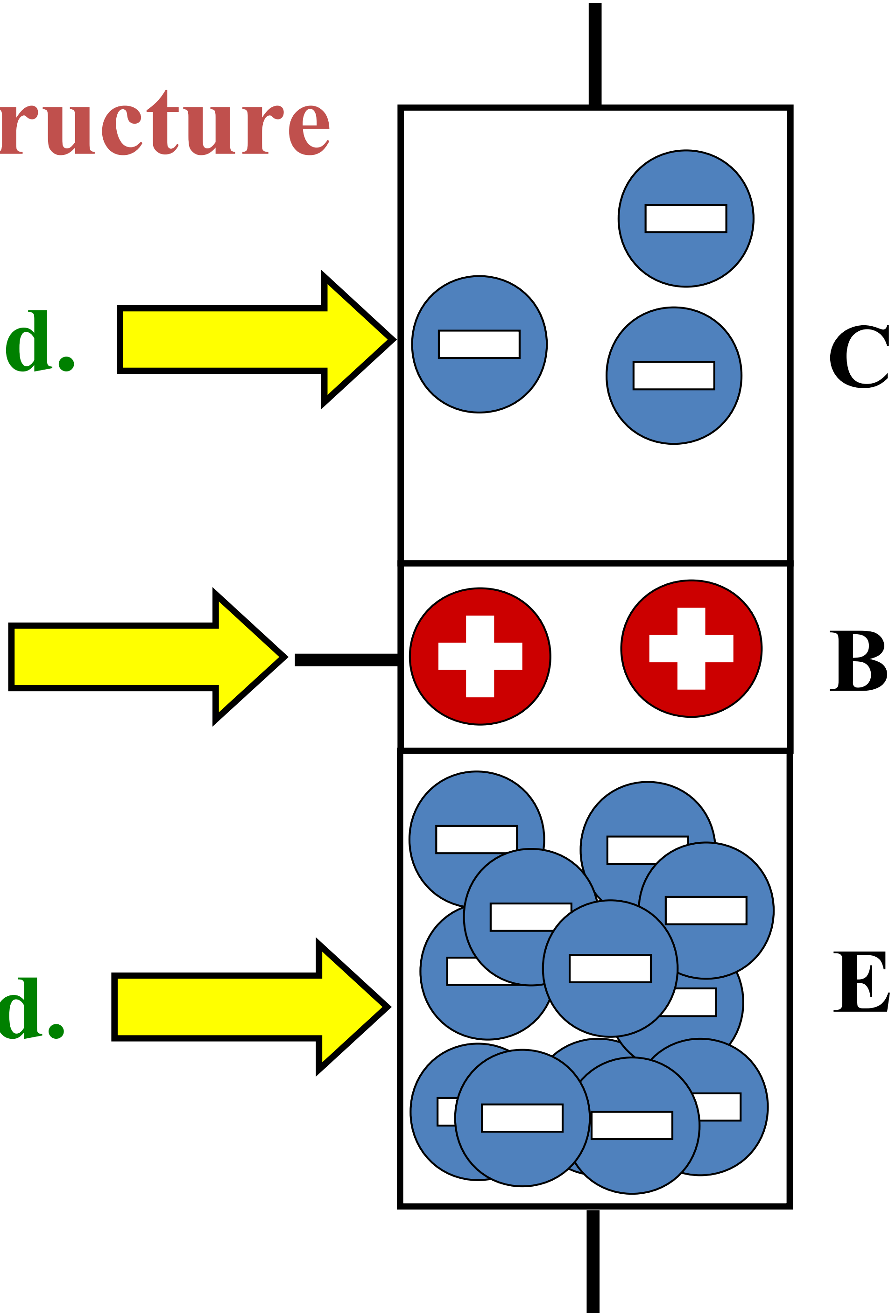


NPN Transistor Structure

The collector is lightly doped.

The base is thin and
is lightly doped.

The emitter is heavily doped.



Transistor Configuration

- **The way we connect the transistor to voltage source** – to get variety operation.

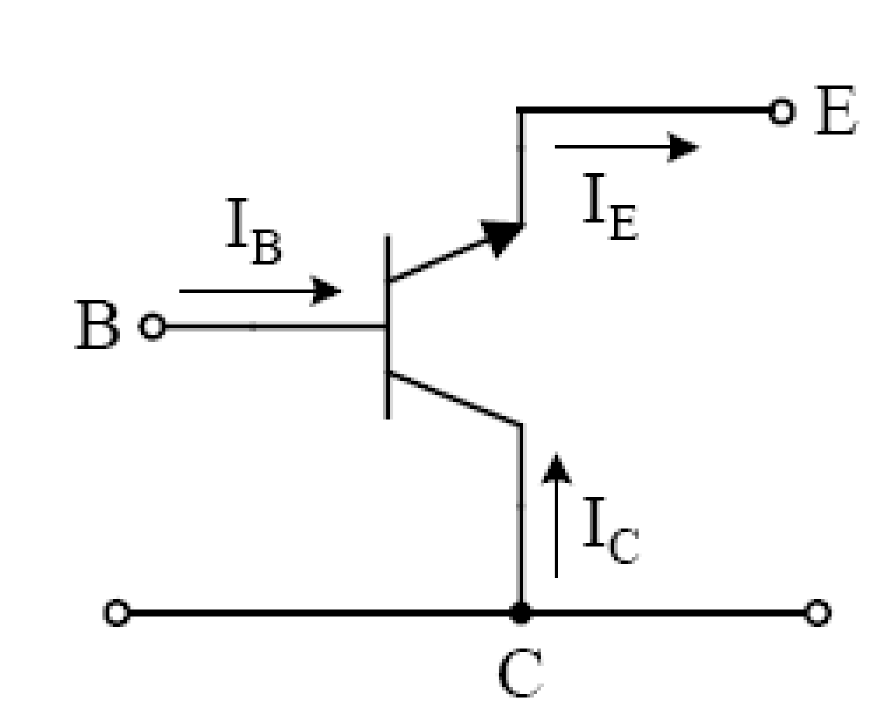
- Three types of configuration:
  - Common Collector
  - Common Base
  - Common Emitter

Common-Collector Configuration

- ***Collector terminal is common to the input and output of the circuit***

- The ***input signal*** is applied to the ***base terminal*** and the ***output*** is taken from the ***emitter terminal***

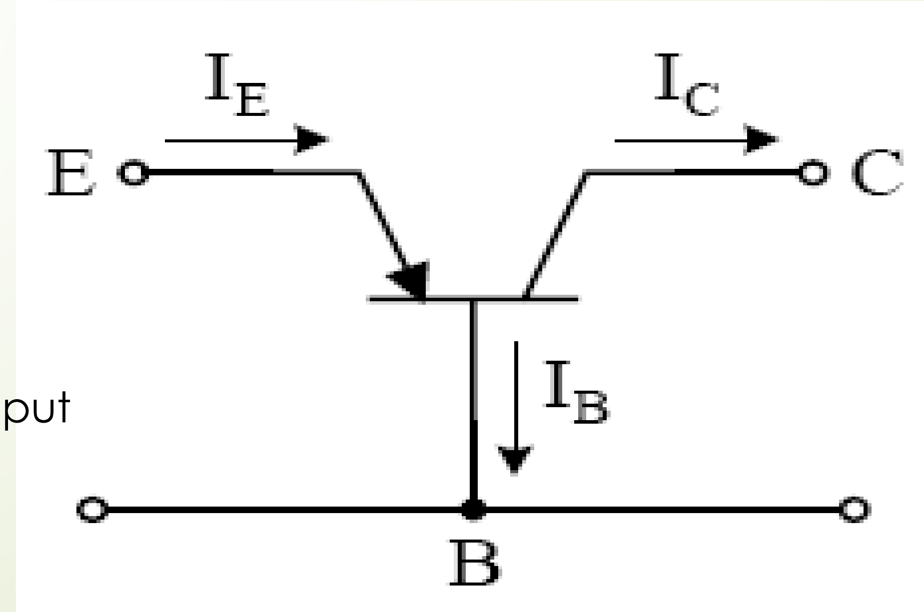
- Input – BC
- Output – EC



Common-Base Configuration

- ***Base terminal is a common point for input and output***
- The ***input signal*** is applied to the ***emitter terminal*** and the ***output*** is taken from the ***collector terminal***
- Input – EB
- Output – CB

Not applicable as an amplifier because the relation between input current gain (Ie) and output current gain (IC) is approximately 1



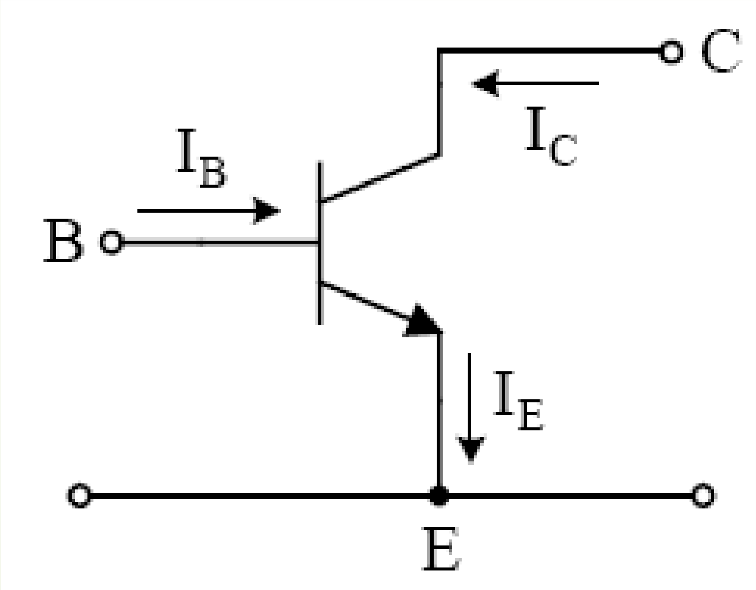
Common-Emitter Configuration

- ***Emitter terminal is common for input and output circuit***

- The ***input signal*** is applied to the ***base terminal*** and the ***output*** is taken from the ***collector terminal***

- Input – BE
- Output – CE

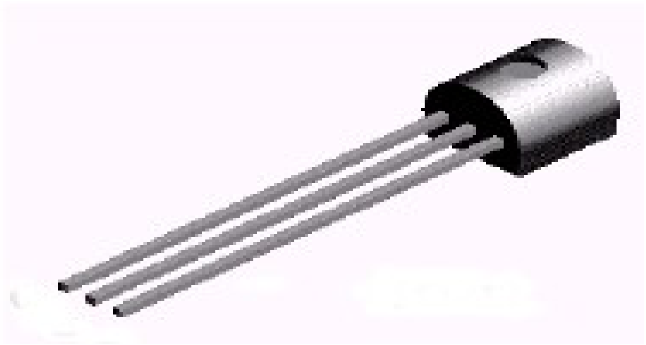
Mostly applied in practical amplifier circuits, since it provides good voltage, current and power gain

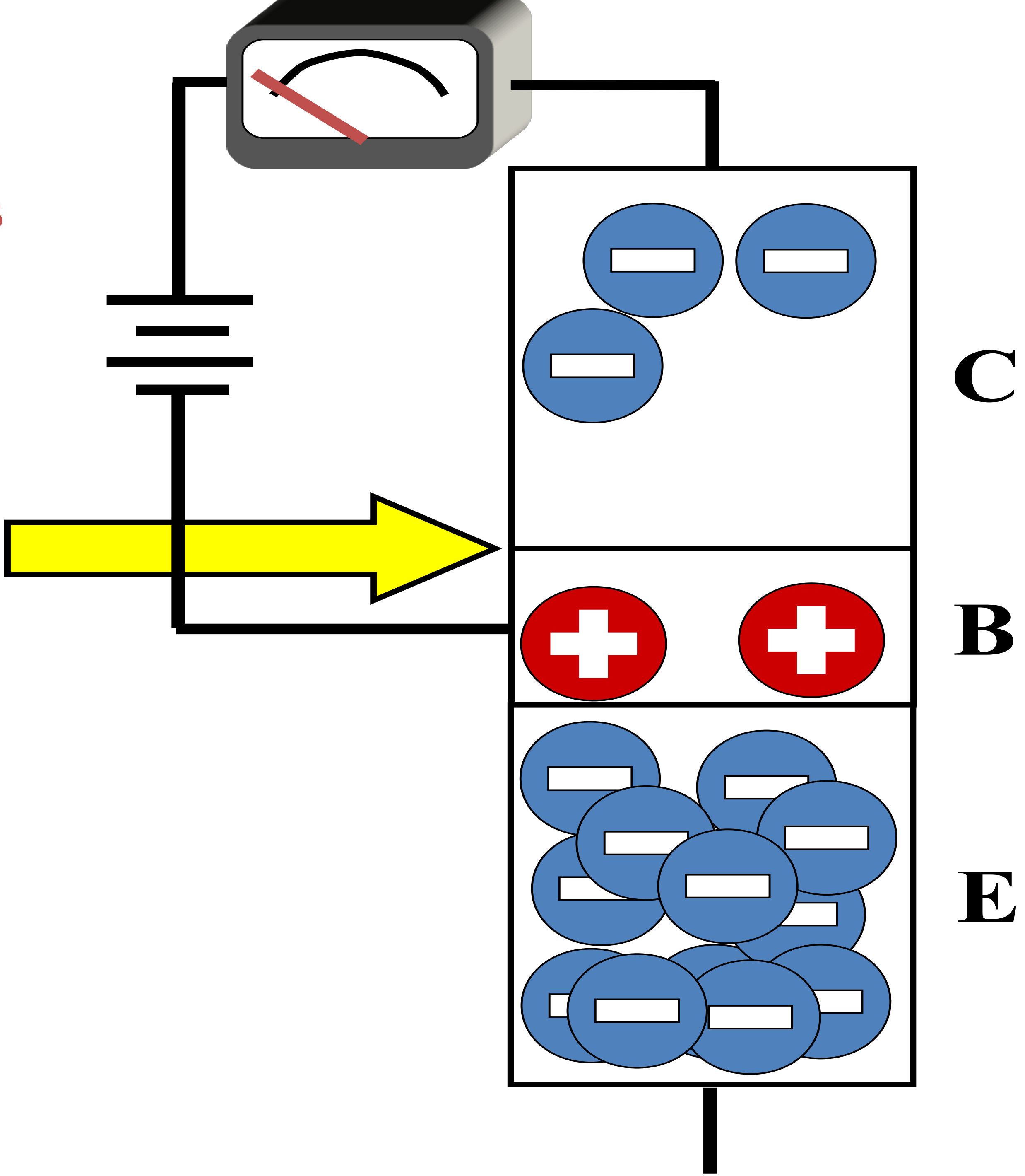


NPN Transistor Bias

No current flows.

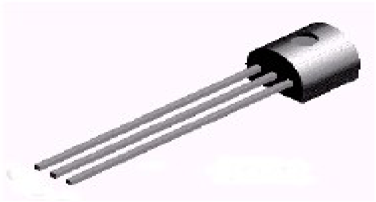
The C-B junction is reverse biased.



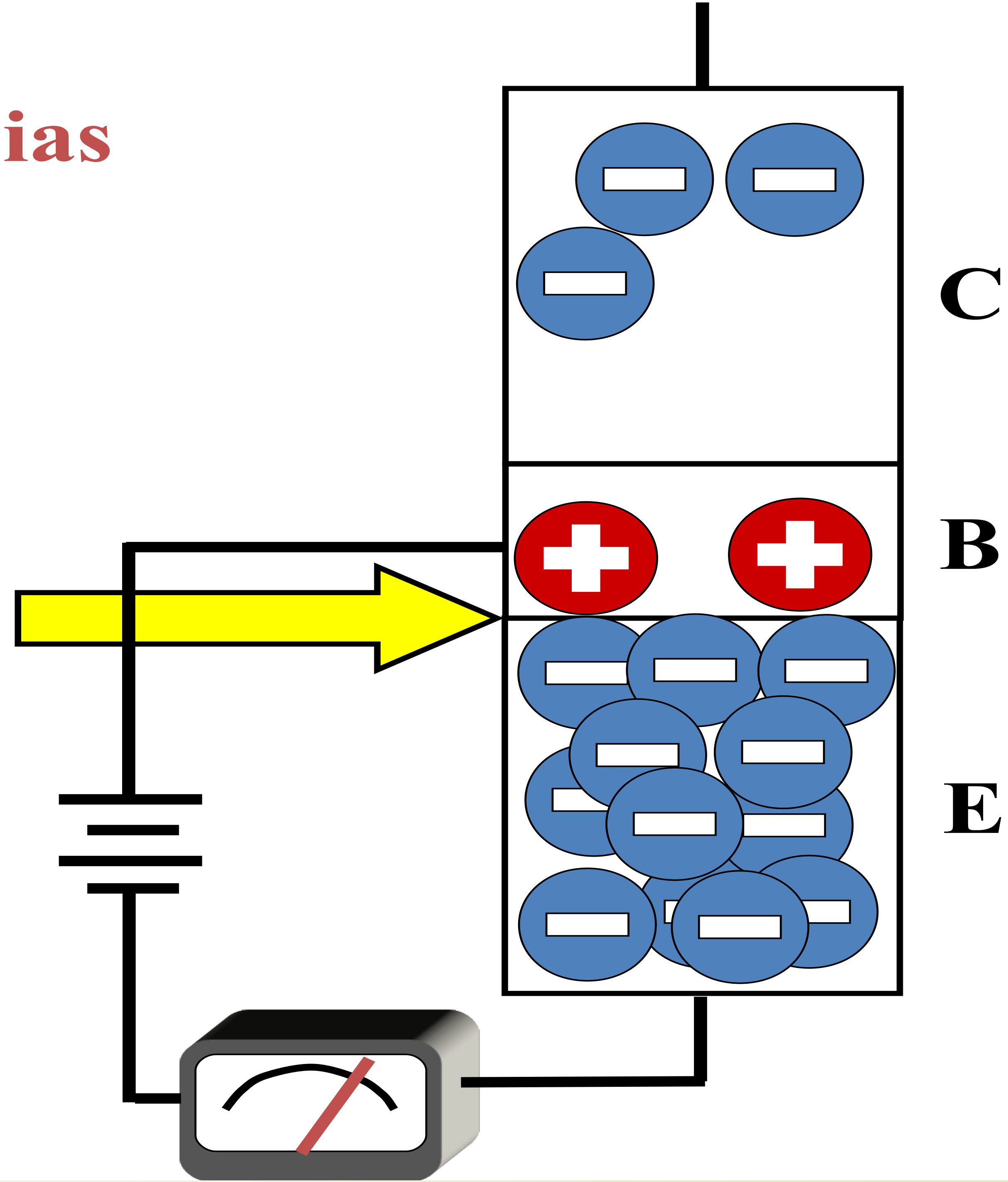


NPN Transistor Bias

The B-E junction is forward biased.



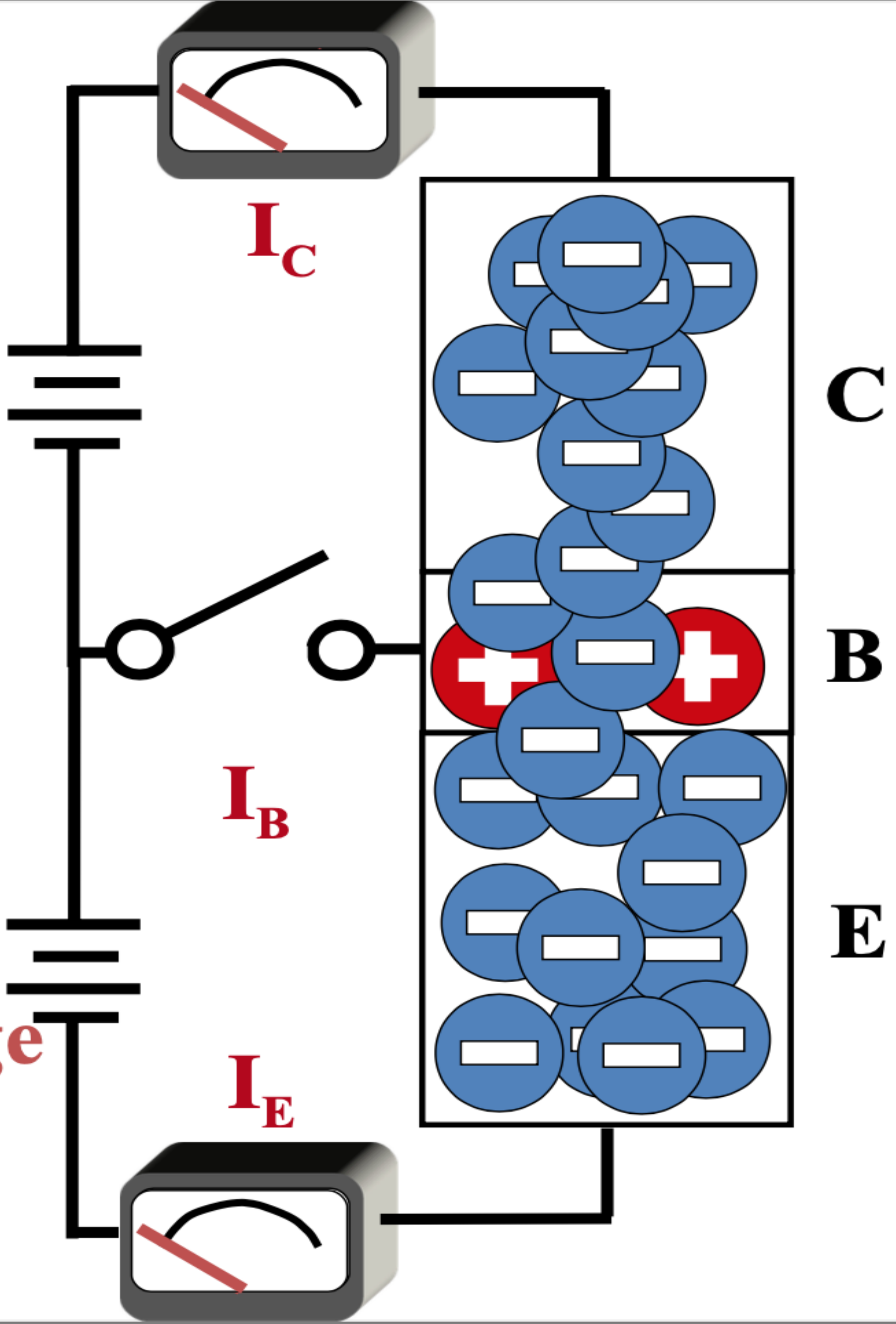
Current flows.



Note: when the switch opens, all currents go to zero.

Although I_B is smaller it controls I_E and I_C.

Gain is something small controlling something large (I_B is small).

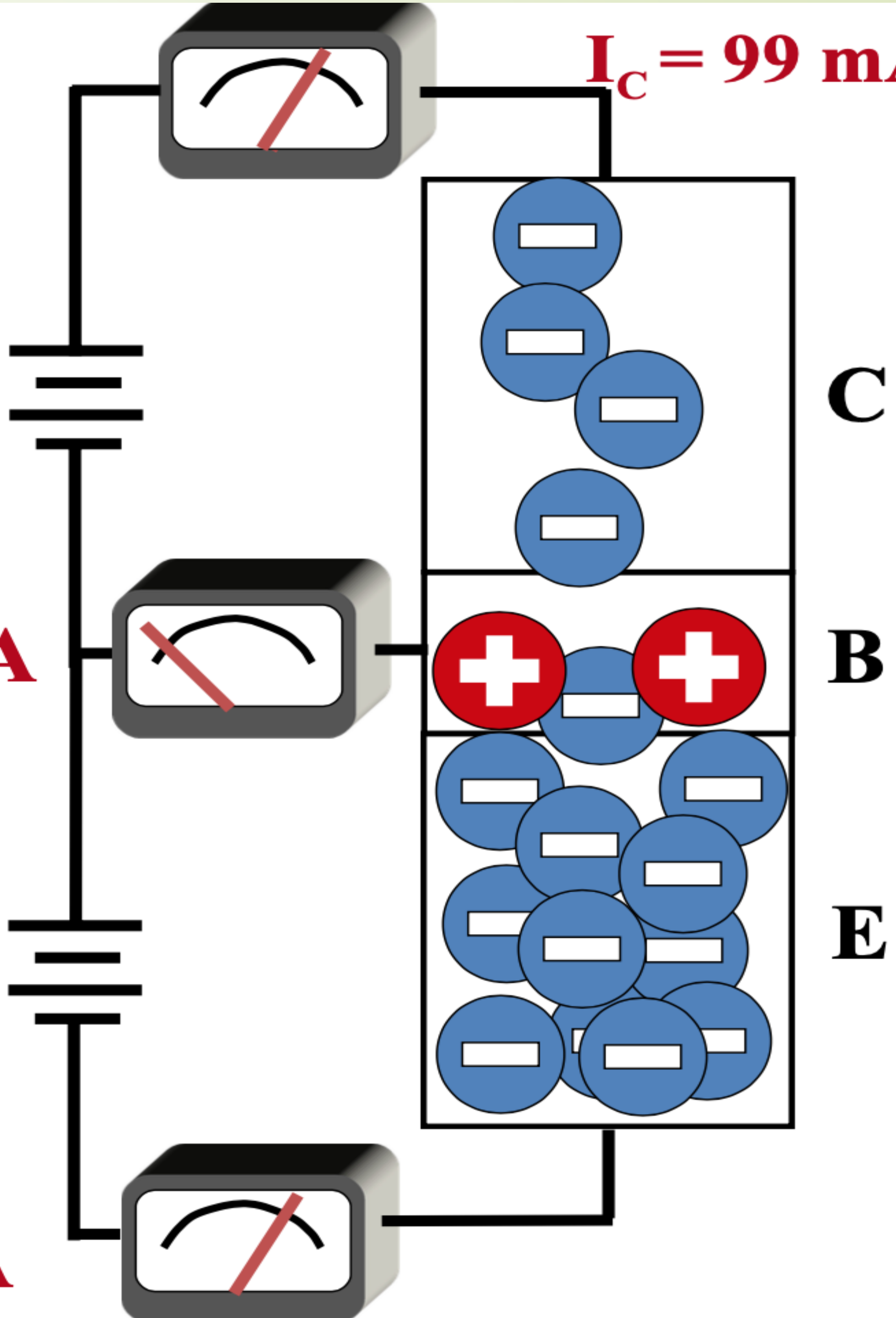


The current gain from base to collector is called β.

$I_C = 99$ mA

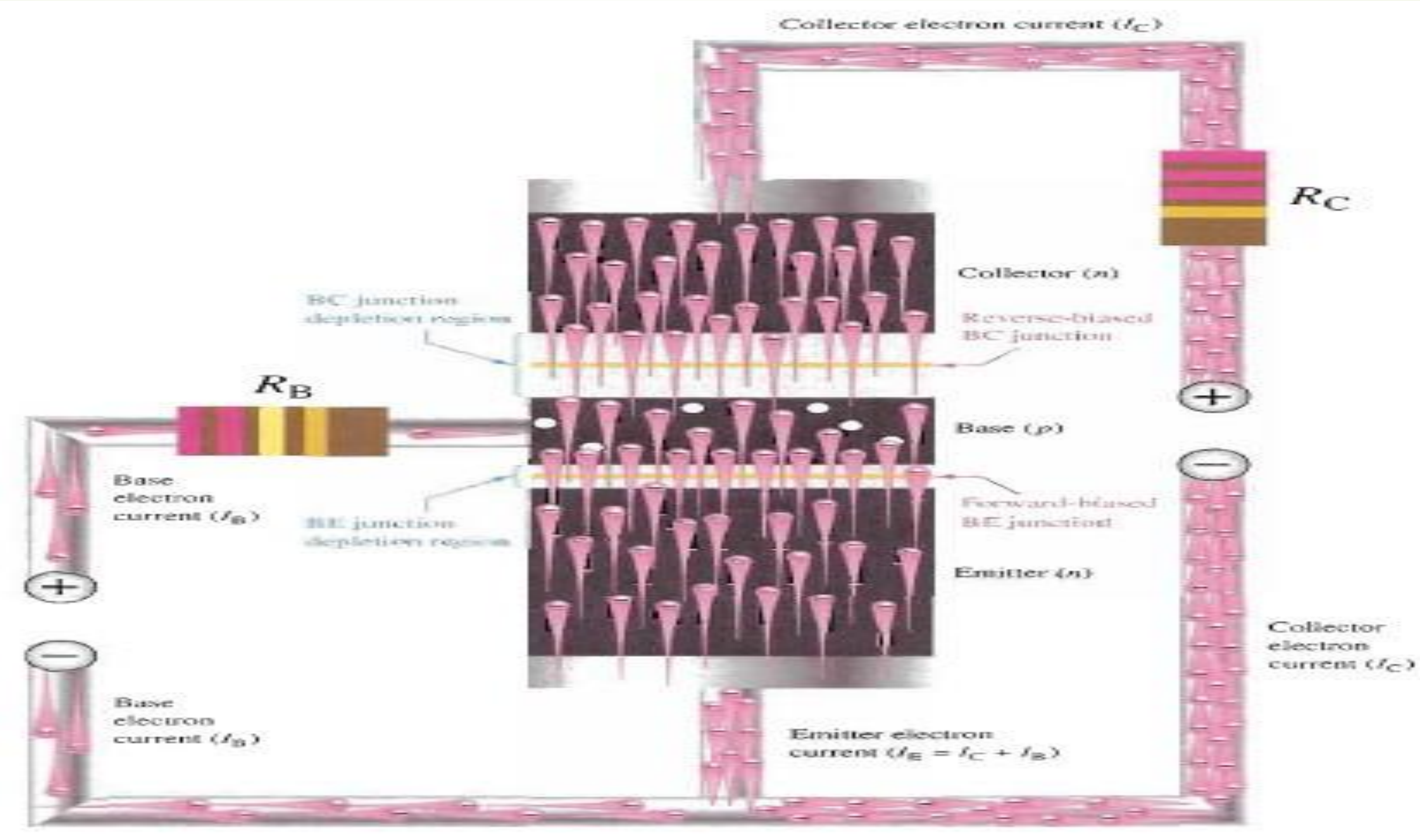
$I_B = 1$ mA

$I_E = 100$ mA

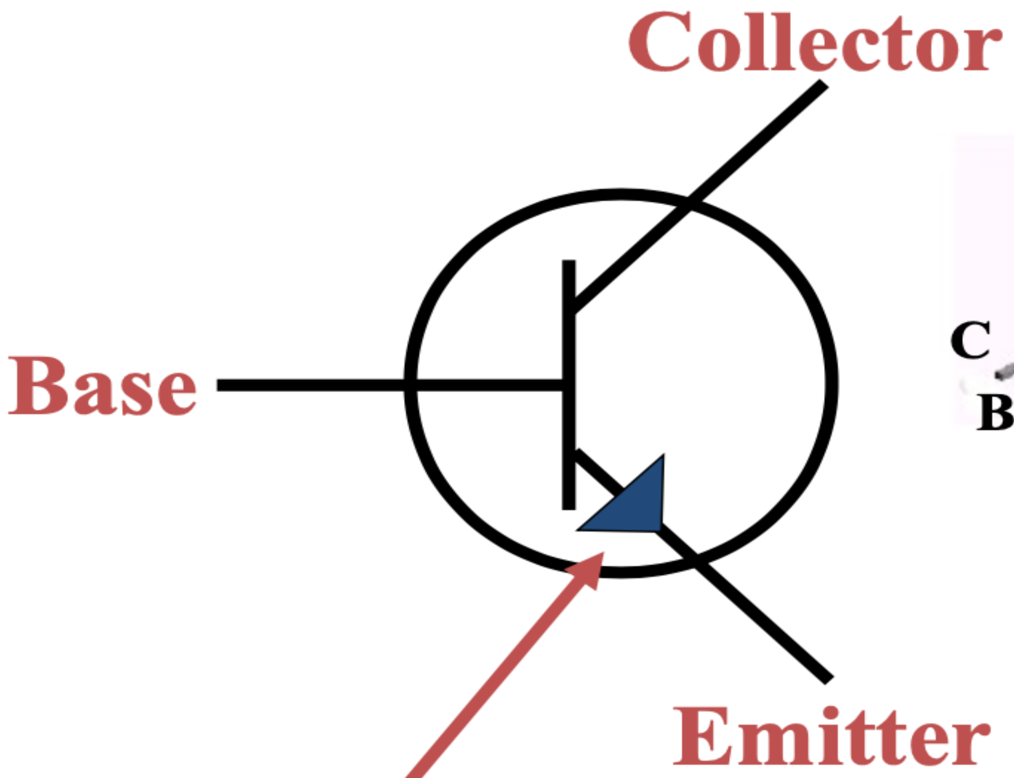


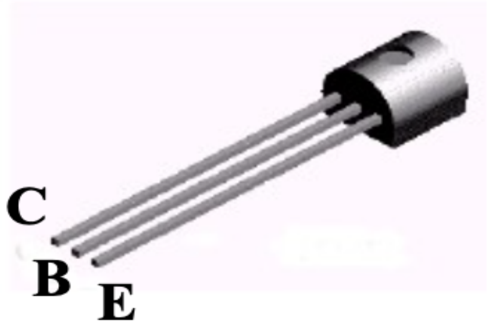
$$\beta = \frac{99\text{ mA}}{1\text{ mA}} = 99$$

Transistor Operation



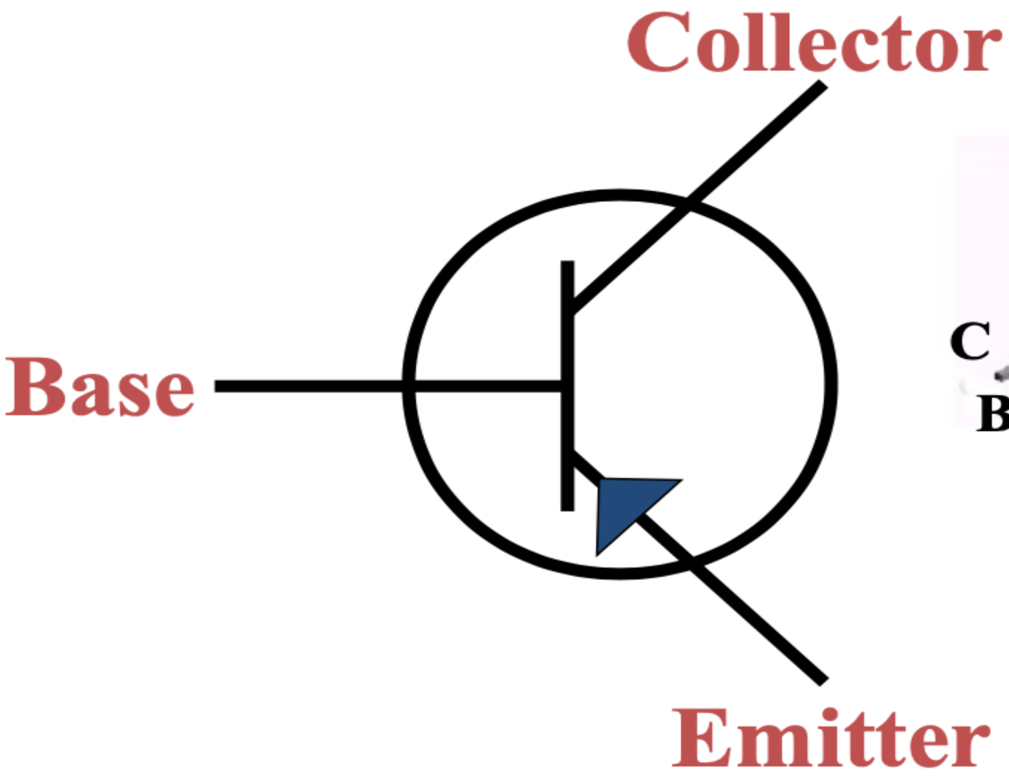
NPN Schematic Symbol

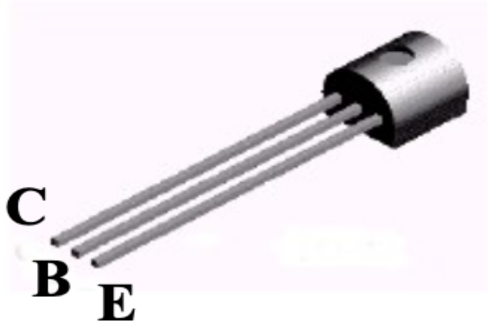




Memory aid: NPN
means Not Pointing iN.

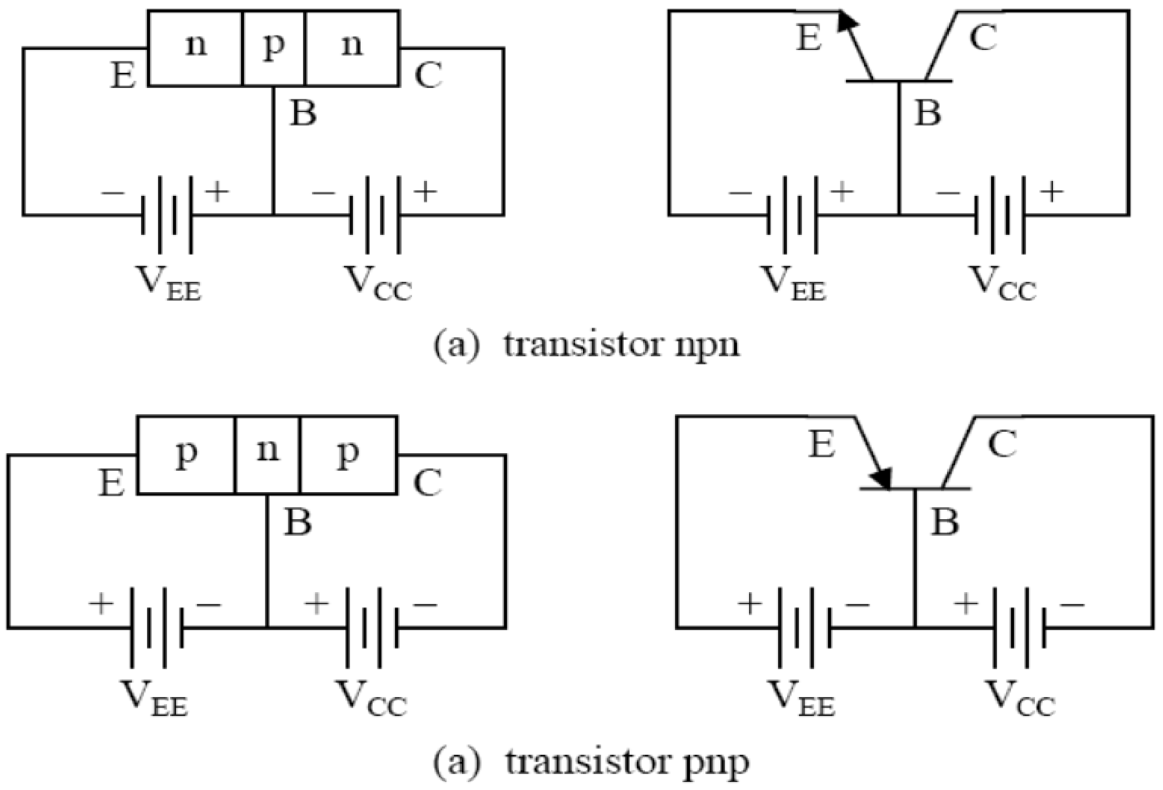
PNP Schematic Symbol





Memory aid: NPN
means Pointing iN Properly.

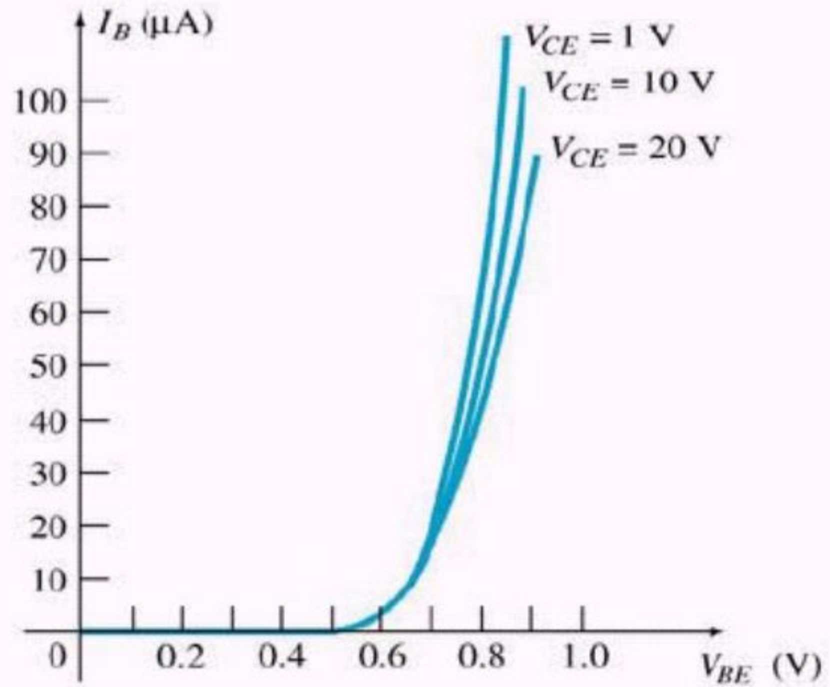
Recall: NPN and PNP Bias



- Fundamental operation of pnp transistor and npn transistor is similar except for:
  - role of electron and hole,
  - voltage bias polarity, and
  - Current direction

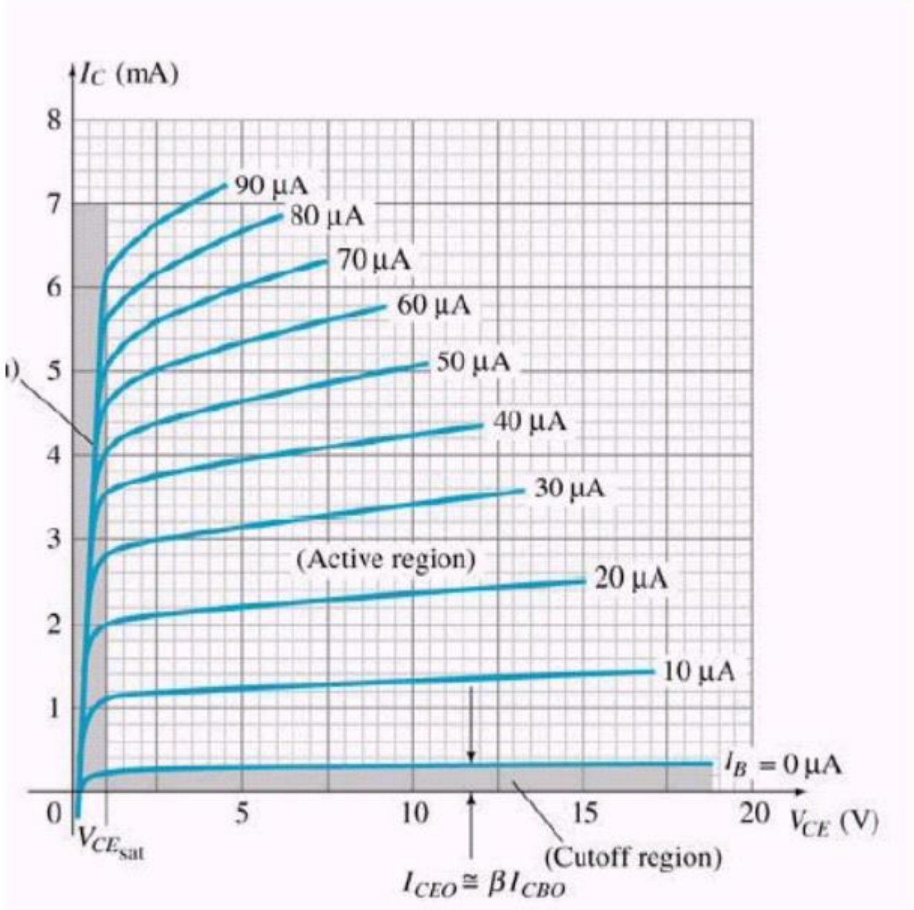
I-V Characteristic for CE configuration : Input characteristic

- Input characteristic: input current (I_B) against input voltage (V_{BE}) for several output voltage (V_{CE})
- From the graph
  - $I_B = 0$ A $V_{BE} < 0.7V$ (Si)
  - I_B = value $V_{BE} > 0.7V$ (Si)
- The transistor turned on when $V_{BE} = 0.7V$



I-V Characteristic for CE configuration : Output characteristic

- Output characteristic: output current (I_C) against output voltage (V_{CE}) for several input current (I_B)
- 3 operating regions:
  - Saturation region
  - Cut-off region
  - Active region

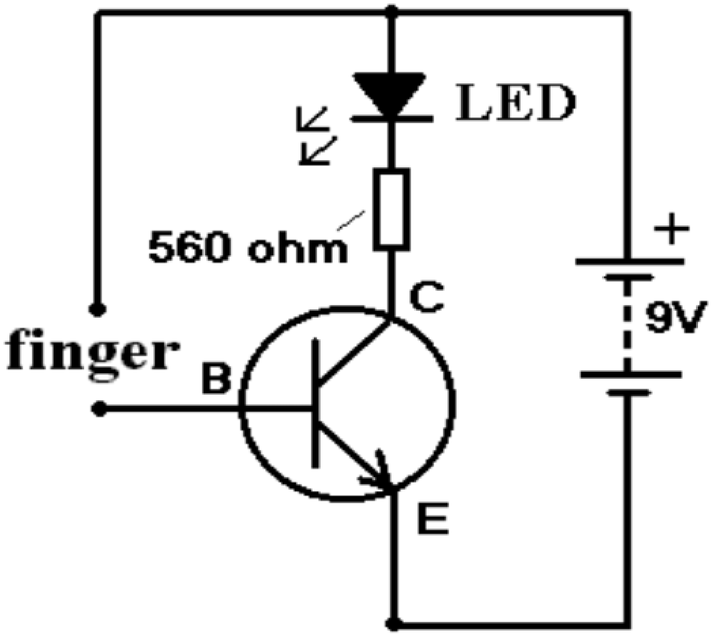


I-V Characteristic for CE configuration : Output characteristic

- Saturation region – in which both junctions are forward-biased and I_C increase linearly with V_{CE}
- Cut-off region – where both junctions are reverse-biased, the I_B is very small, and essentially no I_C flows, I_C is essentially zero with increasing V_{CE}
- Active region – in which the transistor can act as a linear amplifier, where the BE junction is forward-biased and BC junction is reverse-biased. I_C increases drastically although only small changes of I_B.
- Saturation and cut-off regions – areas where the transistor can operate as a switch
- Active region – area where transistor operates as an amplifier

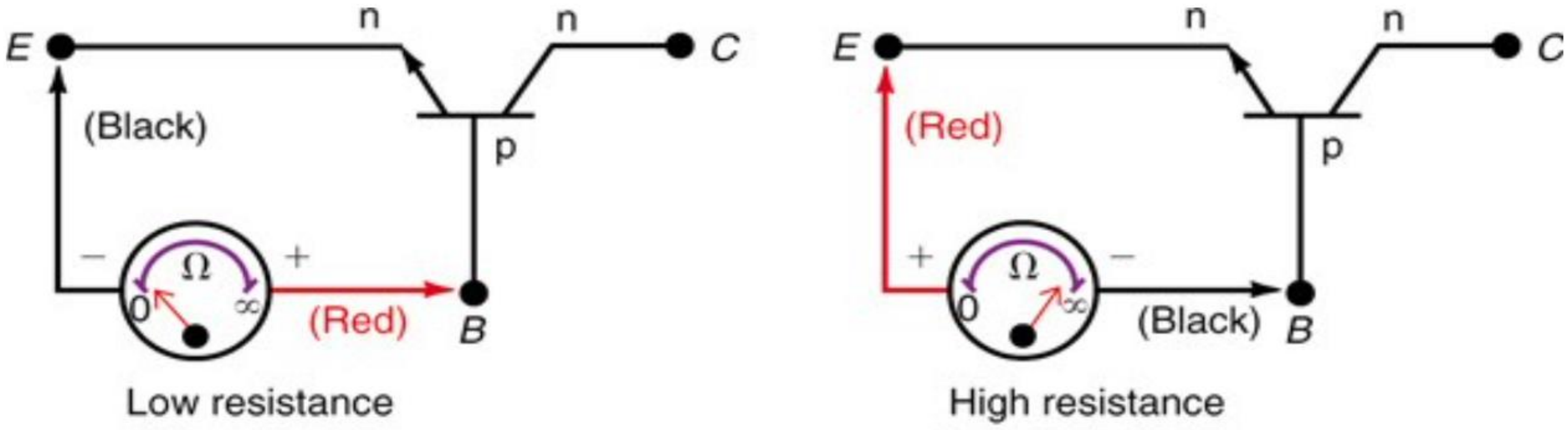
Simple Transistor Circuit

- Pictured below is a very simple circuit which demonstrates the use of **transistors**. When a finger is placed in the circuit where shown, a tiny current of around 0.1mA flows (assuming a finger resistance of 50,000 Ohms). This is nowhere near enough to light the LED which needs at least 10mA. However the tiny current is applied to the *Base* of the transistor where it is boosted by a factor (gain) of around 100 times and the LED lights!



Checking a Transistor with an Ohmmeter

- To check the base-emitter junction of an npn transistor, first connect the ohmmeter as shown in Fig. 28-9 (a) and then reverse the ohmmeter leads as shown in (b).
- For a good p-n junction made of silicon, the ratio R_R/R_F should be equal to or greater than 1000:1.

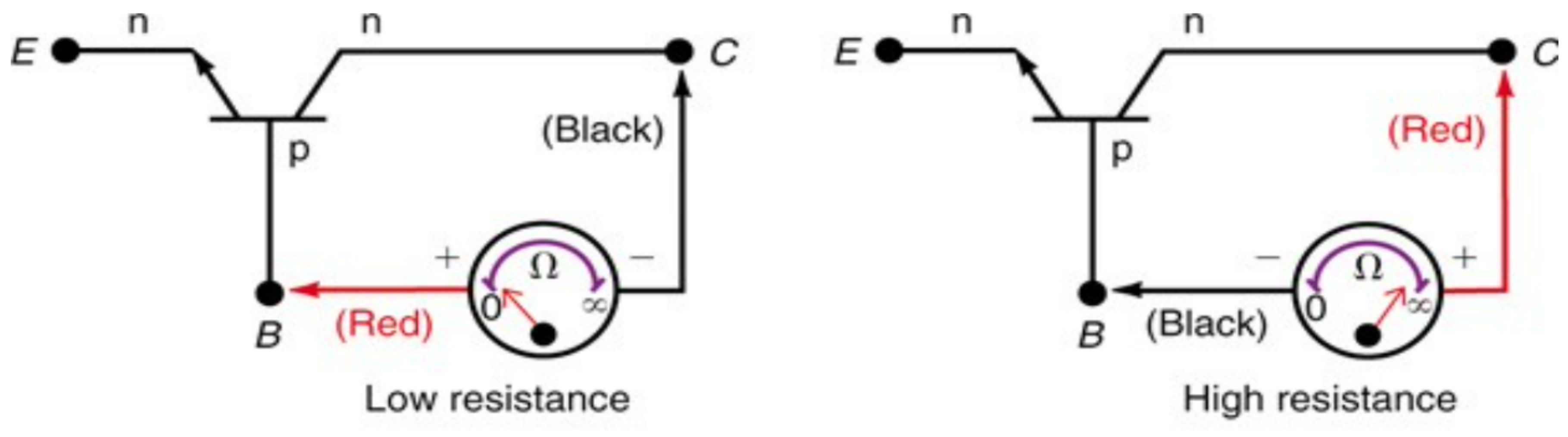


(a)

(b)

Checking a Transistor with an Ohmmeter

- To check the <u>collector-base</u> junction, first connect the ohmmeter as shown in Fig. 28-10 (a) and then reverse the ohmmeter leads as shown in (b).
- For a good p-n junction made of silicon, the ratio R_R/R_F should be equal to or greater than 1000:1.
- The resistance measured between the collector and emitter should read high or infinite for <u>both</u> connections of the meter leads.

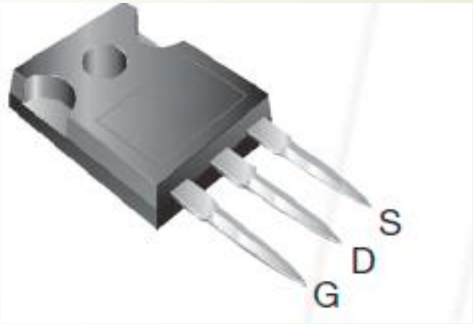


(a) (b)

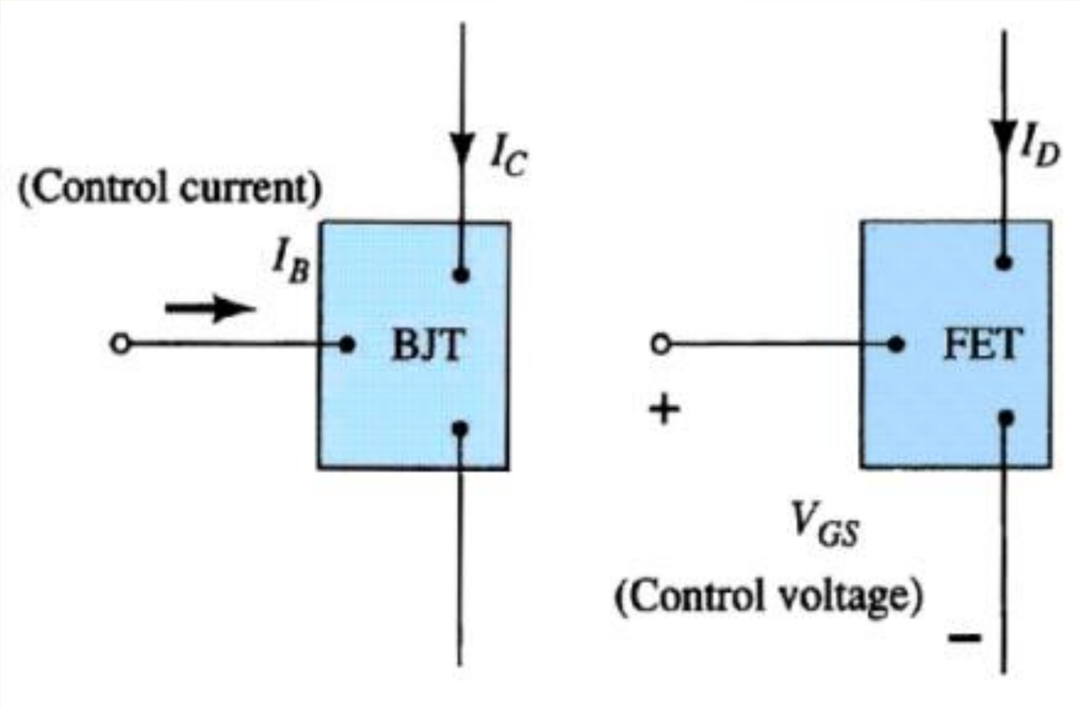
Checking a Transistor with an Ohmmeter

- Low resistance across the junctions in both directions: transistor is shorted.
- High resistance on both directions: transistor is open.
- In these cases, the transistor is defective and must be replaced.

MOSFET’s (Metal–Oxide–Semiconductor Field-Effect Transistor)



Current Controlled vs Voltage Controlled Devices

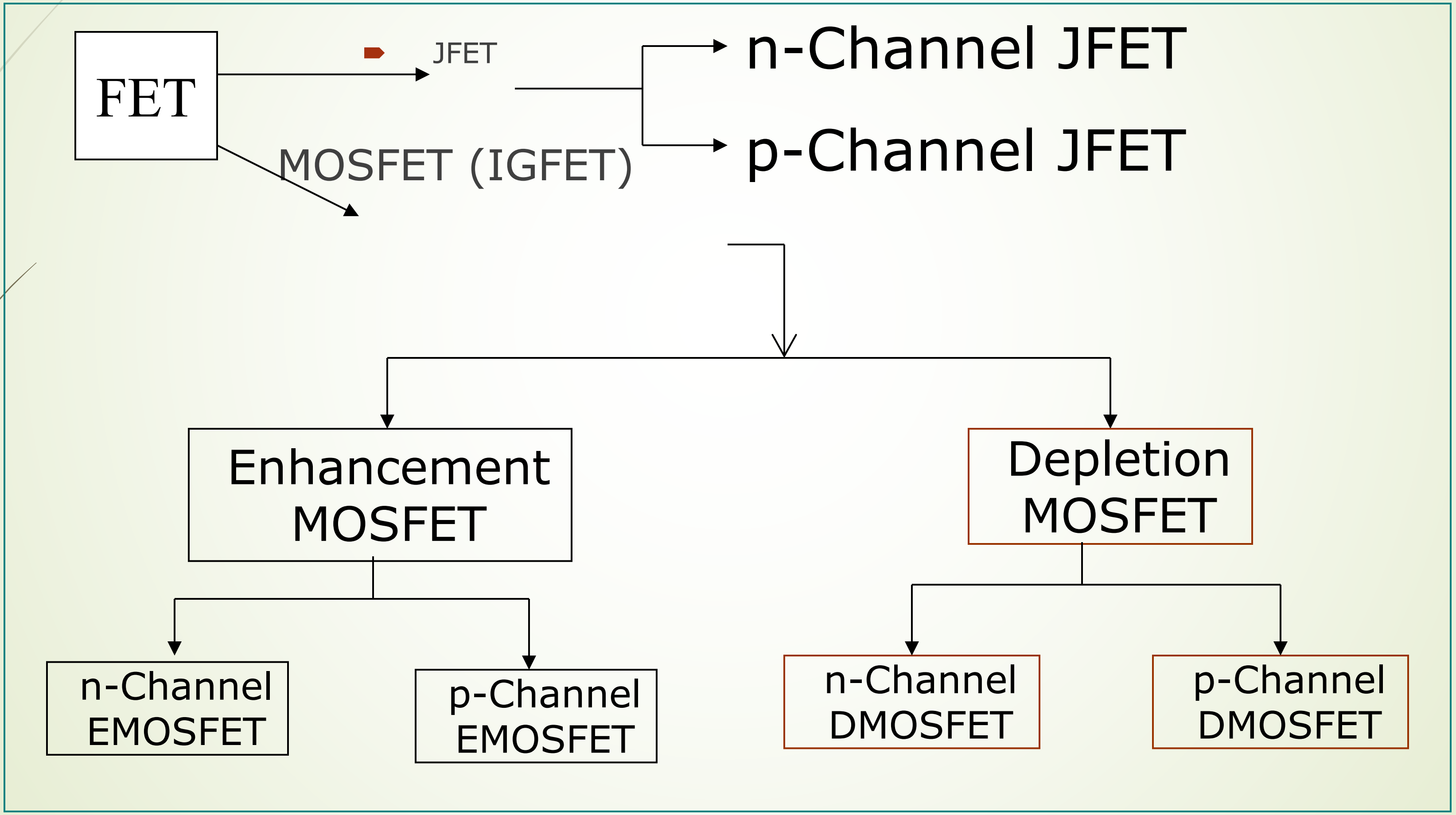


FET (Field Effect Transistor)

Few important advantages of FET over conventional Transistors

1. Unipolar device i. e. operation depends on only one type of charge carriers (*h* or *e*)
2. Voltage controlled Device (gate voltage controls drain current)
3. Very high input impedance ($\approx 10^{9}$-$10^{12}\,\Omega$)
4. Low Voltage Low Current Operation is possible (Low-power consumption)
5. Less Noisy as Compared to BJT
6. Very small in size, occupies very small space in ICs
7. Low voltage low current operation is possible in MOSFETS

Types of Field Effect Transistors (The Classification)

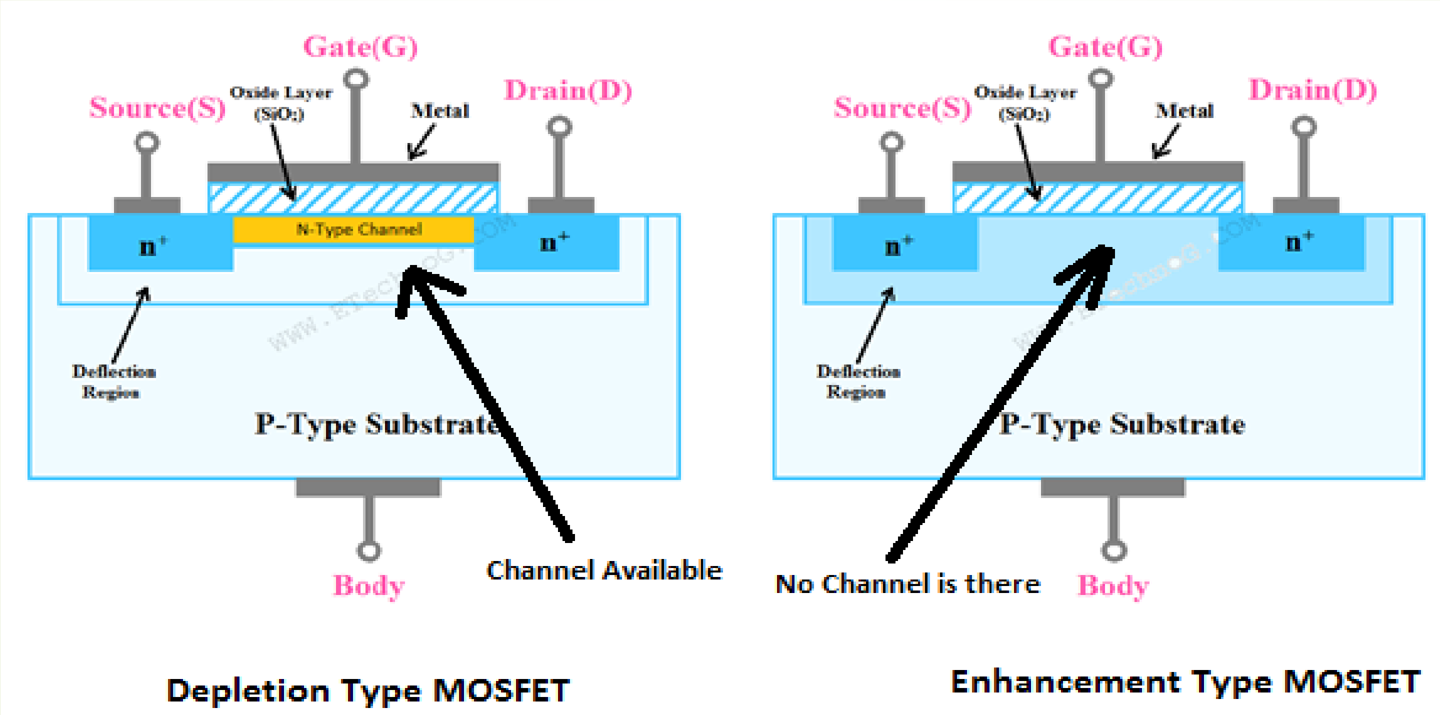


MOSFETs

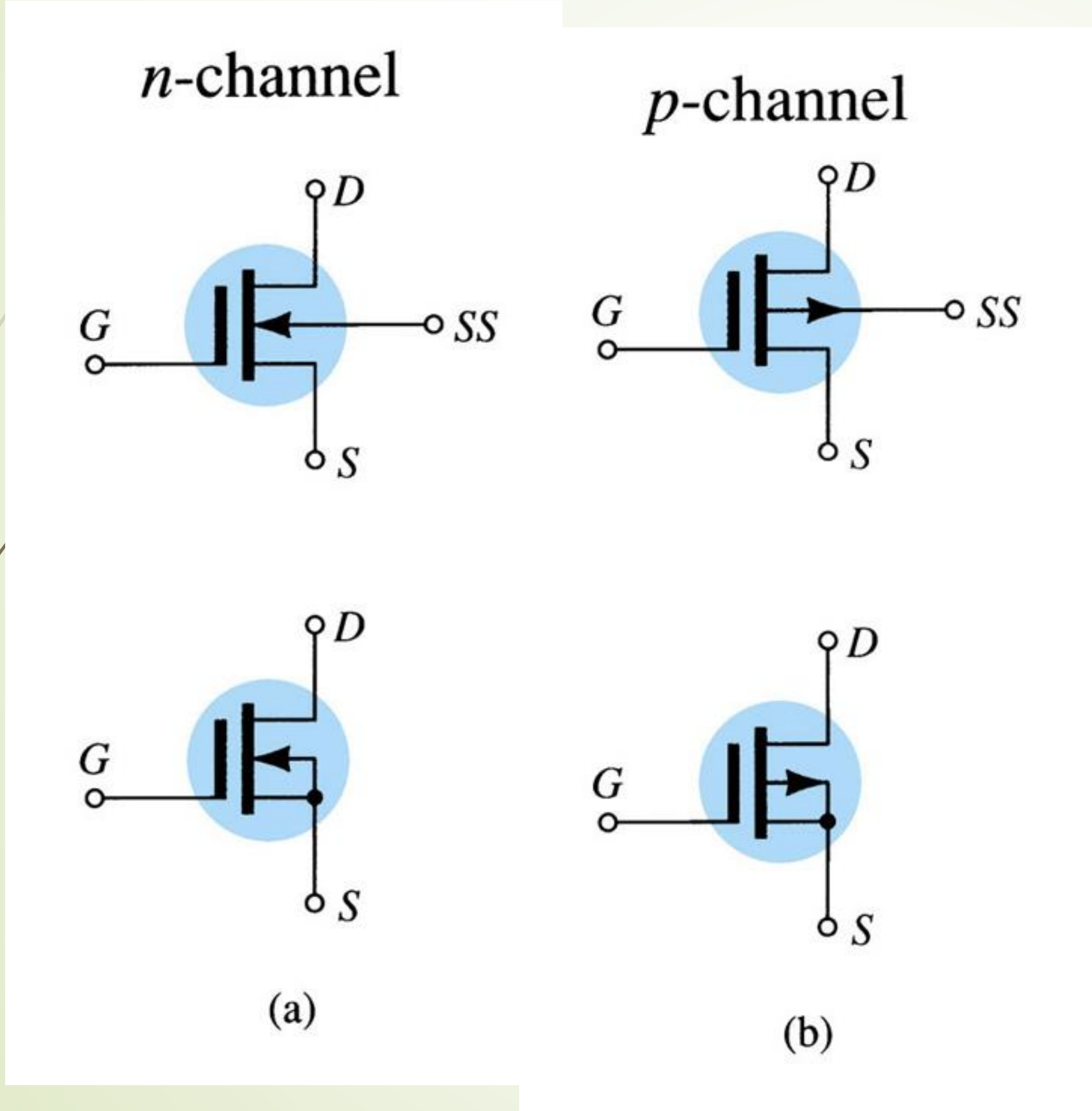
MOSFETs have characteristics similar to JFETs and additional characteristics that make them very useful.

There are 2 types of MOSFET’s:

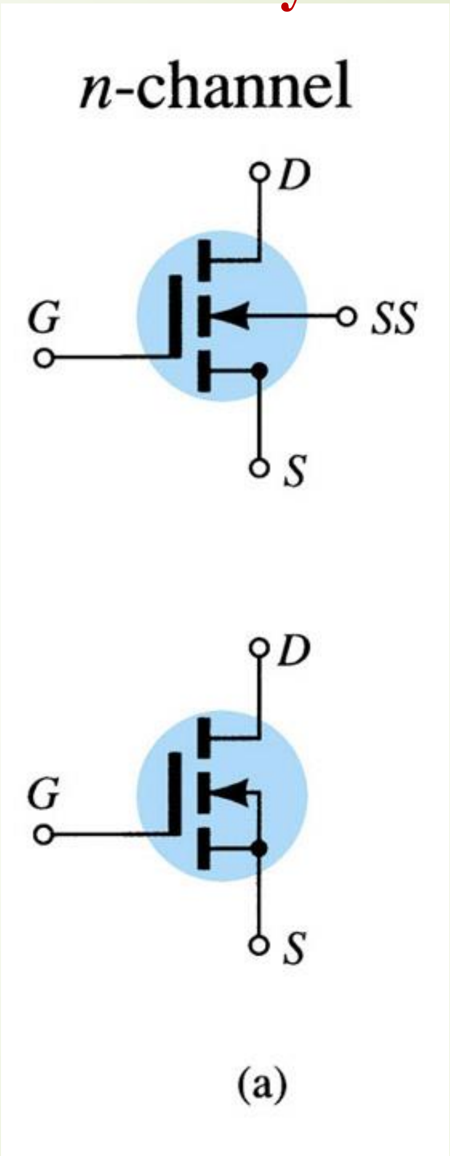
- Depletion mode MOSFET (D-MOSFET)
- Enhancement Mode MOSFET (E-MOSFET)



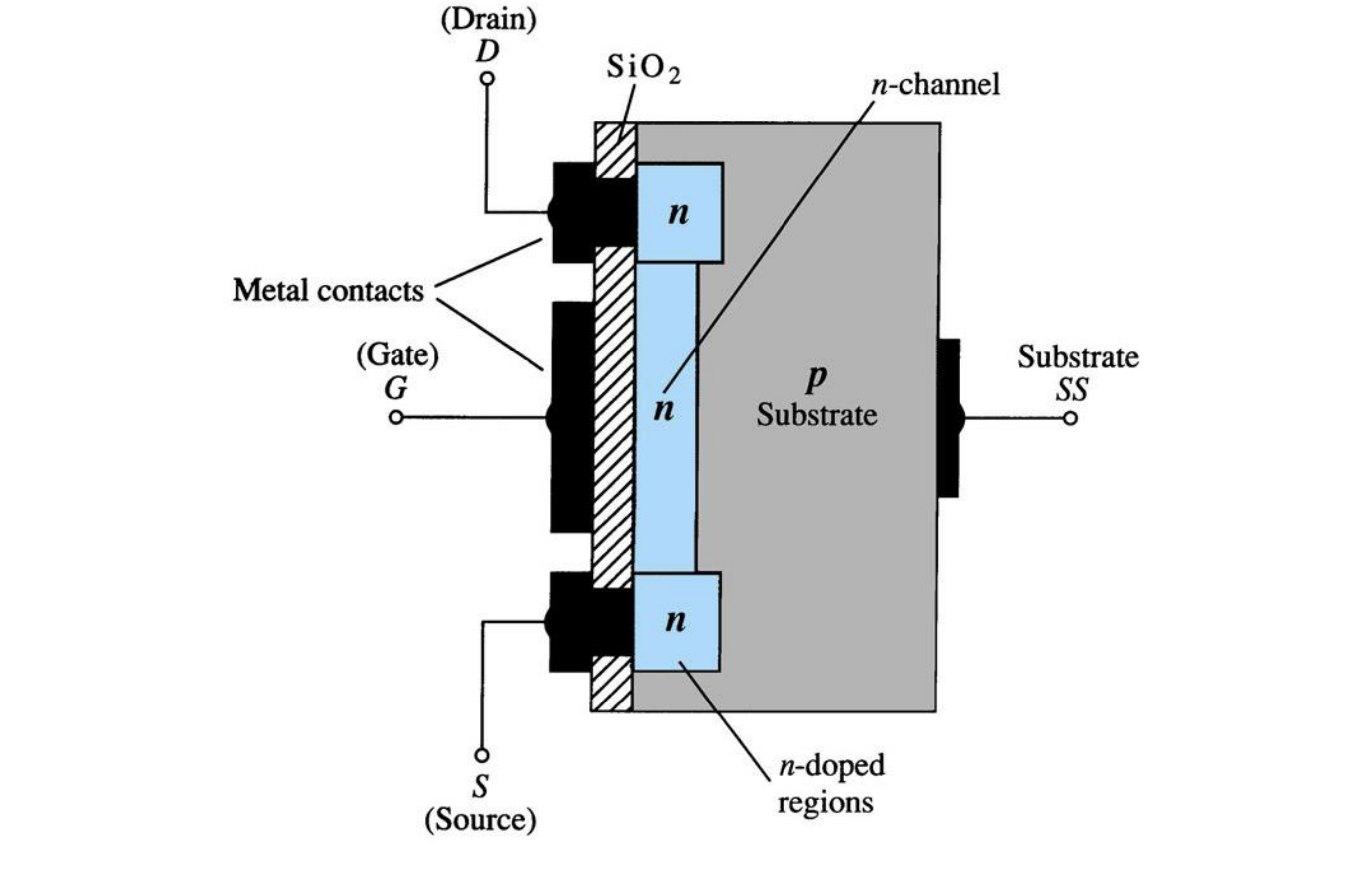
D-MOSFET Symbols



E-MOSFET Symbols

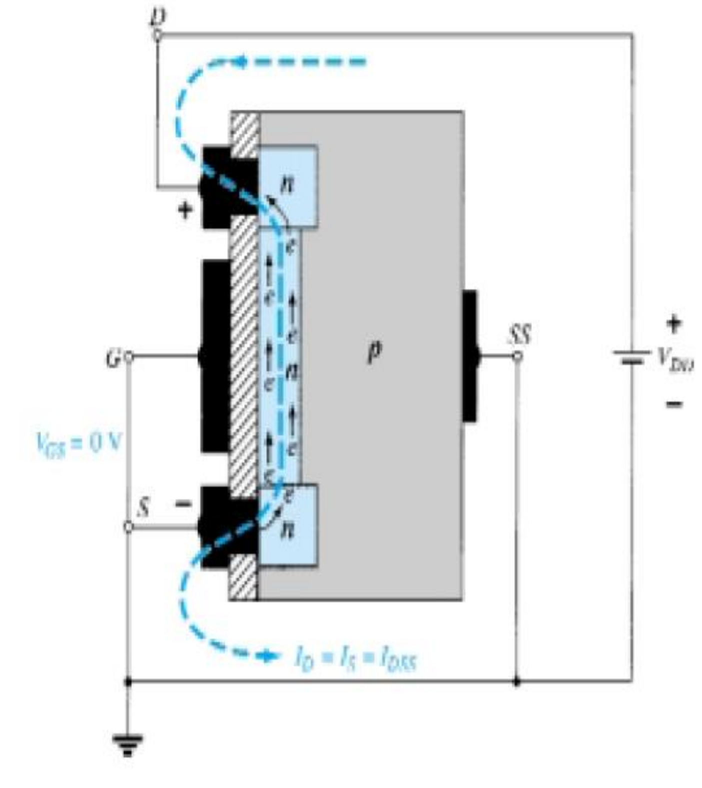


Depletion Mode MOSFET Construction

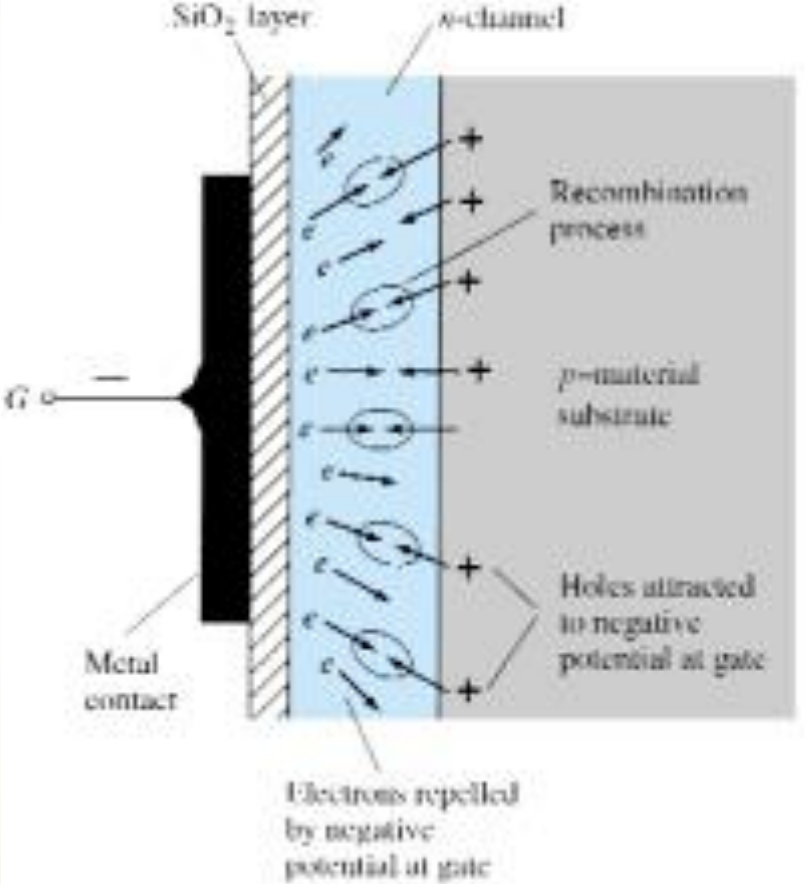


The Drain (D) and Source (S) leads connect to the to n-doped regions
These N-doped regions are connected via an n-channel
This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basics Operation

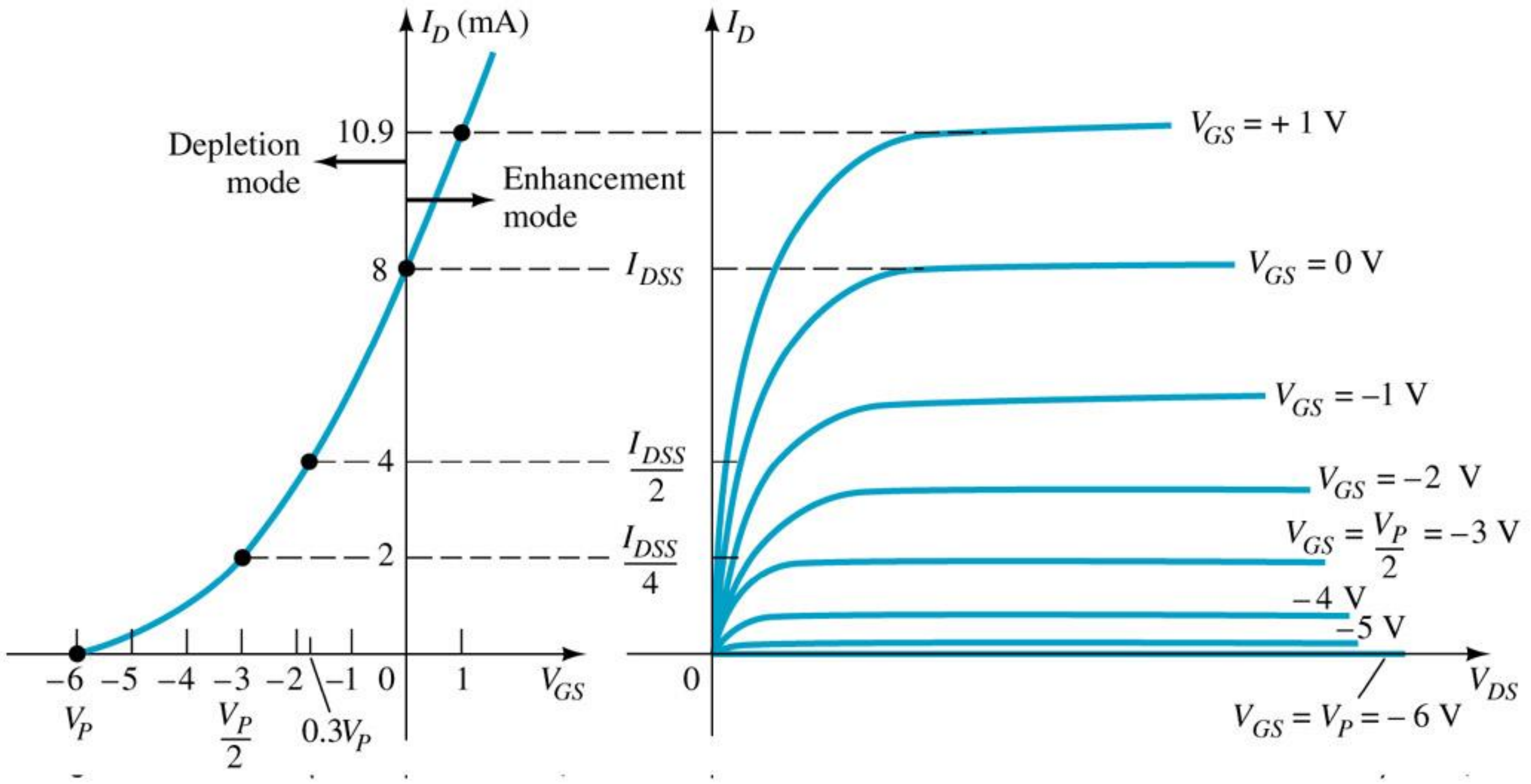


n-Channel depletion-type MOSFET with V_{GS} = 0 V and an applied

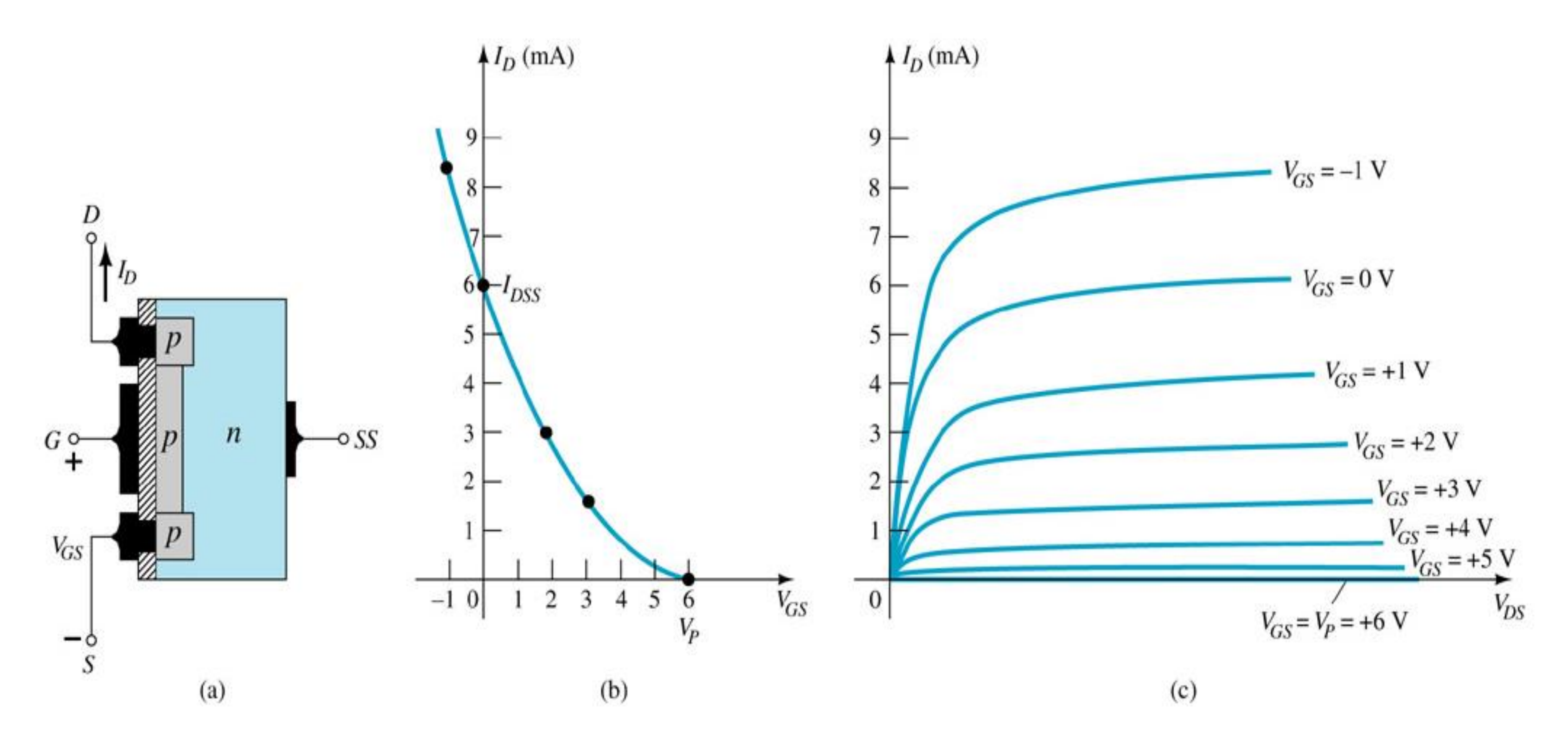


Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion** mode or the **Enhancement** mode



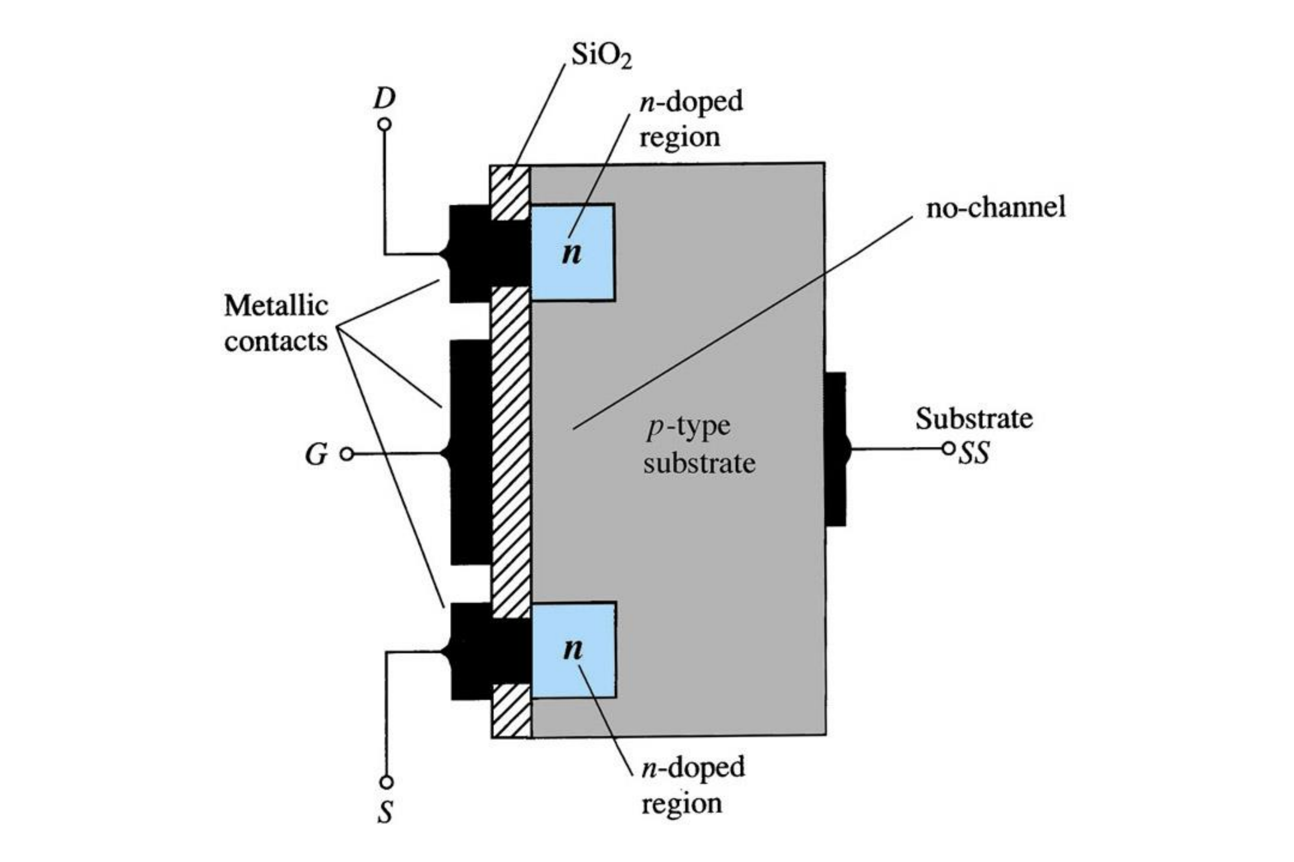
p-Channel Depletion Mode MOSFET



The p-channel Depletion mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed

Enhancement Mode MOSFET's

Enhancement Mode MOSFET Construction



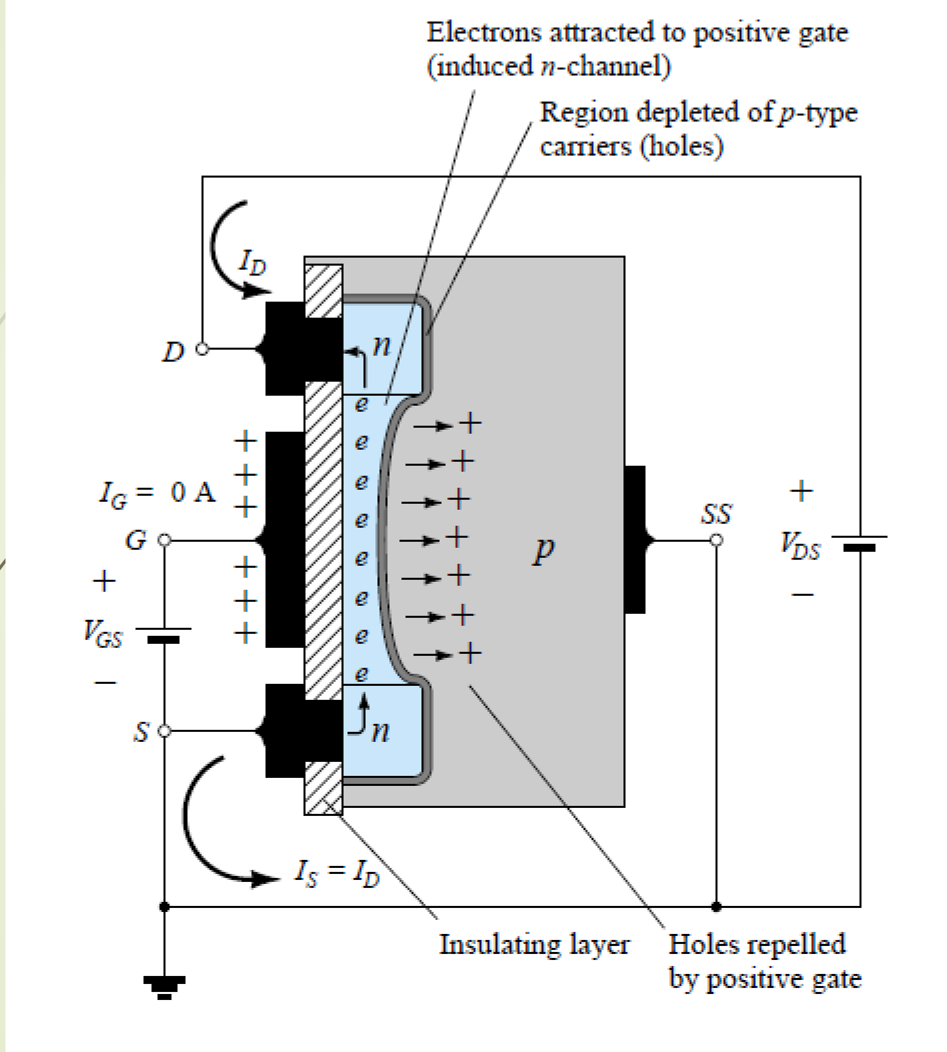
The Drain (D) and Source (S) connect to the to n-doped regions

These n-doped regions are not connected via an n-channel without an external voltage

The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2

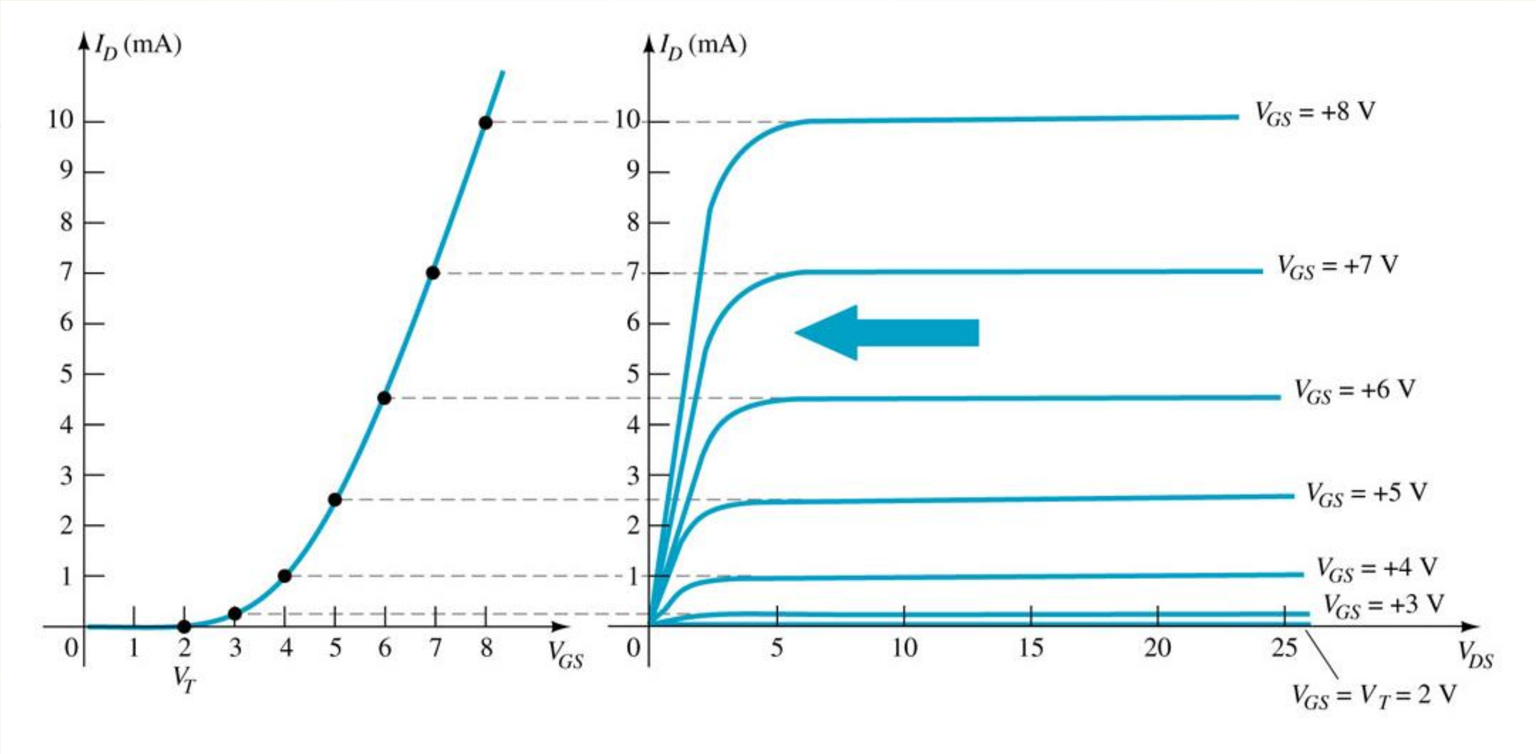
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basics operation



Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive

$I_{DSS} = 0$ when $V_{GS} < V_T$

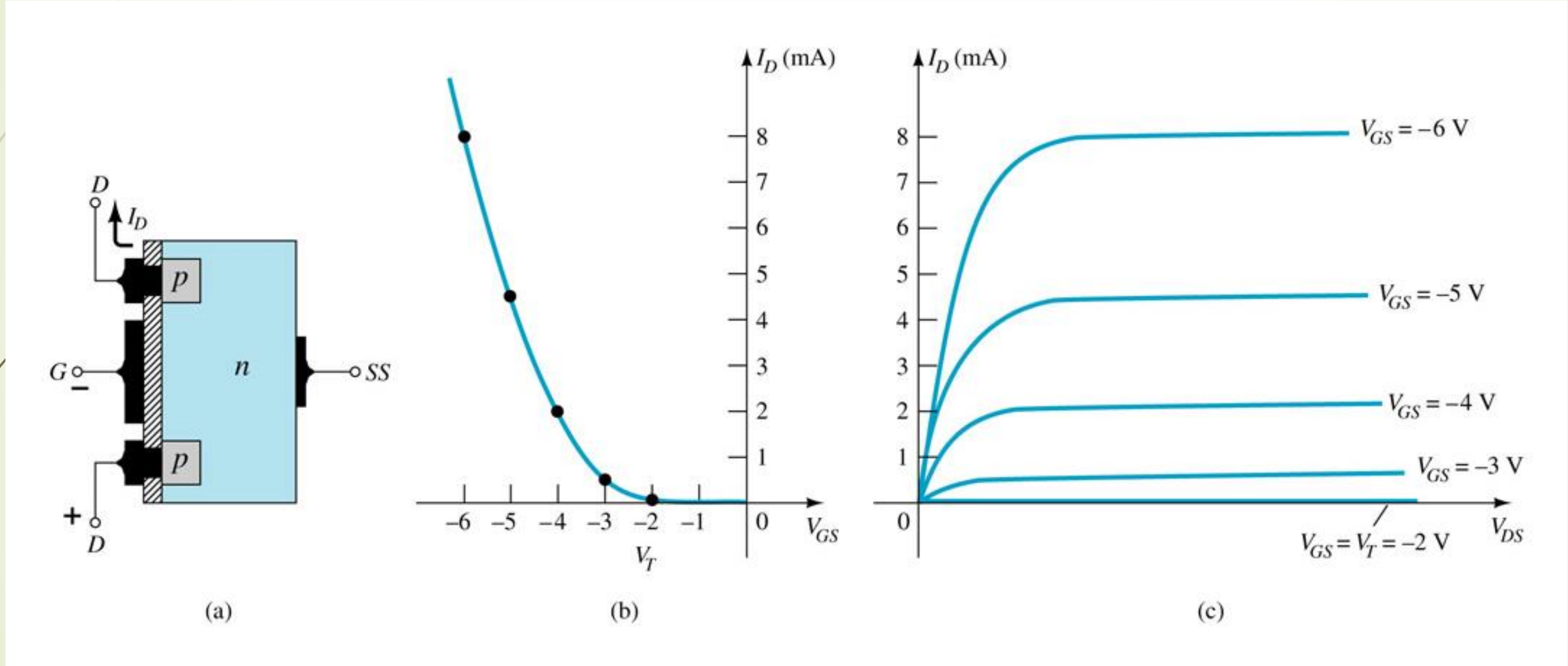
As V_{GS} increases above V_T, I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

p-Channel Enhancement Mode MOSFETs

The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



MCQ

A JFET has three terminals, namely …………

(A) cathode, anode, grid

(B) emitter, base, collector

(C) source, gate, drain

(D) none of the above

MCQ

A JFET has three terminals, namely …………

(A) cathode, anode, grid

(B) emitter, base, collector

(C) **source, gate, drain**

(D) none of the above

MCQ

A MOSFET is a ………… driven device

(A) current

(B) voltage

(C) both current and voltage

(D) none of the above

MCQ

A MOSFET is a ………… driven device

(A) current

(B) **voltage**

(C) both current and voltage

(D) none of the above

MCQ

A MOSFET can be operated with ……………..

(A) negative gate voltage only

(B) positive gate voltage only

(C) positive as well as negative gate voltage

(C) none of the above

MCQ

A MOSFET can be operated with ……………..

(A) negative gate voltage only

(B) positive gate voltage only

(C) **positive as well as negative gate voltage**

(C) none of the above

MCQ

The input control parameter of a MOSFET is ……………

(A) gate voltage

(B) source voltage

(c) drain voltage

(D) gate current

MCQ

The input control parameter of a MOSFET is ……………

(A) gate voltage

(B) source voltage

(c) drain voltage

(D) gate current

MCQ

The input impedance of a MOSFET is of the order of ………..

(A) 1 Ω

(B) a few hundred Ω

(C) kΩ

(D) several MΩ

MCQ

The input impedance of a MOSFET is of the order of ……….

(A) 1 Ω

(B) a few hundred Ω

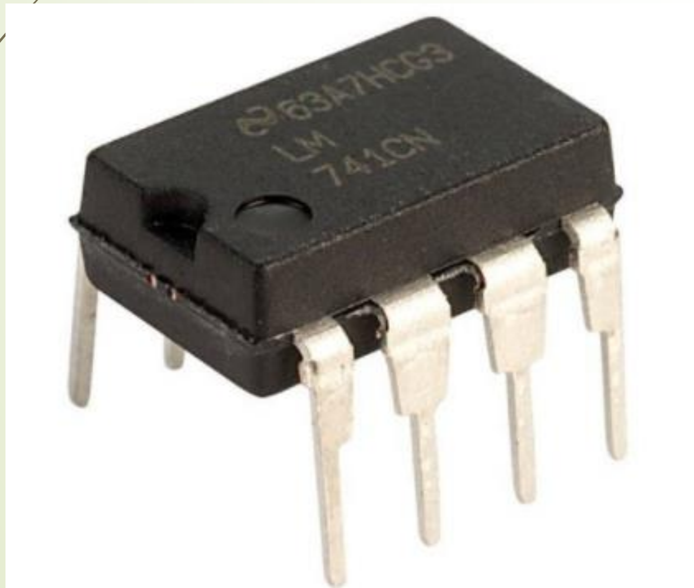
(C) kΩ

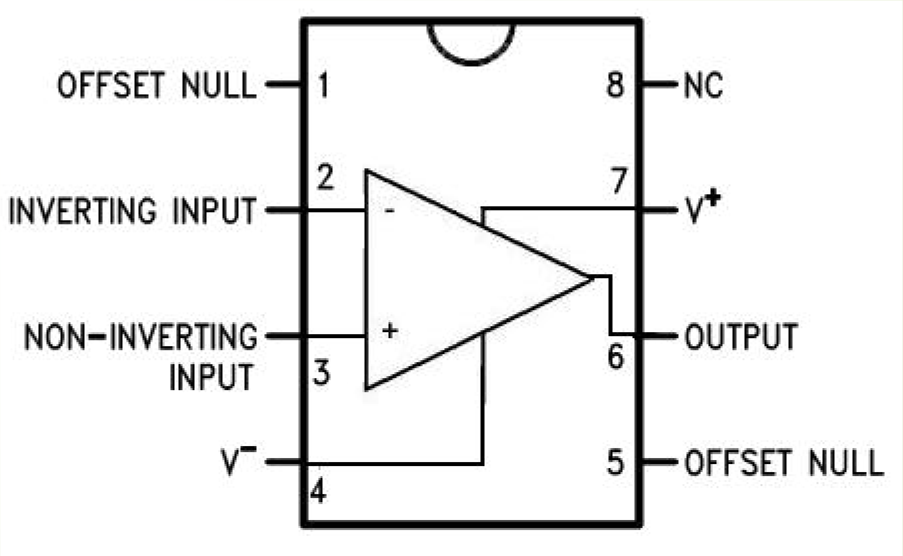
(D) several MΩ

Unit-2:

OP-AMP

(Operational Amplifier)





Op-Amp Applications

Linear

- Scale /Sign Changer Amplifier
- Adder
- Substractor
- Instrumentation Amplifier
- Integrator Differentiator
- Log & Antilog Amplifier

Non-Linear

- Comparator
- Zero crossing detector
- Amplitude distribution analyzer
- Window detector
- Schmitt Trigger
- Precision Half and full wave rectifier
- Sample and Hold circuits
- Clippers and Clamper

Wave Shaping

- Sine wave generator
- Triangular and Rectangular wave generator
- Astable Multivibrator
- Monostable Multivibrator
- Bistable Multivibrator

MCQ

- In which of the following application op-amp is/are used?

(a) Integrator and Differentiator

(b) Voltage to Current Converter

(c) Adder or Summing Amplifier

(d) All of the above

MCQ

- In which of the following application op-amp is/are used?

(a) Integrator and Differentiator
(b) Voltage to Current Converter
(c) Adder or Summing Amplifier
(d) **All of the above**

Introduction

- OP-AMP is basically a multistage amplifier which uses a number of amplifier stages interconnected to each other.

- OP-AMP amplifies the difference between two signal and diminish common signal.

- The integrated op amp offers all the advantage of monolithic integrated circuit such as small size, high reliability, reduced cost, less power consumption.

What is Op-Amp

- Operational Amplifier (Op-Amp), special type of amplifier, by proper selection of its external components, it could be configured for variety of operations
- One of the most important and versatile **analog IC**
- **Two input terminals**
  - **Inverting (- ve)**
  - **Non-Inverting (+ ve)**
- **Single output terminal**
- **Very high Gain (A) = Ideally Infinite**
- **Input resistance (R_i) = Ideally Infinite**
- **Output resistance (R_o) = Ideally 0**

MCQ

- **Op-Amp is abbreviated as ________.**

(a) Operational Amplifier

(b) Operand amplitude

(c) Operational amplitude

(d) None of the above

MCQ

- **Op-Amp is abbreviated as ________.**

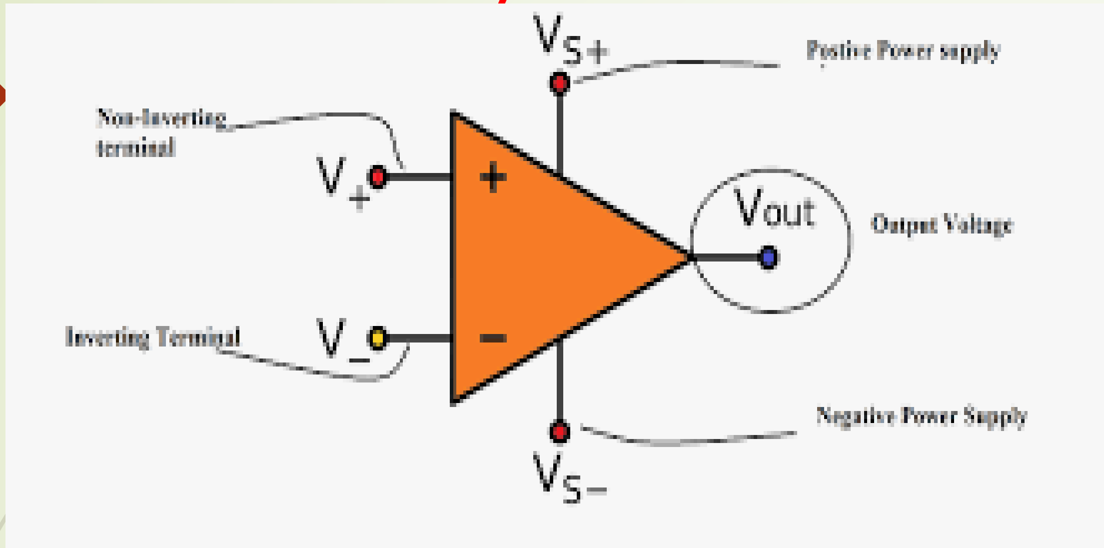
(a) Operational Amplifier

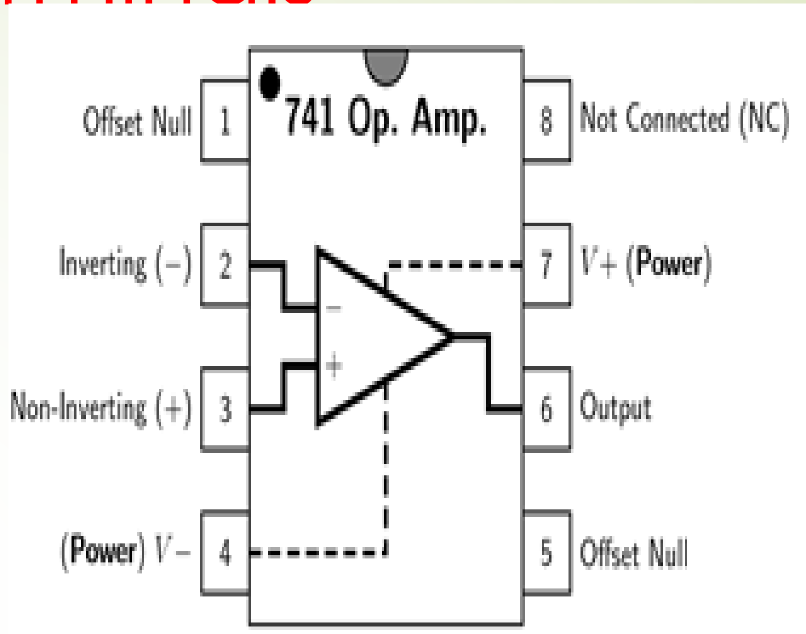
(b) Operand amplitude

(c) Operational amplitude

(d) None of the above

Symbol and terminals





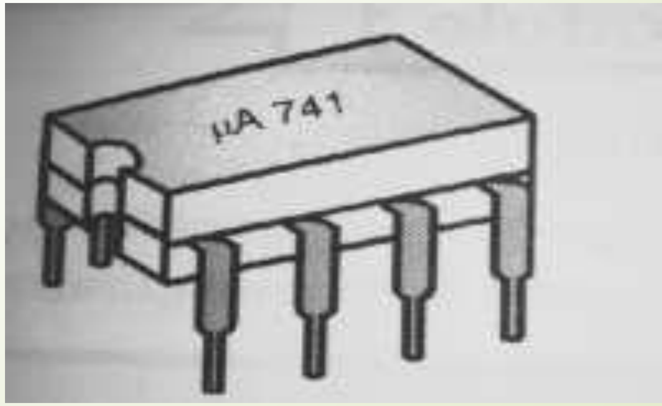
- An OP-AMP has a two input terminal, one output terminal and two supply voltage terminals.
- The input terminal marked with negative(-) sign is called as an inverting terminal .

If we connect the input signal to this terminal then the amplified output signal is 180º out of phase with respect to input.

- The input terminal marked with positive (+) sign is called as Non-Inverting terminal.

If the input is applied to this pin then the amplified output is in phase with the input.

- Offset null is used to nullify the offset voltage and pin no 8 is dummy pin.



MCQ

- **The Op-amp can amplify**

a. a.c. signals only
b. d.c. signals only
c. both a.c. and d.c. signals
d. neither d.c. nor a.c. signals

MCQ

- **The Op-amp can amplify**

a. a.c. signals only
b. d.c. signals only
c. **both a.c. and d.c. signals**
d. neither d.c. nor a.c. signals

MCQ

- Ideal Op-Amp has _______ gain.

(a) Low
(b) High
(c) Zero
(d) Infinity

MCQ

- Ideal Op-Amp has _______ gain.

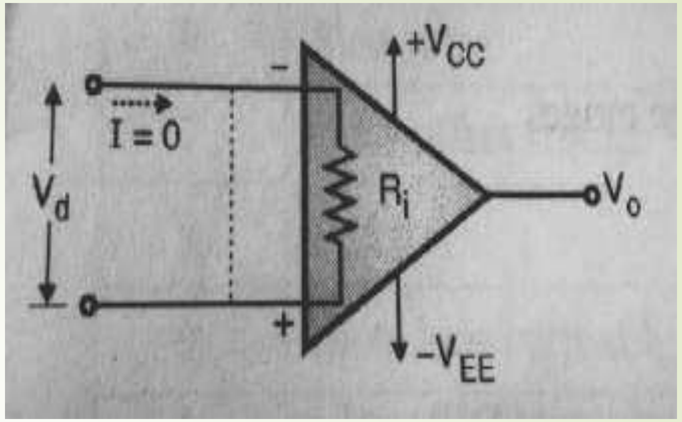
(a) Low

(b) High

(c) Zero

(d) Infinity

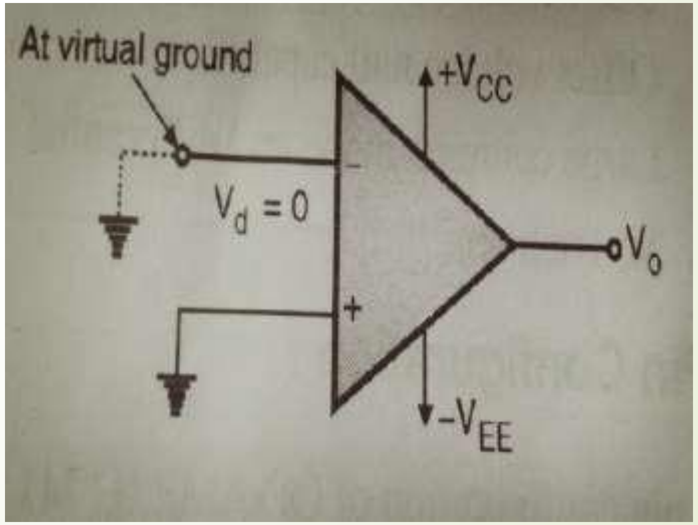
Concept of virtual short



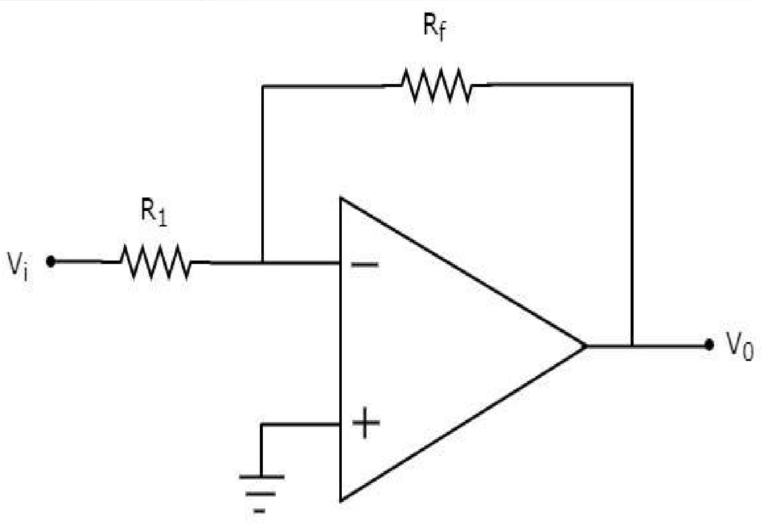
- The input impedance of an OP-AMP is ideally infinite. Hence current flowing from one input terminal to the other will be zero.
- Thus the voltage drop across Ri will be zero and both the terminals will be at the same potential.
- Means they are virtually shorted to each other

Virtual Ground

If one of the terminal of OP-AMP is connected to ground then due to the virtual short existing between the other input terminal, the other terminal is said to be at ground potential.

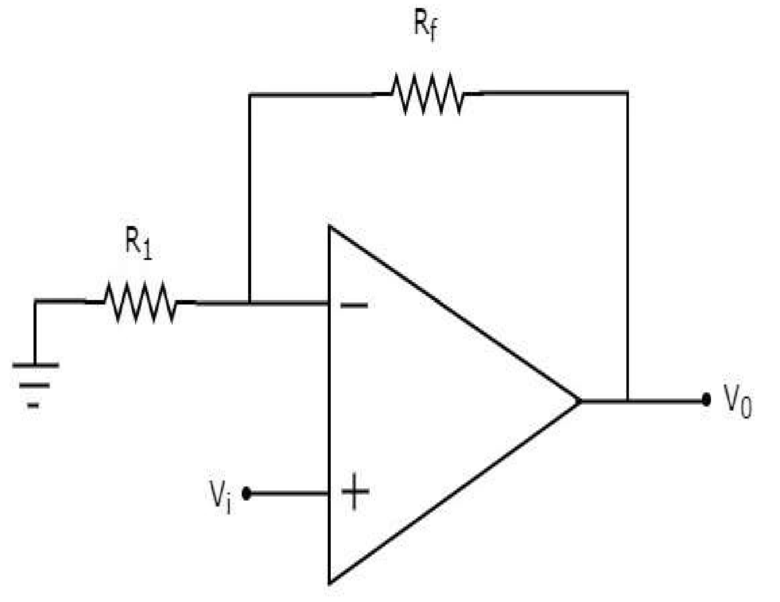


Inverting Amplifier



$$\frac{V_0}{V_i} = \frac{-R_f}{R_1}$$

Non- Inverting Amplifier



$$\frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

Characteristics of an OP-AMP

- Characteristics are important because, we can use them to compare the performance of various op amp ICs and select the best suitable from them for the required application.

characteristics	Practical value	Ideal value
Voltage gain	2×10^5	∞
Input resistance	2MΩ	∞
Output resistance	75Ω	0
Bandwidth	1 MHz	∞
CMRR	90 dB	∞
Slew rates	0.5V/µs	∞
PSRR	150µV/V	0

MCQ

- Which one of the following characteristics is true for ideal op-amp?

(a) Ri=0

(b) Ro= ∞

(c) B.W.= 0

(d) CMRR= ∞

MCQ

- Which one of the following characteristics is true for ideal op-amp?

(a) Ri=0

(b) Ro= ∞

(c) B.W.= 0

(d) ***CMRR= ∞***

MCQ

- Which one of the following characteristics is not true for ideal op-amp?

(a) Ri= ∞

(b) Ro= 0

(c) B.W.= 0

(d) Gain= ∞

MCQ

- Which one of the following characteristics is not true for ideal op-amp?

(a) Ri= ∞

(b) Ro= 0

(c) B.W.= 0

(d) Gain= ∞

MCQ

- Which one of the following combination for op-amp characteristics is true ?

(a) Ri= ∞, Voltage gain= 0

(b) Ro= 0, CMRR= ∞

(c) B.W.= 0, Voltage Gain= 0

(d) Gain= ∞, Slew Rate = 0

MCQ

- Which one of the following combination for op-amp characteristics is true ?

(a) Ri= ∞, Voltage gain= 0

(b) ***Ro= 0, CMRR= ∞***

(c) B.W.= 0, Voltage Gain= 0

(d) Gain= ∞, Slew Rate = 0