PROJECT: Thermal Expansion & CTE Mismatch Study in IC Packaging (MATLAB Simulation)

1. Project Overview

This project analyzes the effect of **Coefficient of Thermal Expansion (CTE) mismatch** between key IC packaging materials — silicon die, BT-resin substrate, and epoxy mold compound. A MATLAB-based simulation is used to model temperature-dependent expansion behavior, compute strain differences relative to silicon, and interpret the impact of thermal stress on **package warpage and reliability**.

The objective of the study is to understand how unequal material expansion during temperature variations can introduce mechanical stress, bending deformation, and long-term reliability risks such as solder fatigue, die-attach stress, and delamination.

2. Engineering Background

In semiconductor packaging, multiple bonded materials experience thermal expansion when exposed to temperature changes. Since each material has a unique CTE value, the system undergoes **differential expansion**, which generates internal stress and structural distortion.

- Silicon has **low CTE (~2.6 ppm/°C)**
- Organic substrate and mold compounds have **much higher CTE (17–20 ppm/°C)**

When these materials are bonded, the mismatch in expansion produces:

- tensile and compressive stress
- bending curvature / **package warpage**
- strain accumulation during thermal cycling

Understanding this behavior is critical for **material selection, structural design, and packaging reliability engineering**.

3. Materials & Modeling Assumptions

The study considers three commonly used IC packaging materials:

Material	Role in Package	Typical CTE (ppm/°C)
Silicon Die	Active device layer	2.6
BT Resin Substrate	Interconnect carrier	17.0
Epoxy Mold Compound	Mechanical protection	20.0

Model parameters:

- Reference temperature = **25°C**
- Simulation temperature sweep = **–40°C to 125°C**
- Increment = **5°C**
- Nominal material length = **10 mm (converted to meters for computation)**

4. Mathematical Model

Thermal expansion is computed using:

$$\Delta L = L \times CTE \times \Delta T$$

Where:

- L = initial material length
- CTE = coefficient of thermal expansion (ppm/°C → converted to ×10^{-6}
- $\Delta T = T - T_{ref}$

To evaluate warpage tendency, silicon is treated as the **reference layer**, and strain difference is computed as:

$$\Delta\varepsilon = \Delta L_{material} - \Delta L_{silicon}$$

Higher strain difference indicates **greater mismatch → higher warpage potential**.

5. MATLAB Implementation

A MATLAB script was developed to:

- define material properties
- generate temperature sweep
- compute expansion for each material
- calculate strain difference relative to silicon

- generate plots and export results

Two plots were produced:

1. **Expansion vs Temperature**
2. **Strain Difference vs Temperature**

The simulation outputs were saved into a results directory including plots and data files.

6. Results & Observations

Thermal Expansion Behavior

The simulation shows:

- Silicon exhibits **minimal expansion** due to low CTE
- Substrate and mold materials expand **significantly more** as temperature increases
- Expansion difference increases with ΔT, particularly beyond 85°C

Strain Difference Analysis

Strain mismatch relative to silicon increases steadily with temperature rise. This mismatch acts as a **primary driver of package warpage**.

Key implications:

- Tensile stress develops in high-CTE materials
- Compressive stress develops in the silicon layer
- Bending curvature forms at bonded interfaces
- Stress accumulation is amplified during **thermal cycling**

Reliability Impact

The study highlights potential risk points:

- solder joint fatigue and crack propagation
- die-attach interface stress concentration
- delamination risk at mold–substrate boundary
- long-term structural deformation under load cycles

The analysis reinforces the importance of **CTE matching, material optimization, and mechanical reliability design** in IC packaging.

7. Conclusion

The MATLAB-based CTE mismatch study demonstrates how variations in thermal expansion between silicon, substrate, and mold compound contribute to **warpage behavior and mechanical reliability challenges** in IC packages.

The results emphasize that:

- silicon acts as a structurally rigid reference layer
- organic materials contribute greater dimensional change
- strain mismatch increases with temperature
- CTE-aware material selection is essential to mitigate warpage and reliability risks

This project establishes a quantitative understanding of **thermo-mechanical interaction in IC packaging structures**, and serves as a foundational study for further work in **material optimization, thermal-mechanical modeling, and package reliability engineering**.