SPEC-AX and PARSEC-AX Extracting Accelerator Benchmarks from Microprocessor Benchmarks

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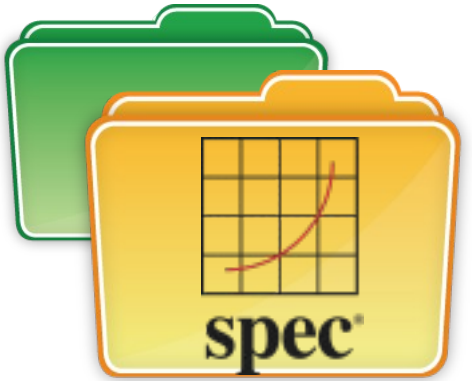
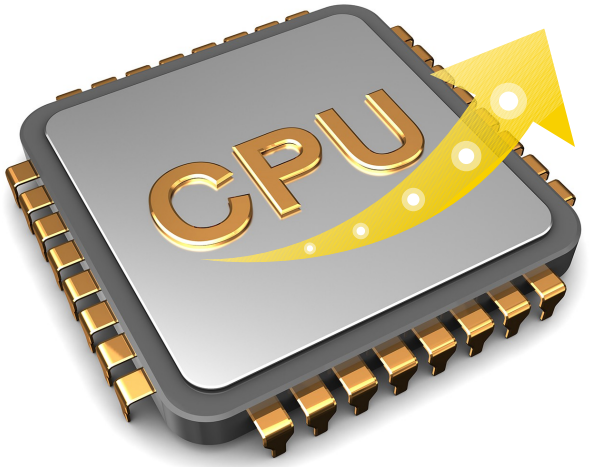
ENGAGING THE WORLD

The Problem

Benchmarks



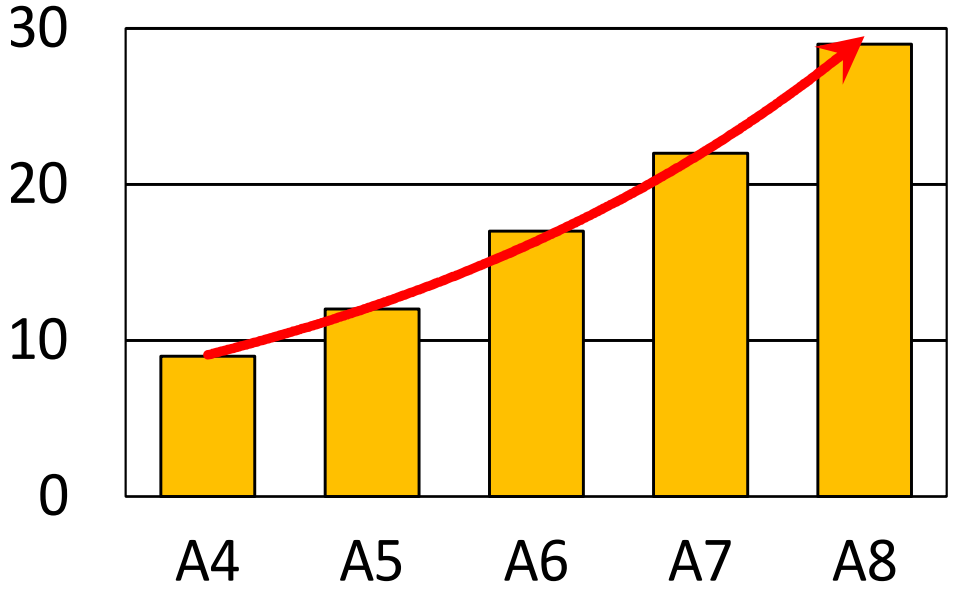


Architects

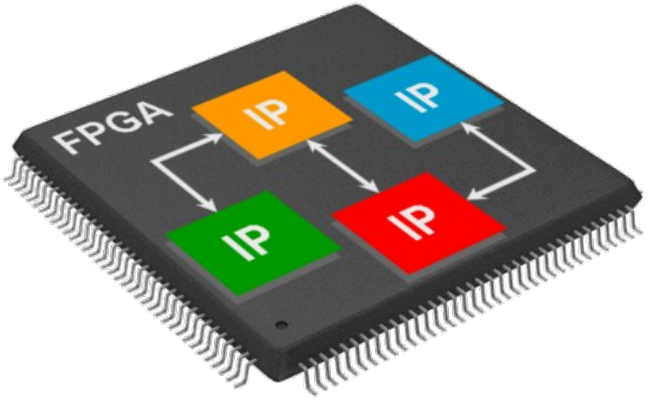
Accelerators

Breakdown of Dennard and Moore scaling

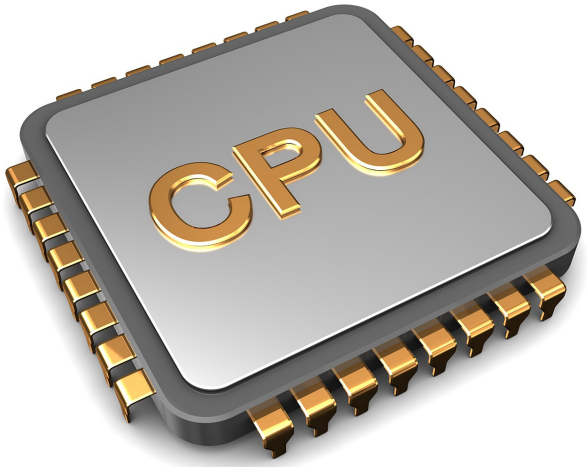
IP BLOCKS



Use accelerators !

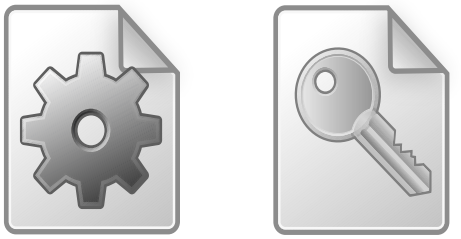


The Problem



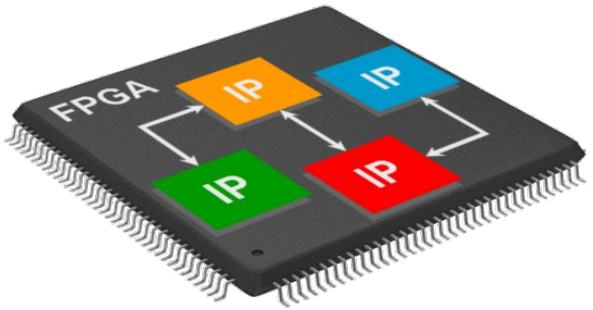
Existing Solution

LIBRARIES

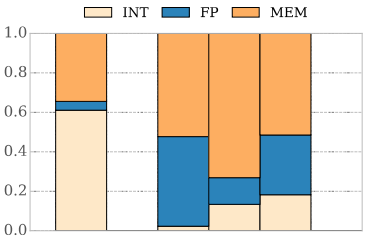


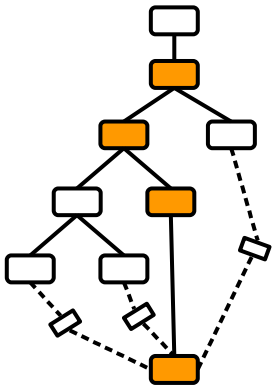
CANT GENERALIZE!

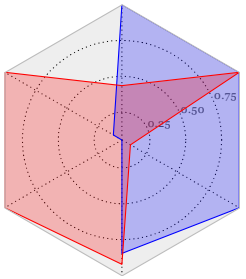
Accelerators



Executive Summary







- Accelerators present unique challenges
- Coarse grain analyses misleading
- Paths are suitable for analyses
- Characterized 29 workloads
- Release workload suite

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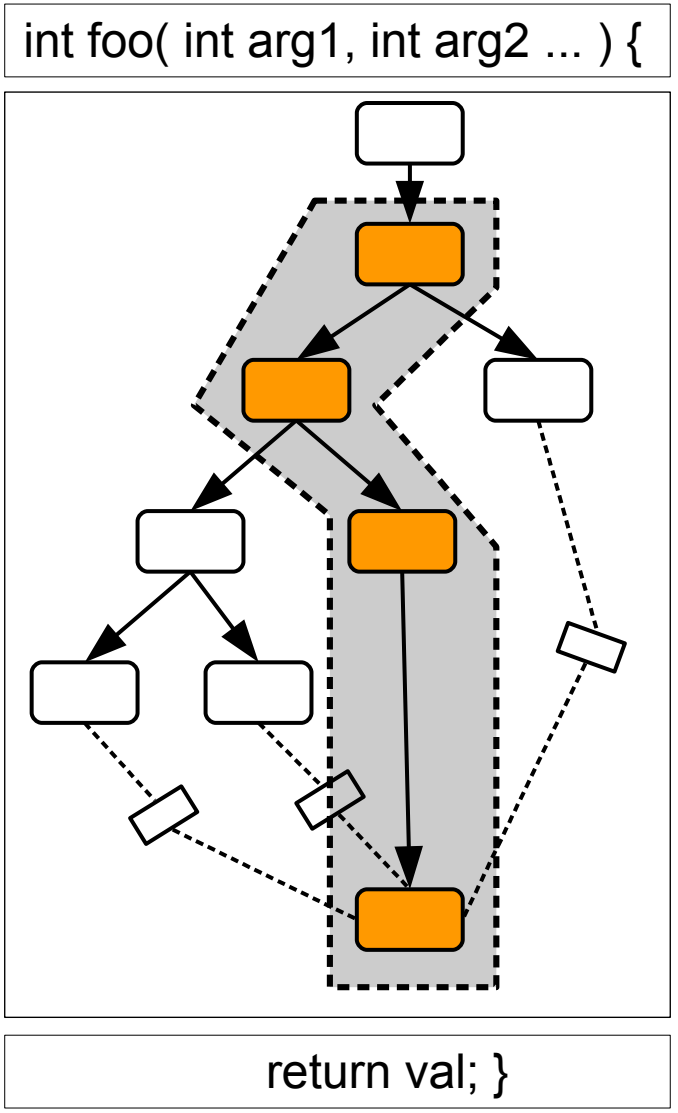
Functions and Paths



FUNCTIONS

PATHS

Ball-Larus ‘96

For Better or Worse, Benchmarks Shape a Field
– David Patterson

- Representative
- Comparable
- Generalizable

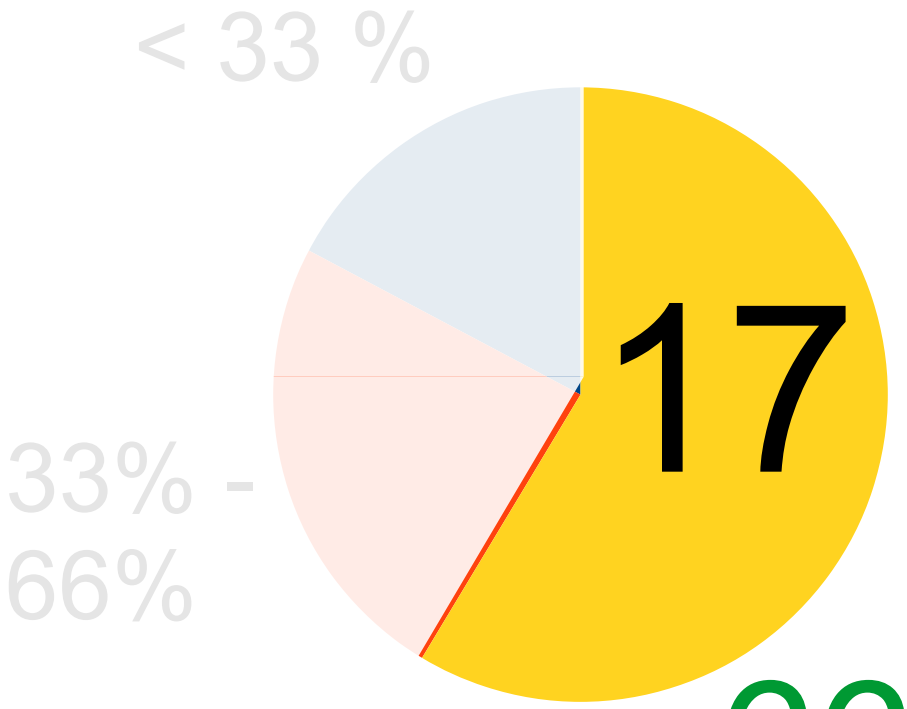
For Better or Worse, Benchmarks Shape a Field
– David Patterson

- Representative
- Comparable
- ~~Generalizable~~ Specializable

Paths are Representative

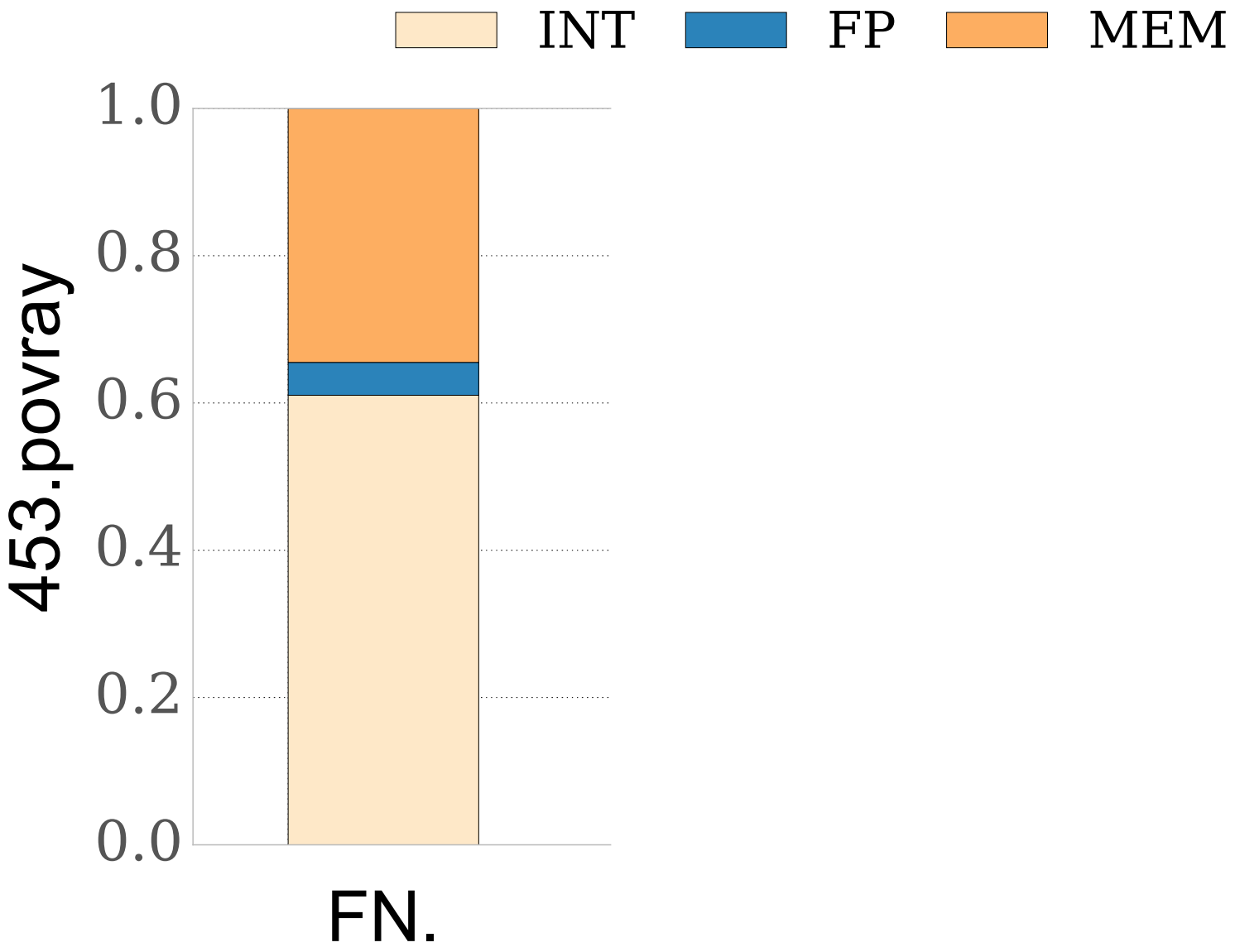
% dynamic instructions executed

Top 5 paths

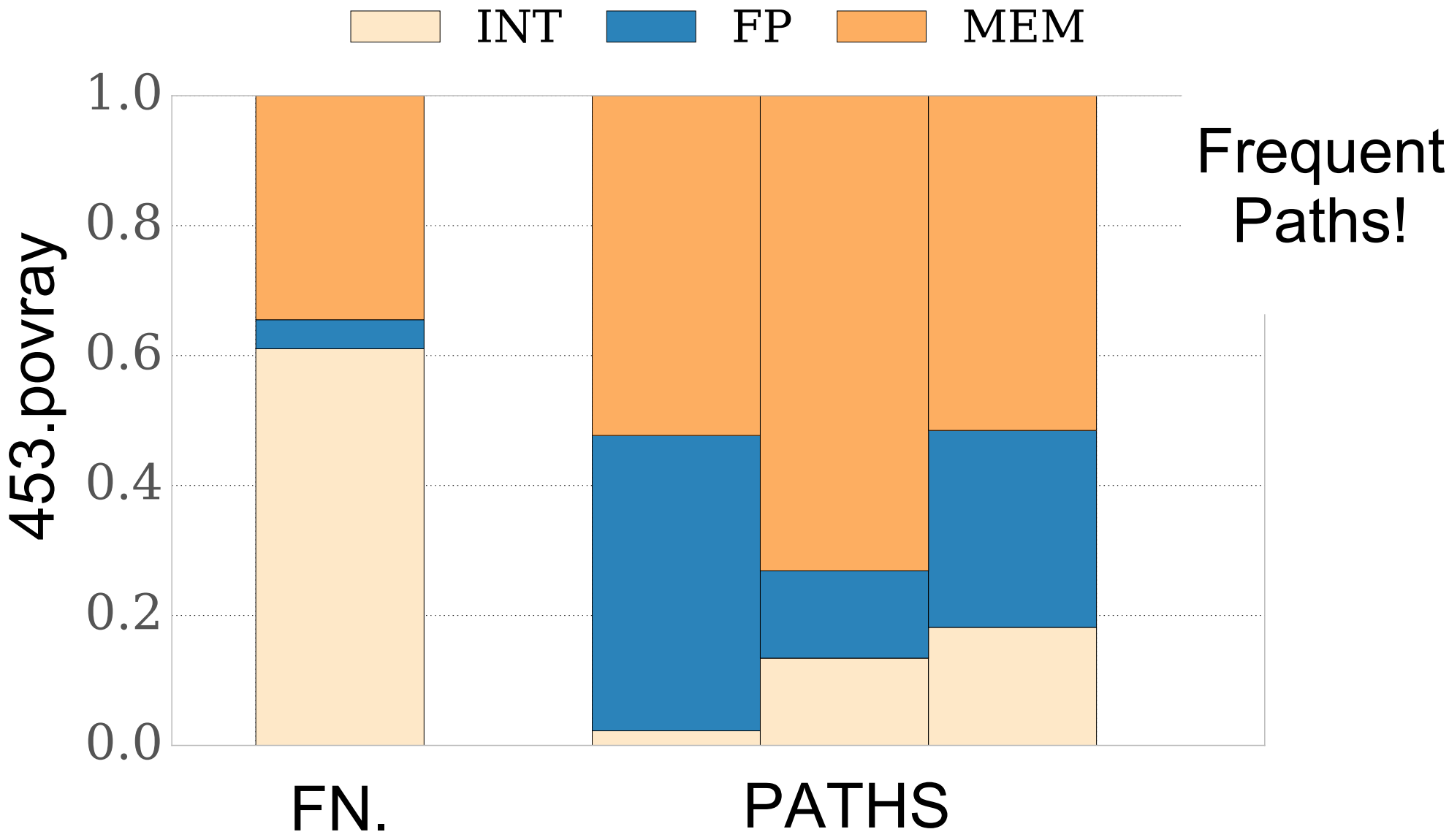


6 workloads more than 95%

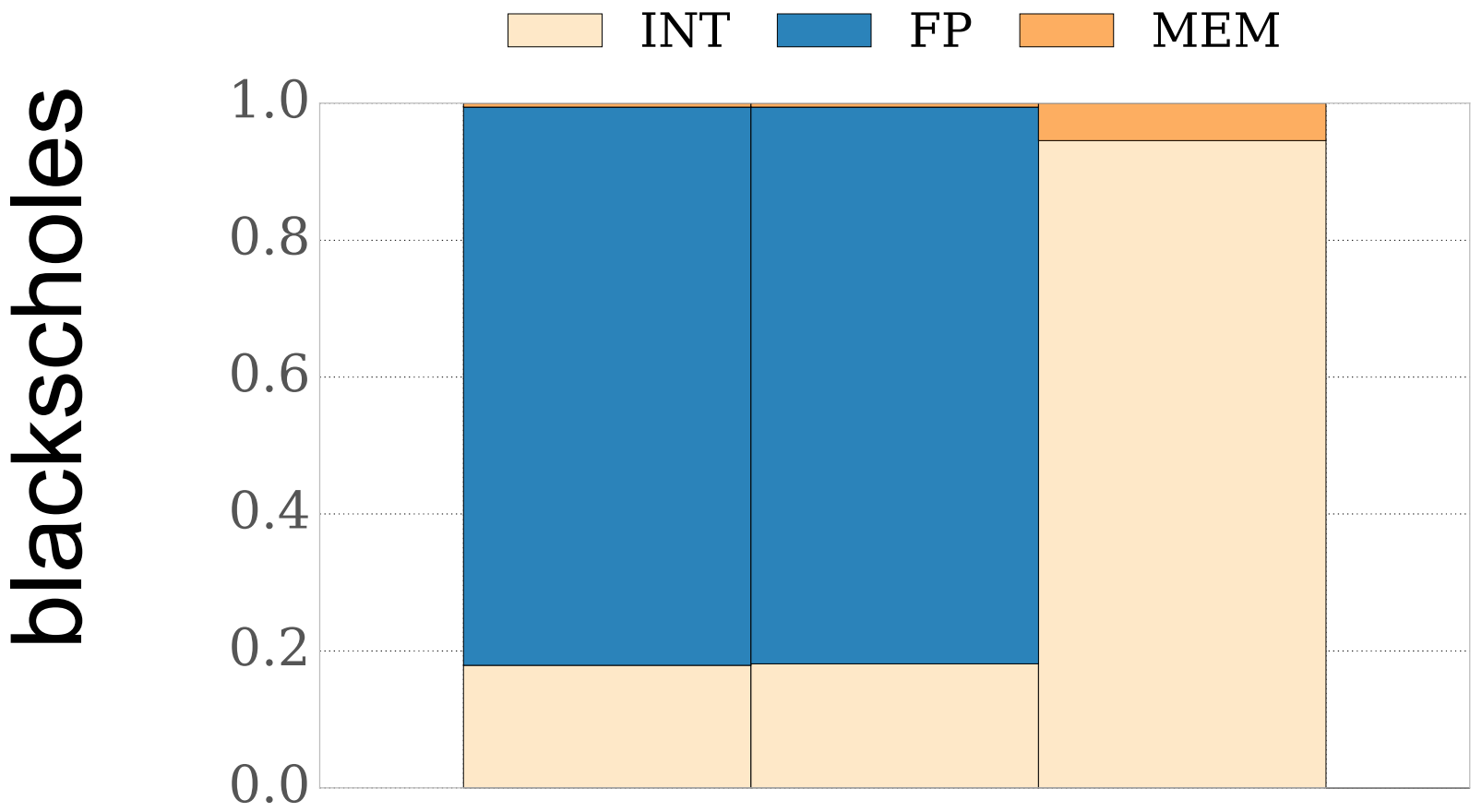
Paths are Specializable



Paths are Specializable

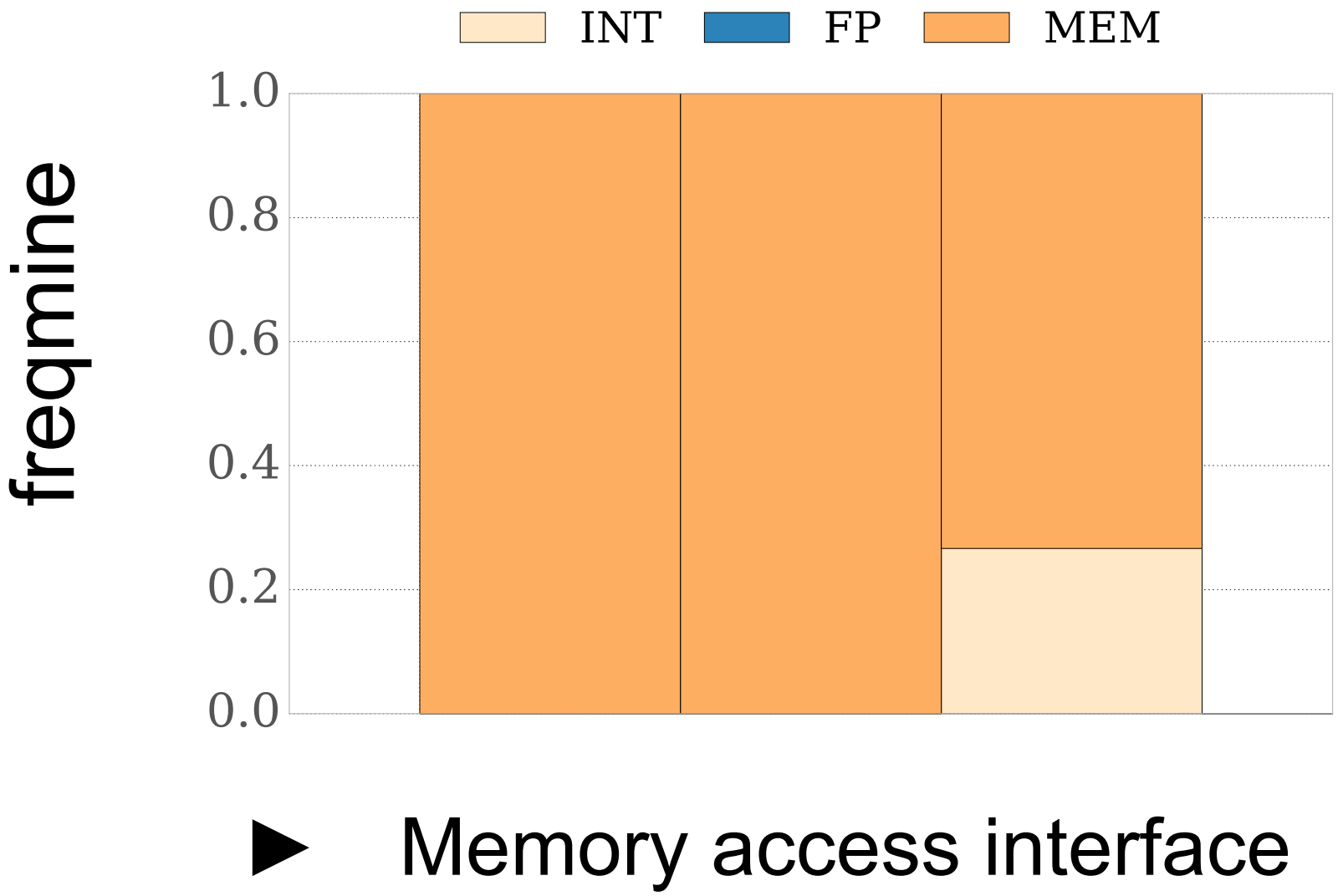


Implications of Variability



- Accelerator micro architecture

Implications of Variability



- Memory access interface

Workloads and Infrastructure

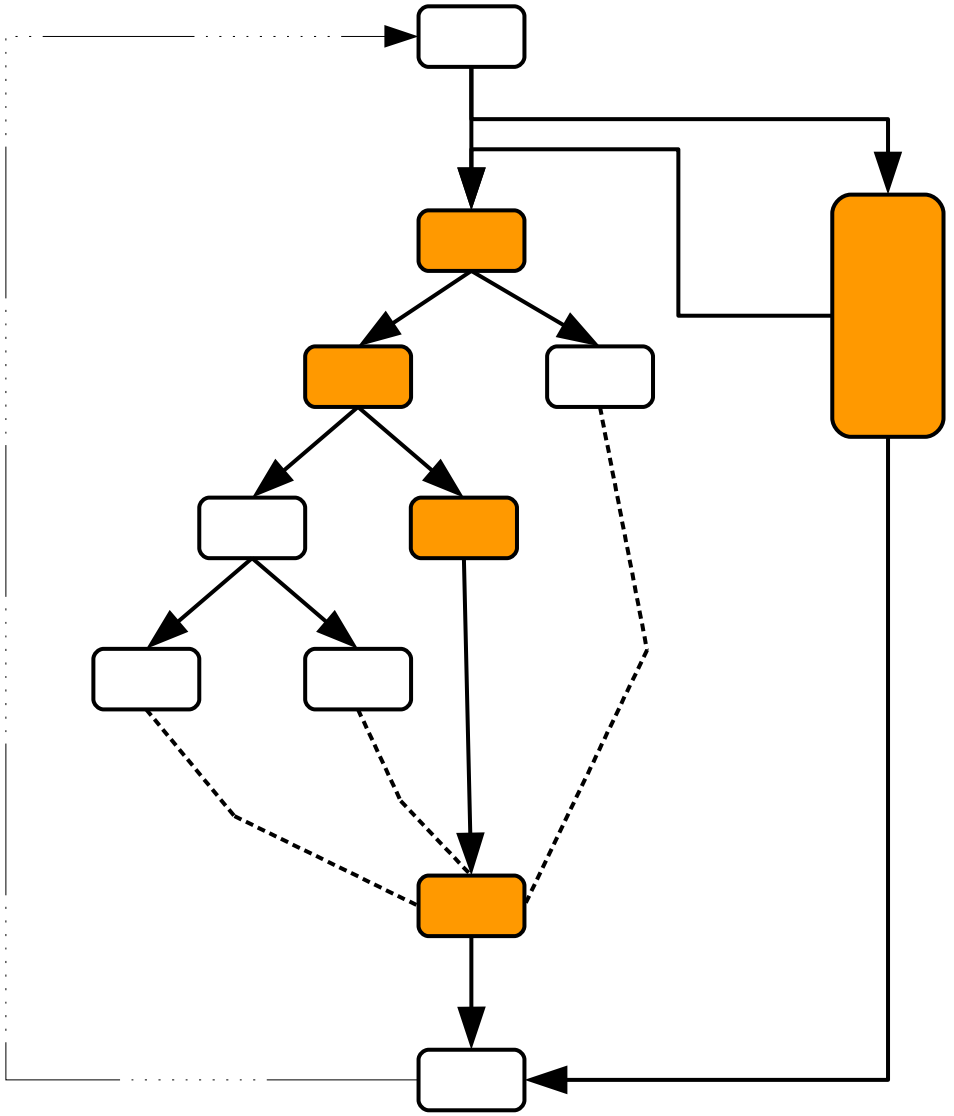
SPEC	2000	8
SPEC	2006	11
PARSEC	3.0	7
PERFECT	1.0	4

Total 29

omit workloads with accelerator unfriendly features
eg. exception handling, setjmp/longjmp

LLVM based toolchain for path identification, extraction, analysis

Outlining Hot Paths



HOT PATH( )

COPY BLOCKS

MODIFY CFG

SIDE EXITS

Path Derived Workload Suite

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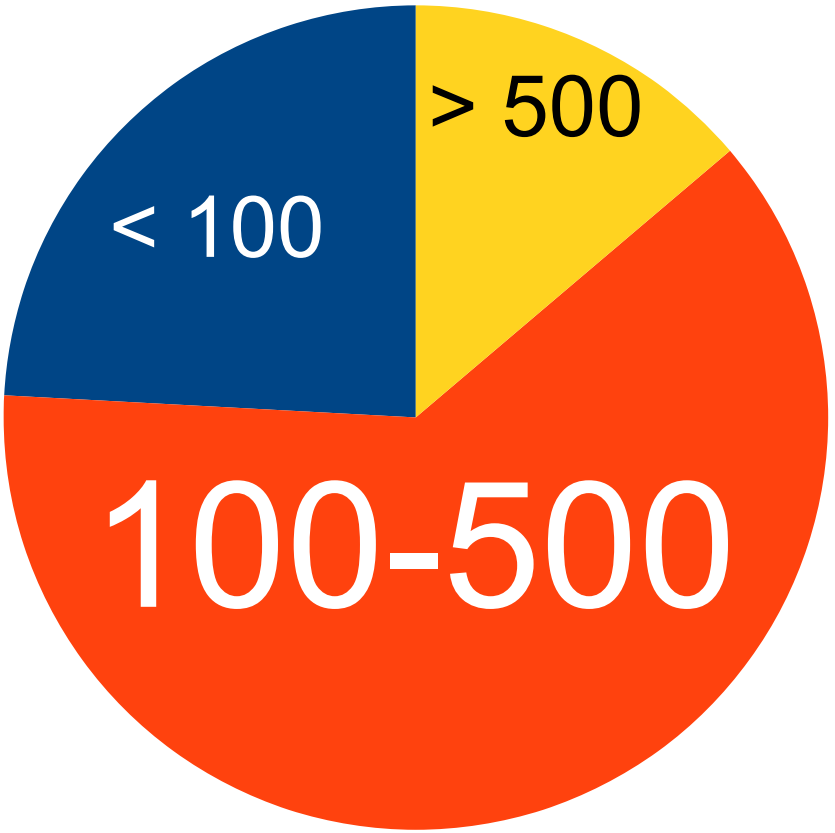
- Dominant behaviour isolated
- LLVM IR format
- Easy to target
  - Static Analysis using LLVM
  - Target Accelerator Codegen
  - Dynamic Analysis Tools (eg. Pin)

Characterization and Implications

Characteristics – What's Important ?

Cov. and Size	▶	More work accelerated
Branches	▶	Control flow
Live Values	▶	State transferred
Opcodes	▶	Types of operations

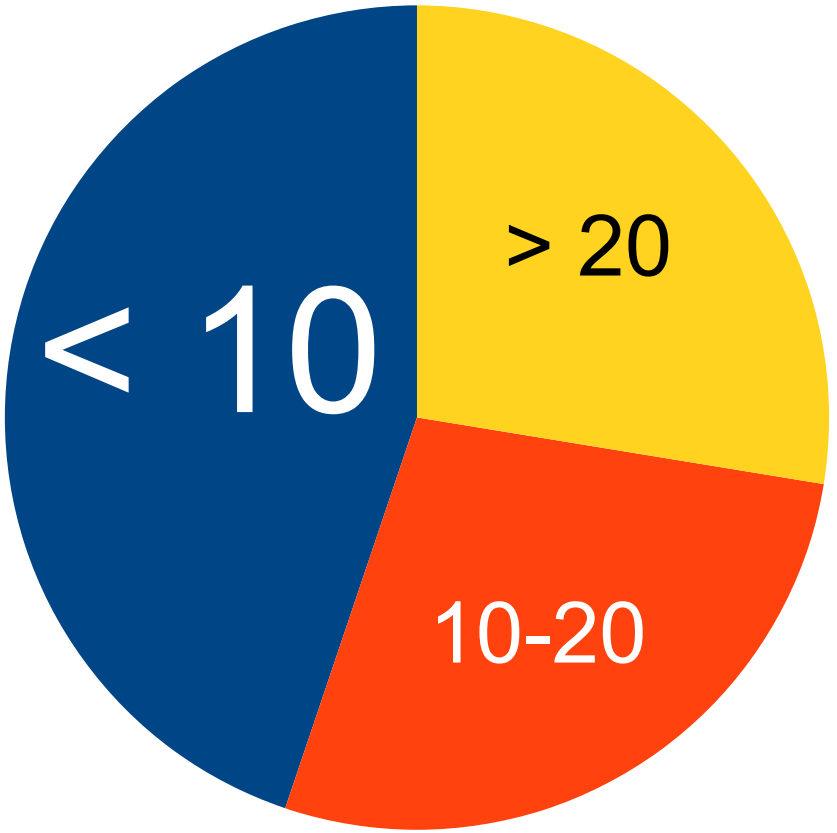
Size ► More work accelerated



Max. Ops

Max : 962
(183.equake)
Median : 232

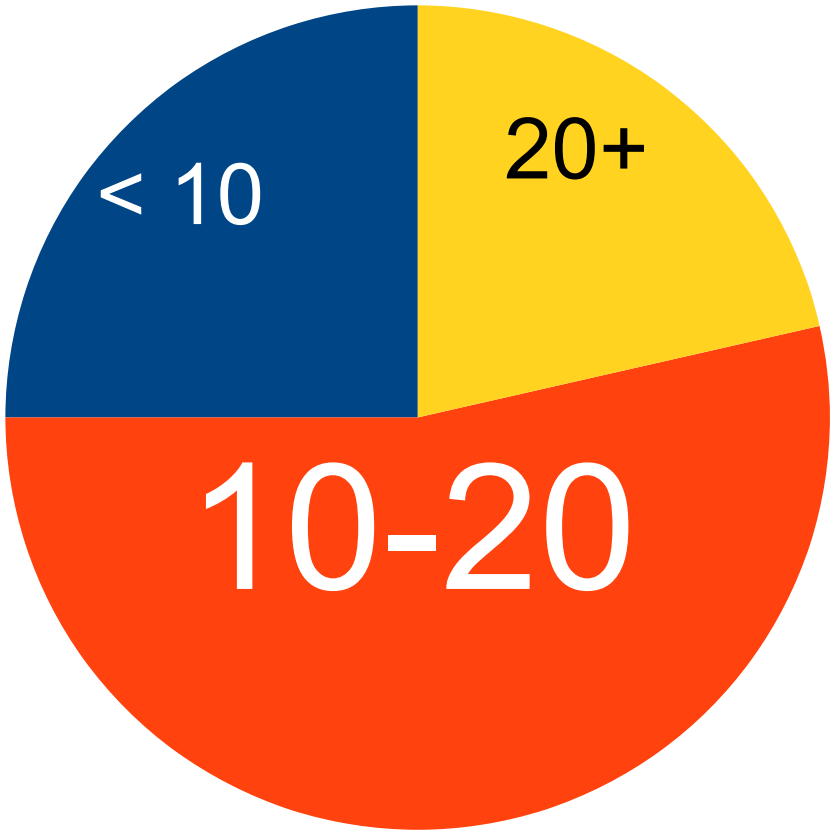
Branches ▶ Control flow



Min. Divergence

Max : 71
(401.bzip2)
Median : 12

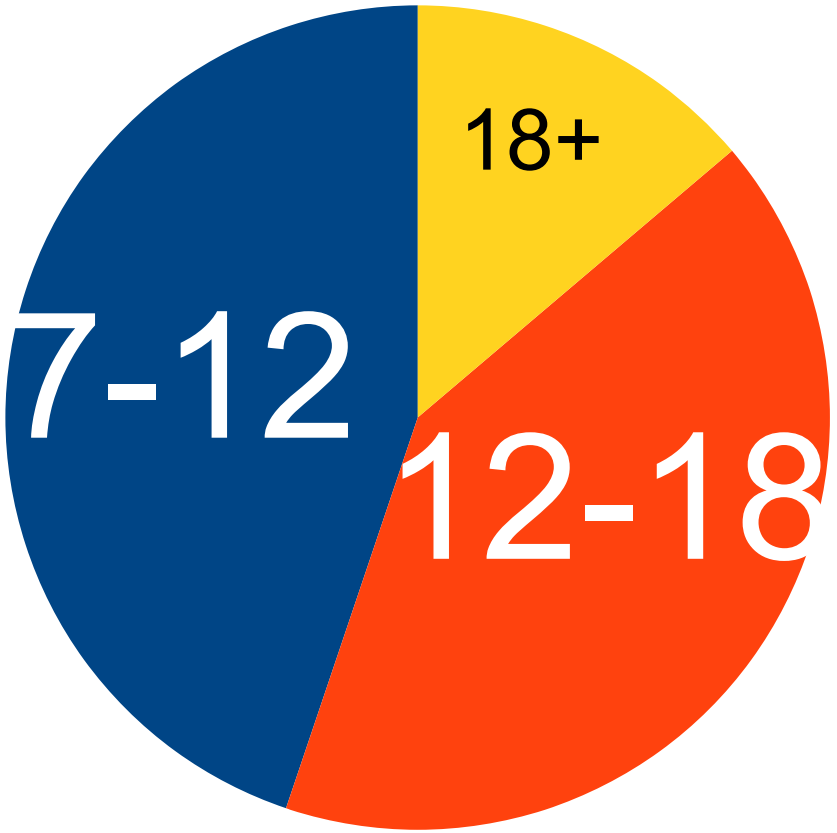
Live Values ▶ State transferred



Min. State

Max : 52
(444.namd)
Median : 15

Opcodes ▶ Types of operations



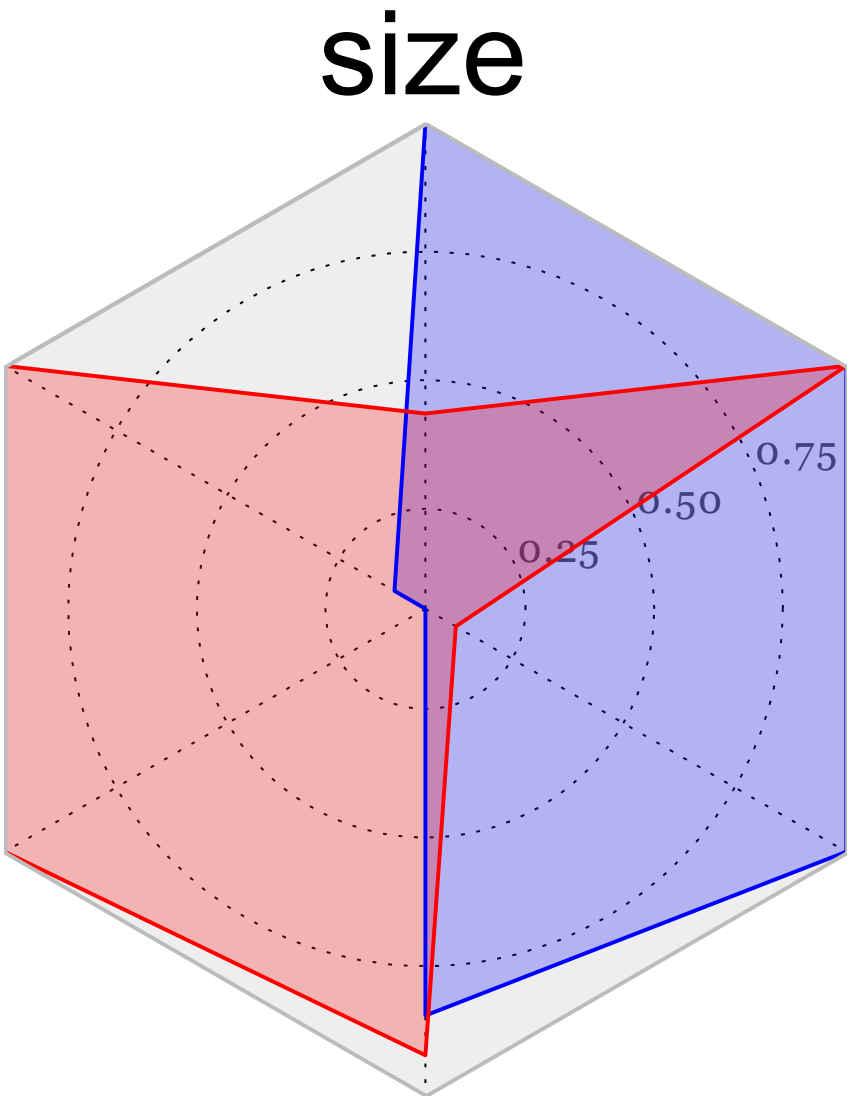
Simple Arch.

Max : 25 (swaptions)
Median : 13

Characteristics – Variability

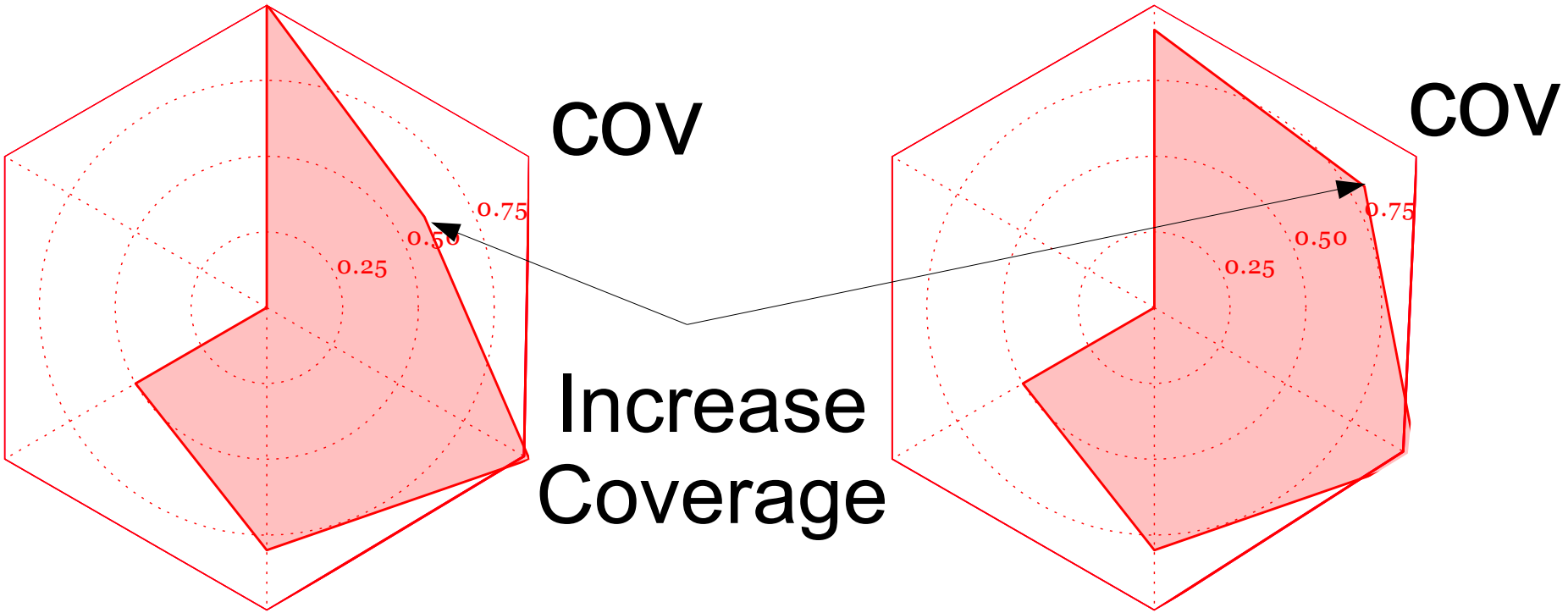
PATH #2

PATH #1



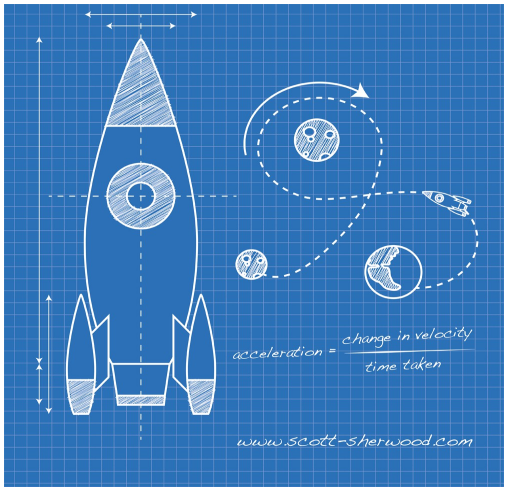
181.mcf ► 429.mcf

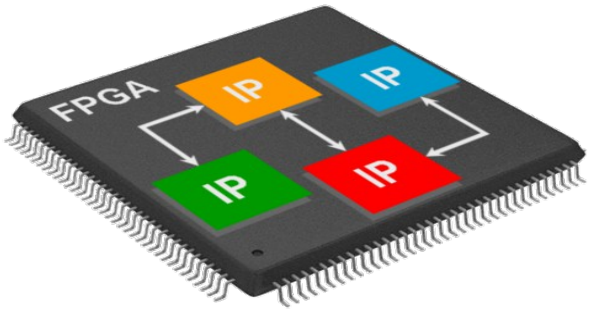
```
realloc condition :

if( net->n_trips <=
MAX_NB_TRIPS_FOR_SMALL_NET ) in implicit.c.
```



Conclusion

SPECAX, PARSECAX





Open Source

sfu-arch.github.io/pdws/

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