LDO Design Approach

We first started by using our MP4 amplifier but then encountered difficulty satisfying the DC line regulation requirement of ≤ 500 μV/V. Using the relationship:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{A_{E0} \cdot \beta}$$

We found that the open-loop gain in our design resulted in a feedback factor $\beta = 1.812$, which is not physically realizable. Since β represents the ratio of the resistive feedback network, it must be strictly less than 1. To resolve this, we replaced our amplifier with the one used in the MP4 solution, which has a higher open-loop gain of approximately 66.7 dB. This correction led to a valid feedback factor of $\beta = 0.94$.

At first, the design did not satisfy the load regulation constraint of ≤ 50 μV/mA. This can be understood from the expression:

$$R_{\text{out}} = \frac{r_{\text{dsp}}}{1 + T_0}$$

where r_{dsp} is the output resistance of the pass transistor and T_0 is the loop gain. To improve the load regulation, we increased g_{mp} by increasing the size of the pass transistor. Specifically, we set the channel length to $L = 180$ nm and chose the width as $W = 12,500 \times L$. This sizing allowed us to meet the load regulation requirement.

After resizing the pass transistor to improve load regulation, the phase margin requirement was no longer met. To address this, we adjusted the feedback resistor network. We initially selected $R_1 = 1$ kΩ, but a sweep of the feedback resistor values revealed that reducing R_1 to 10 Ω improved stability and restored adequate phase margin. Given the target output voltage, this change corresponded to a value of approximately $R_2 = 167$ Ω. With these updated values, the LDO met the phase margin specification.

We observed that our LDO stopped functioning as intended when the input voltage dropped below 1.7 V. This limitation also resulted in the failure to meet the line regulation specification below this voltage. Although we attempted to address the issue by modifying the biasing network and achieved some improvement, we were ultimately unable to meet the line regulation requirement for input voltages below 1.68 V. However, the LDO successfully met the line regulation specification within the input voltage range of 1.68 V to 1.98 V.

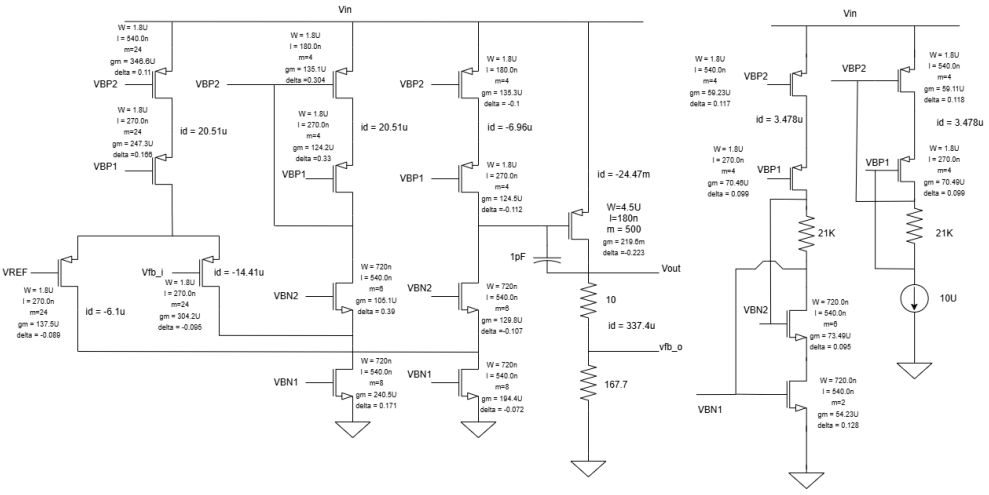

Figure 1: amplifier schematic

Performance Summary

Table 1: Performance summary

Design parameter/variable	Simulated performance	Specification
Input voltage	$1.7 - 1.98$V	$1.8\text{V} \pm 10\%$
Output voltage	$1.0\text{V} - 1.4\text{V}$	$1.0\text{V} - 1.4\text{V}$
Load current	$1\text{mA} - 25\text{mA}$	$1\text{mA} - 25\text{mA}$
DC load regulation	$35.7\mu\text{V/mA}$	$\leq 50\mu\text{V/mA}$
DC line regulation	$392\mu\text{V/V}$	$\leq 500\mu\text{V/V}$
Quiescent current ($\text{I}_\text{L} = 1\text{mA}/\text{I}_\text{L} = 25\text{mA}$)	$\text{I}_\text{q} = 1\text{mA}/\text{I}_\text{q} = 0.38\text{mA}$	Minimum
DC loop gain ($\text{I}_\text{L} = 1\text{mA}/\text{I}_\text{L} = 25\text{mA}$)	$68.85dB/63.46dB$	–
Loop-gain unity gain frequency ($\text{I}_\text{L} = 1\text{mA}/\text{I}_\text{L} = 25\text{mA}$)	$3.35MHz/3.12MHz$	–
Loop-gain phase margin($\text{I}_\text{L} = 1\text{mA}/\text{I}_\text{L} = 25\text{mA}$)	$76.18°/91.08°$	–
Loop-gain gain margin ($\text{I}_\text{L} = 1\text{mA}/\text{I}_\text{L} = 25\text{mA}$)	$30.85dB/32.33dB$	–

Loop-gain AC Response

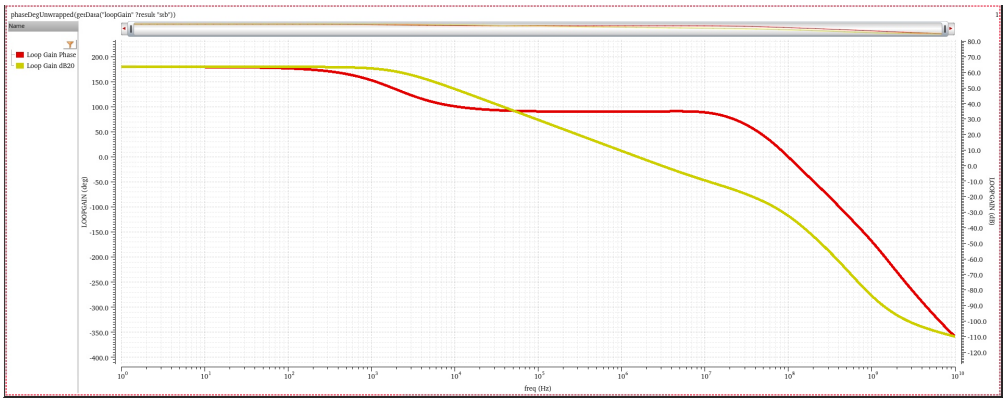

Figure 2: Loop-gain AC response (magnitude and phase) with clearly marked DC gain, loop-gain bandwidth, and phase- and gain-margins for minimum and maximum load currents.

DC Load and Line Regulation Response

Figure 3: DC line regulation response plots. Ratio of the dy's shown in plots give LR.

Here, from these differences, we see our LR = 392 uV/V. Again this is only true for our line regulation range of 1.7-1.98 V.

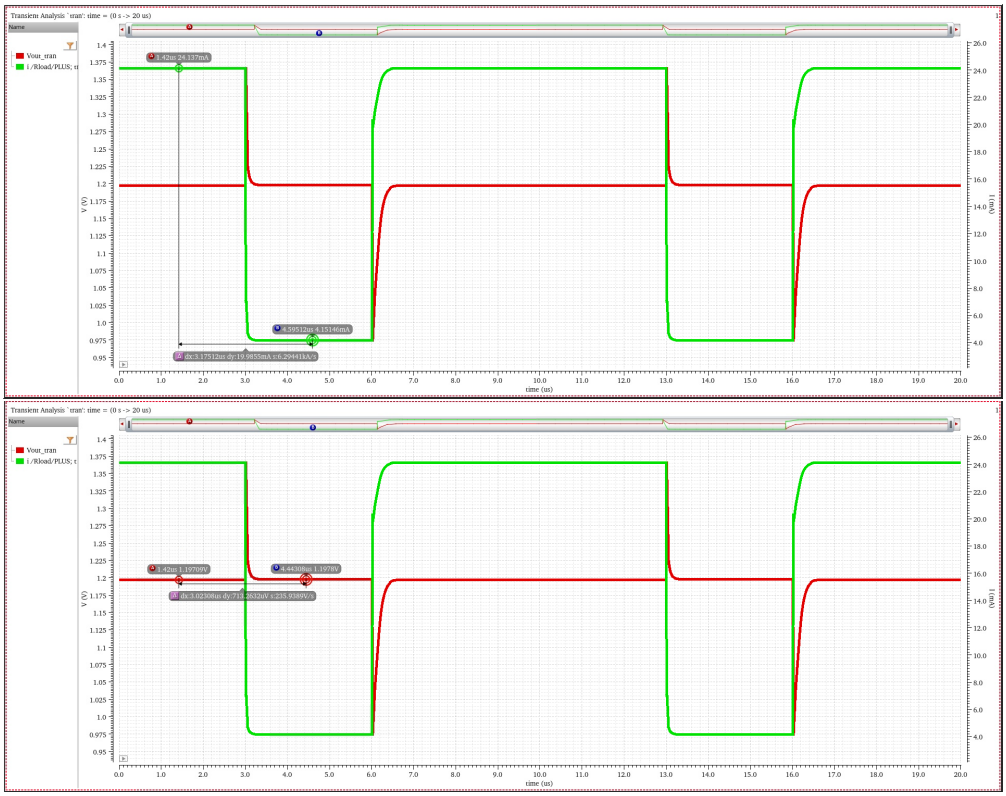

Figure 4: DC load regulation response plots. Ratio of the dy's shown in plots give LDR.

Here, from these differences, we see our LDR = 35.7 uV/mA.