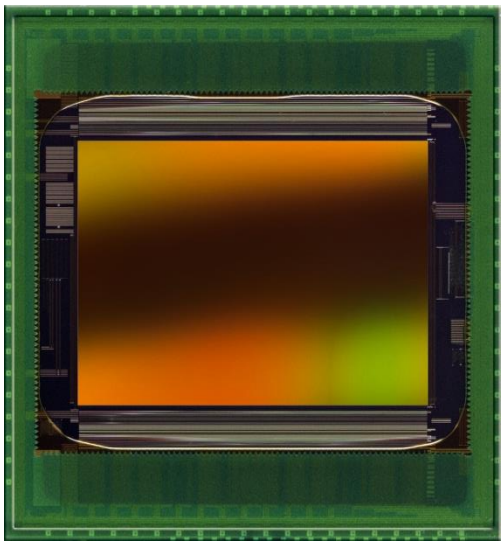
VGA resolution CMOS image sensor

Datasheet



Change record

Issue	Date	Modification
1	13/04/2011	Origination
1.1	5/8/2011	Update after tape out
1.2	20/10/2011	Update after samples test and debug
1.3	25/4/2012	Updated maximum output rate from 600Mbps to 300 Mbps
1.4	22/08/2012	Updated recommended register values Added Spectral Response and QE graphs
1.5	28/09/2012	Updated recommended register values Updated supply settings
1.6	19/12/2012	Removed Draft status Updated Part Numbers
1.7	8/1/2012	Updated VDD18 range
2.0	05/06/2013	Updated: - maximum output rate from 300Mbps to 480Mbps - Full Well Charge: 20ke$^-$ - Conversion factor: 0.2LSB/e$^-$ - Dynamic range: 60dB - Dark current: 125e$^-$/s - Total power: 700mW - VDDPIX: 3.3V - VDD18 renamed to VDD20 - Supply settings - FOT calculation and value - Piecewise Linear Response details - PLR external mode pulse requirements - Bit mode details - Recommended registers Added: - Temperature sensor formulas and graphs - Output skew - Control channel test pin (Test3) programming - Disable PLL - Actual exposure calculations - ADC vs actual gain - Detailed frame cycle timing
V2.1	03/07/2013	Updated: - Detailed frame cycle timing - Exposure calculation

Disclaimer

This is a preliminary datasheet. CMOSIS reserves the right to change the product, specification and other information contained in this document without notice. Although CMOSIS does its best efforts to provide correct information, this is not warranted.

Table of Contents

1 INTRODUCTION

1.1 OVERVIEW

The CMV300 is a high speed CMOS image sensor with 648 by 488 pixels (1/3 optical inch) developed for machine vision applications. The image array consists of 7.4µm x 7.4µm pipelined global shutter pixels which allow exposure during read out, while performing CDS operation. The image sensor has 4 8, 10 or 12 bit digital LVDS outputs (serial) or one 10 bit parallel CMOS output. The image sensor also integrates a programmable gain amplifier and offset regulation. Each LVDS channel runs at 300 Mbps maximum which results in 300 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.2 FEATURES

- 648 * 488 active pixels on a 7.4µm pitch
- 8 Dark reference and dummy rows and columns
- Frame rate 480 frames/sec @ 640 * 480 resolution
- Row windowing capability
- X-Y mirroring function
- Master clock: 10-40MHz
- 4 LVDS-outputs @ 480Mbit/s (480 fps) multiplexable to 2 (240fps) and 1 (120 fps) outputs
- One 10 bit parallel CMOS output running at maximum 40 MHz (120 fps)
- LVDS control line with frame and line information
- LVDS DDR output clock to sample data on the receiving end
- 12 bit ADC output at maximum frame rate
- Multiple High Dynamic Range modes supported
- On chip temperature sensor
- On chip timing generation
- On chip black reference
- SPI-control
- Chip scale package (8 x 8 BGA pins)
- 3.3V and 2.2V signaling
- Available in panchromatic and Bayer (RGB)

1.3 SPECIFICATIONS

- Full well charge: 20Ke$^-$
- Sensitivity: 6 V/lux.s (with microlenses)
- Dark noise: 20e$^-$ RMS
- Conversion factor: 0.2LSB/e$^-$ (12 bit mode) at recommended gain
- Dynamic range: 60 dB
- Extended dynamic range: piecewise linear response or interleaved read-out
- Parasitic light sensitivity: 1/50 000
- Dark current: 120 e/s (@ 25C die temperature)
- Fixed pattern noise: <4 LSB (12 bit mode, <0.1% of full swing, standard deviation on full image)
- Power consumption: 700mW

1.4 CONNECTION DIAGRAM

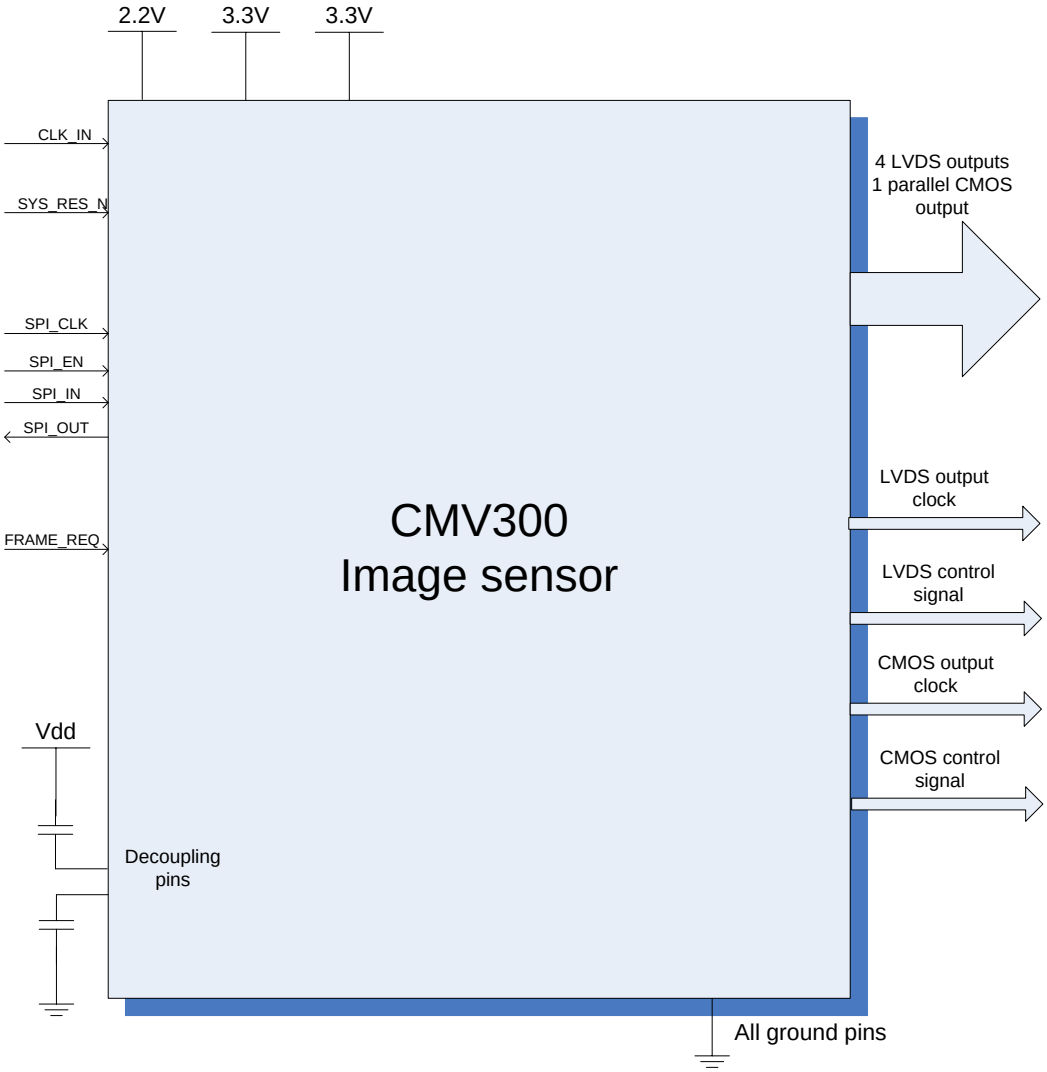


FIGURE 1: CONNECTION DIAGRAM FOR THE CMV300 IMAGE SENSOR

Please look at the pin list for a detailed description of all pins and their proper connections. Some optional pins are not displayed on the figure above. The exact pin numbers can be found in the pin list and on the package drawing.

2 SENSOR ARCHITECTURE

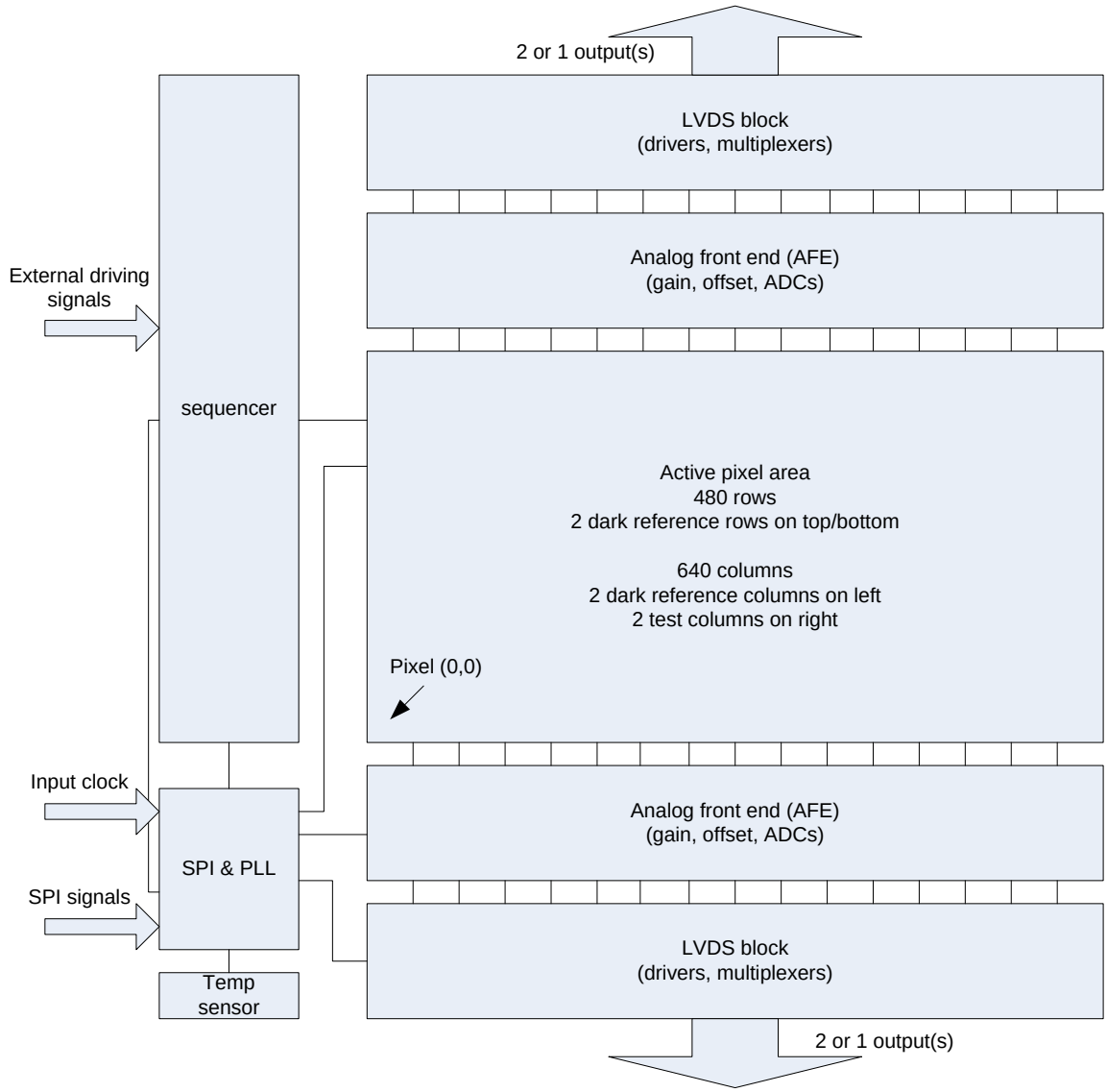


FIGURE 2: SENSOR BLOCK DIAGRAM

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels or one parallel CMOS output. Each LVDS channel reads out 324 adjacent columns of the array. Two rows are being read out at the same time when 4 LVDS channels are used. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

2.1 PIXEL ARRAY

The pixel array consists of 648 x 488 square global shutter pixels with a pitch of 7.4µm (7.4µm x 7.4µm). The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%). There are 4 dark reference rows available on the sensor (rows 0, 1, 486 and 487) and 2 dark reference columns (column 0 and 1). Columns 646 and 647 are test

columns and do not contain useful image data. This means that the useable image data area is 644 x 484. This results in an optical area of 1/3 optical inch (5.9 mm). This means that off-the-shelf C-mount lenses can be used.

2.2 ANALOG FRONT END

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 12 bit value. A digital offset can also be applied to the output of the column ADC's. All gain and offset settings can be programmed using the SPI interface.

2.3 LVDS BLOCK

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 300Mbps. The sensor has 6 LVDS output pairs:

- 4 Data channels
- 1 Control channel
- 1 Clock channel

The 4 data channels are used to transfer 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in section 4 of this document.

2.4 PARALLEL CMOS OUTPUT BLOCK

The parallel CMOS block sends the digital data coming from the column ADC to a standard 1.8V CMOS parallel output running at maximum 25MHz. The parallel output has 13 pins:

- 10 Data channels
- 2 Control channels
- 1 Clock channel

The 10 data channels are used to transfer 10-bit pixel data from the sensor to a receiver. The output clock channel transports a clock, synchronous to the data on the data channels. This clock can be used at the receiving end to sample the data. The data on the control channels contains status information on the validity of the data on the data channels (LVAL, DVAL). Details on the parallel CMOS timing and format can be found in section 4 of this document.

2.5 SEQUENCER

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in section 5 of this document.

2.6 SPI INTERFACE

The SPI interface is used to load the sequencer registers with data. The data in these registers is used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Section 5 contains more details on register programming.

2.7 TEMPERATURE SENSOR

A 16-bit digital temperature sensor is included in the image sensor and can be read out through the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 78 and 79 (in burst mode, see section 3.9.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements. A typical temperature sensor output vs. temperature curve can be found below. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode.

A typical value of the sensor at 0°C is about $\frac{f[MHz]}{25} * 4900$ DN. A typical slope will be around $\frac{f[MHz]}{25} * 13$ DN/°C. A sensor will typically heat up about 15°C above ambient temperature.

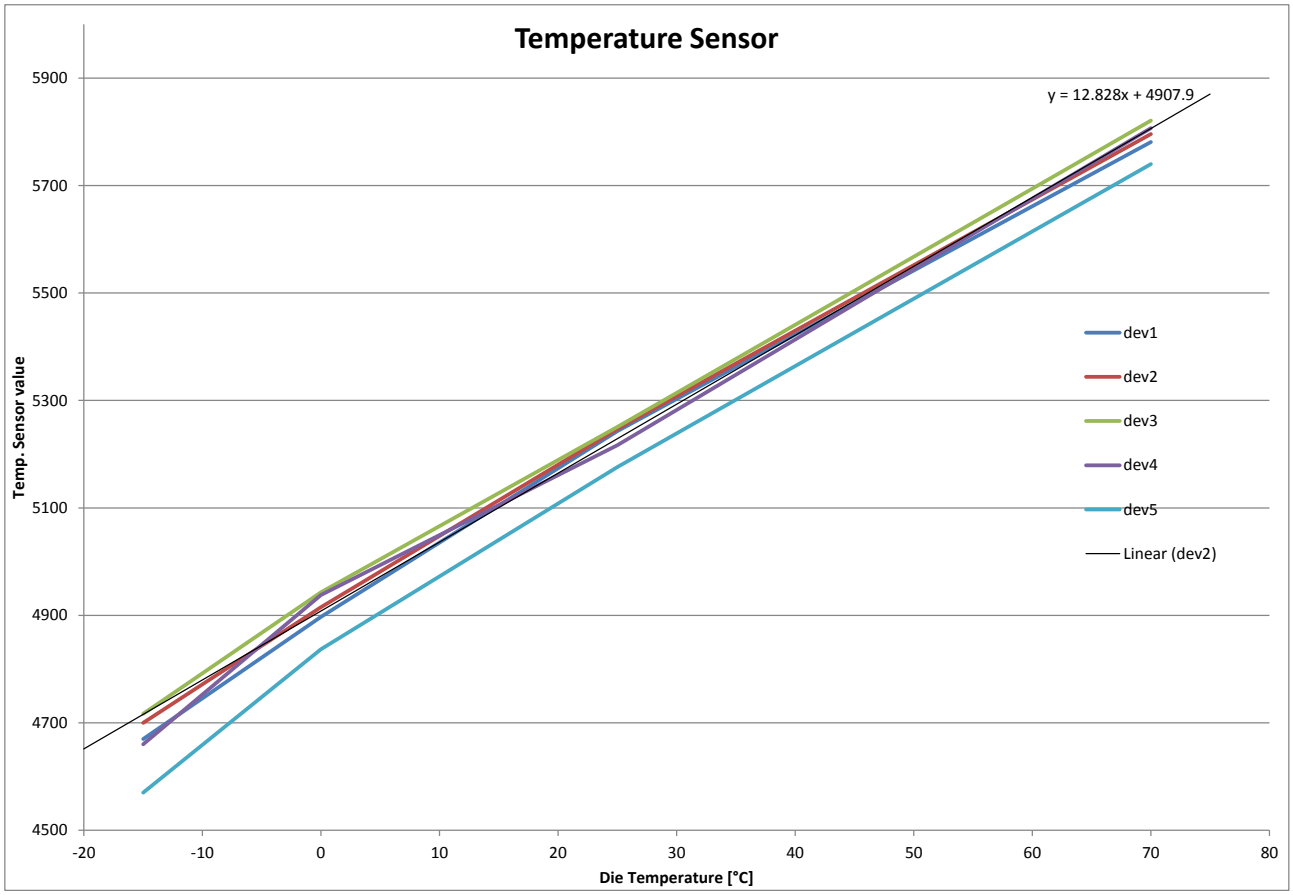


FIGURE 3: TYPICAL OUTPUT OF THE TEMPERATURE SENSOR OF SEVERAL CMV300 SENSORS @ 25MHZ

3 DRIVING THE CMV300

3.1 SUPPLY SETTINGS

The CMV300 image sensor has the following supply settings:

Supply name	Usage	Recommended value	Maximum Ratings	DC Current Idle	DC Current Nom.	DC Current Max.
VDD20	LVDS, ADC	2.2V	1.8V-2.2V	175mA	220mA	270mA
VDD33	Dig. I/O. SPI, ADC	3.3V	3V-3.6V	25mA	30mA	30mA
VDDpix	Pixel array supply	3.3V	2.3V-3.6V	1mA	5mA	5mA
			Total DC Power	470mW	600mW	710mW

See pin list for exact pin numbers for every supply.

The maximum currents will be reached during readout. The current of the VDD20 supply depends on the average value of the image (a pure white image will draw 270mA). Idle is when the sensor is idle (not reading out or integrating) and nominal is a 50% grey average image. These values are for a sensor running at 40MHz. The power consumption decreases with the clock speed albeit little.

Besides these DC currents, decoupling should be foreseen to suppress current spikes. VDDPIX can generate current spikes up to 500mA during FOT. Because this supply is the pixel array supply, the voltage should be as noise-free as possible, because noise can ripple through to the image. We propose to use 5x 100nF capacitors on each supply as close to the sensor as possible.

3.2 BIASING

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

3.3 DIGITAL INPUT PINS

The table below gives an overview of the external pins used to drive the sensor.

Pin name	Description
CLK_IN	Master input clock, frequency range between 10 and 40 MHz
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up
FRAME_REQ	Frame request pin. This signal should be at least one period of CLK_IN long to assure detection.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI
SPI_CLK	SPI clock. This is the clock on which the SPI runs (max 40Mz)

Pin name	Description
T_EXP1	Input pin which can be used to program the exposure time externally. This signal should be at least one period of CLK_IN long to assure detection.
T_EXP2	Input pin which can be used to program the exposure time externally in interleaved high dynamic range mode. This signal should be at least one period of CLK_IN long to assure detection.

3.4 ELECTRICAL IO SPECIFICATIONS

3.4.1 DIGITAL IO CMOS/TTL DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3V I_{OH}=-2mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3V I_{OL}=2mA			0.4	V

3.4.2 PARALLEL CMOS OUTPUT DC SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OH}	High level output voltage	VDD=1.8V I_{OH}=-2mA	1.6			V
V_{OL}	Low level output voltage	VDD=1.8V I_{OL}=2mA			0.2	V

3.4.3 LVDS RECEIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN}$=1.2V±50mV, 0≤ $V_{INP\|INN}$≤2.4V			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA

3.4.4 LVDS DRIVER SPECIFICATIONS

Parameter	Description	Conditions	min	typ	max	Units
V_{OD}	Differential output voltage	Steady State, RL = 100Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100Ω			50	mV
V_{OC}	Common mode voltage	Steady State, RL = 100Ω	1.125	1.25	1.375	V

Parameter	Description	Conditions	min	typ	max	Units
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	V_{OUTP}=V_{OUTN}=GND			24	mA
$I_{OS,PN}$	Output short circuit current	V_{OUTP}=V_{OUTN}			12	mA

3.5 INPUT CLOCK

The input clock (CLK_IN) defines the output data rate of the CMV300. The master clock (CLK_IN) is 12 times slower than the output date rate. The maximum data rate of the output is 480Mbps which results in a CLK_IN of 40MHz. The minimum frequency is 10MHz for CLK_IN. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate. The SPI register with address 83 must be programmed to the correct frequency range when the CLK_IN frequency is changed.

3.6 FRAME RATE CALCULATION

The frame rate of the CMV300 is defined by 2 main factors.

1. Exposure time
2. Read out time

For ease of use we will assume that the exposure time is no longer than the read out time. By assuming this the frame rate is completely defined by the read out time (because the exposure time happens in parallel with the read-out time). The read-out time (and thus the frame rate) is defined by:

1. Output clock speed: max 480Mbps
2. Number of lines read-out
3. Number of outputs used: max 4 LVDS outputs (2 on the top and 2 on the bottom) or one parallel CMOS output

This means that if any of the parameters above is changed, it will have an impact on the frame rate of the CMV300. In normal operation (4 outputs @ 480Mbps, 12 bit and full resolution) this will result in 480 fps.

Total readout time is composed of two parts: FOT (frame overhead time) + image readout time.

$$FOT = \left(\frac{4}{\#\ bottom\ outputs\ used} + \frac{reg58}{4}\right) * 325 * clk\_per$$

With clk_per being equal to one period of CLK_IN and reg58 should be a multiple of 4.
==> When running the CMV300 sensor at 40MHz with 4 outputs and recommended FOT settings this results in: 97.5us

$$Readout\ time = line\ time * \frac{\#\ lines}{\#\ sides\ used}$$

$$Line\ time = \frac{2 * 325 * clk\_per}{\#\ bottom\ outputs\ used}$$

When running the CMV300 sensor at 40MHz with 4 outputs and reading 480 lines this results in: 1950µs
This results in a total read-out time of 97.5us + 1966.25µs = 2.08ms ==> 484.5fps for 640 * 480 resolution.

3.7 START-UP SEQUENCE

The following sequence should be followed when the CMV300 is started up in default output mode (300Mbps, 12bit resolution).

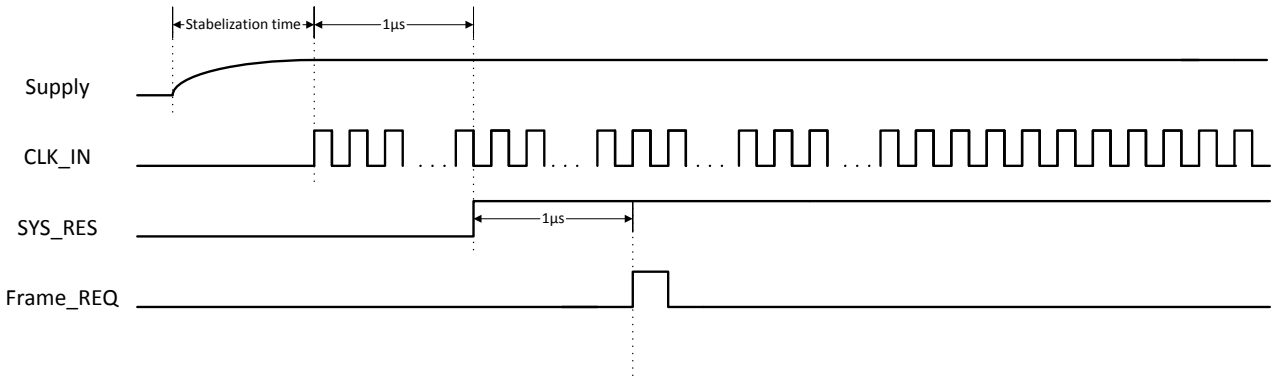


FIGURE 4: START-UP SEQUENCE FOR 300MBPS @ 12-BIT

The master clock (25MHz for 300Mbps in 12-bit mode) should only start after the supplies are stable. The external reset pin should be released at least 1µs after the supplies have become stable. The first frame can be requested 1µs after the reset pin has been released. An optional SPI upload (to program the sequencer) is possible 1µs after the reset pin has been released. In this case the FRAME_REQ pulse must be postponed until after the SPI upload has been completed.

When the CMV300 will be used in 8 or 10-bit mode or at another speed than 300mbps, an SPI upload is necessary to program the sensor. In this case the start-up sequence looks like the diagram below. A PLL lock-time of 1ms should be considered after uploading the register settings and before sending the FRAME_REQ pulse.

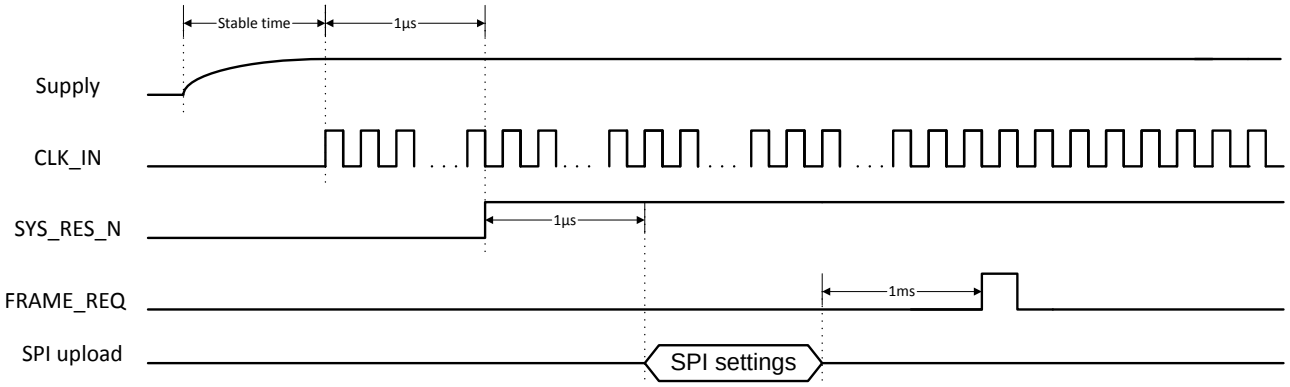


FIGURE 5: START-UP SEQUENCE FOR 8 OR 10 BIT MODE OR ANOTHER SPEED

The following SPI registers should be uploaded in this mode:

1. Bit mode settings (address 68) : set to 8 or 10 bit mode
2. PLL settings (address 83): set to correct PLL range

3.8 RESET SEQUENCE

If a sensor reset is necessary while the sensor is running the following sequence should be followed.

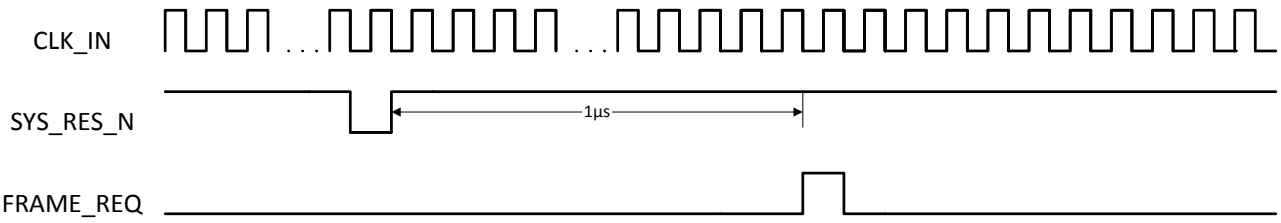


FIGURE 6: RESET SEQUENCE

The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. After the reset there is a minimum time of 1µs needed before a FRAME_REQ pulse can be sent. When a lower clock speed is desired while the sensor is running the reset sequence should be executed. In this case it must be followed by a SPI upload to program the sensor for this lower clock speed.

3.9 SPI PROGRAMMING

Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

3.9.1 SPI WRITE

The timing to write data over the SPI interface can be found below.

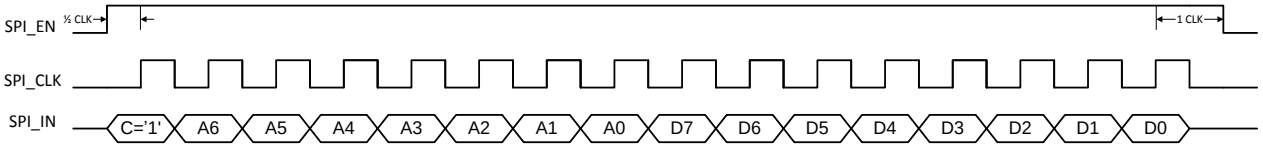


FIGURE 7: SPI WRITE TIMING

The data is sampled by the CMV300 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 40MHz. The SPI_EN signal has to be high for half a clock period before the first databit is sampled. SPI_EN has to remain high for 1 clock period after the last databit is sampled. The sampled data will be written in the sequencer on the last falling clock edge, so SPI_CLK has to go low again at the end for the write operation to be successful.

One write action contains 16 databits:

- One control bit: First bit to be sent, indicates whether a read (‘0’) or write (‘1’) will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The data is written MSB first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the figure below for an example of 2 registers being written in burst.

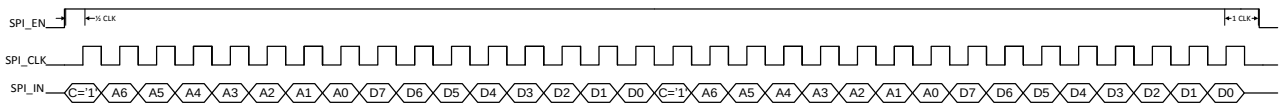


FIGURE 8: SPI WRITE TIMING FOR 2 REGISTERS IN BURST

3.9.2 SPI READ

The timing to read data from the registers over the SPI interface can be found below.

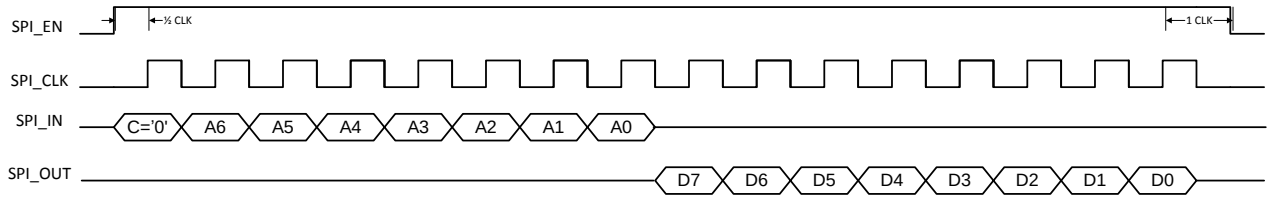


FIGURE 9: SPI READ TIMING

To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made '0'. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 78 and 79 should be read out in burst mode (keep SPI_EN high).

3.10 REQUESTING A FRAME

After starting up the sensor (see section 3.7), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 55 and 56). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the sections below.

3.10.1 INTERNAL EXPOSURE CONTROL

In this mode, the exposure time is set by programming the appropriate registers (address 42-44) of the CMV300.

After the high state of the FRAME_REQ pulse is detected, the exposure time will start immediately. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). After the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one (pipeline mode). See the diagram below for more details.

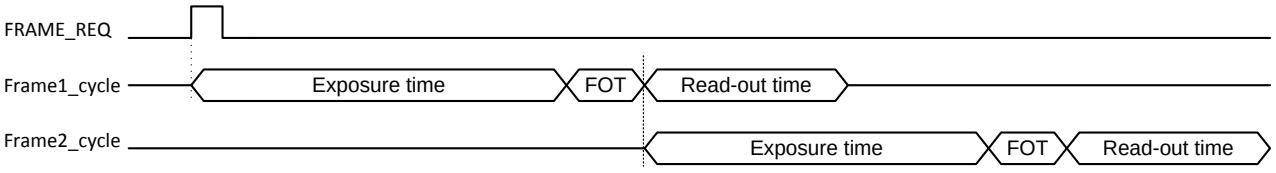


FIGURE 10: REQUEST FOR 2 FRAMES IN INTERNAL- EXPOSURE-TIME MODE

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame.

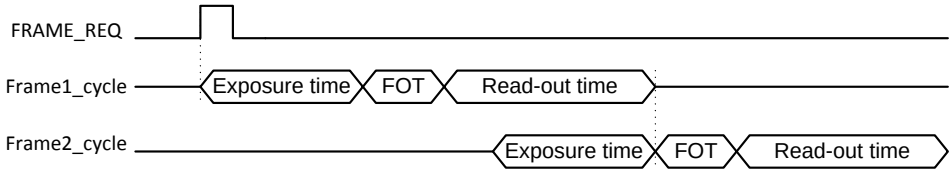


FIGURE 11: REQUEST FOR 2 FRAMES IN INTERNAL-EXPOSURE-TIME MODE WITH EXPOSURE TIME < READ-OUT TIME

3.10.2 EXTERNAL EXPOSURE CONTROL

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame.

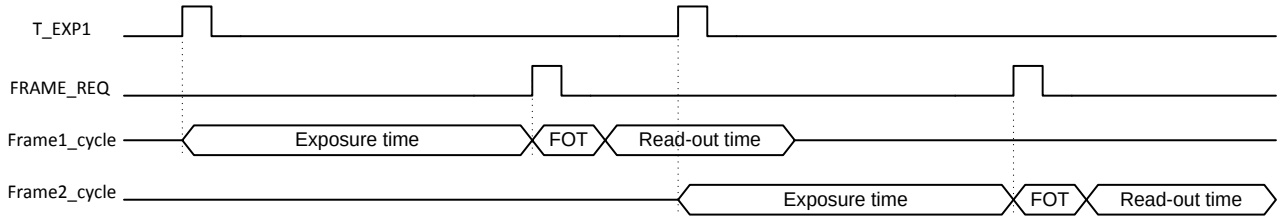


FIGURE 12: REQUEST FOR 2 FRAMES USING EXTERNAL-EXPOSURE-TIME MODE

4 READING OUT THE SENSOR

When reading out the CMV300, the user has a choice to use 4 LVDS outputs (max 480fps) or 1 parallel CMOS output (max 120 fps). This choice is made by connecting pin B2 to VDD33 (LVDS outputs) or GND (parallel CMOS output).

4.1 LVDS DATA OUTPUTS

The CMV300 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 4 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 6 LVDS output pairs (2 pins for each LVDS channel):

- 4 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 12 pins of the CMV300 are used for the LVDS outputs (8 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs. The 4 data channels are used to transfer the 12-bit, 10-bit or 8-bit pixel data from the sensor to the receiver in the surrounding system. The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480Mbps output data rate is used, the LVDS output clock will be 240MHz. The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 12-bit words that are transferred synchronous to the 4 data channels.

4.1.1 LVDS LOW-LEVEL PIXEL TIMING

The figures below show the timing for transfer of 8-bit, 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred LSB first, with the transfer of bit D[0] during the high phase of the DDR output clock.

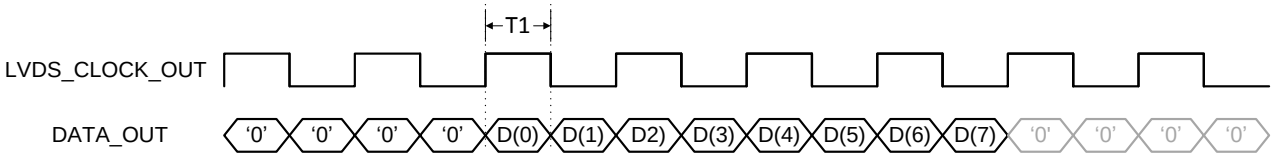


FIGURE 13: 8-BIT PIXEL DATA ON AN LVDS CHANNEL

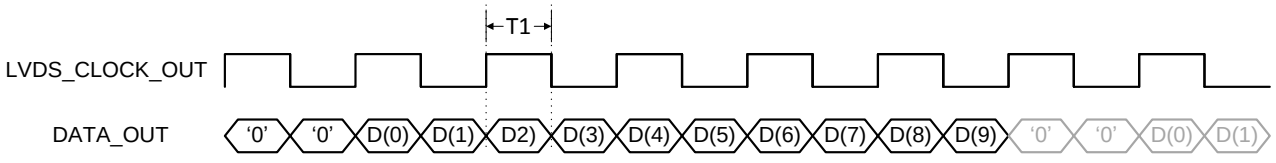


FIGURE 14: 10-BIT PIXEL DATA ON AN LVDS CHANNEL

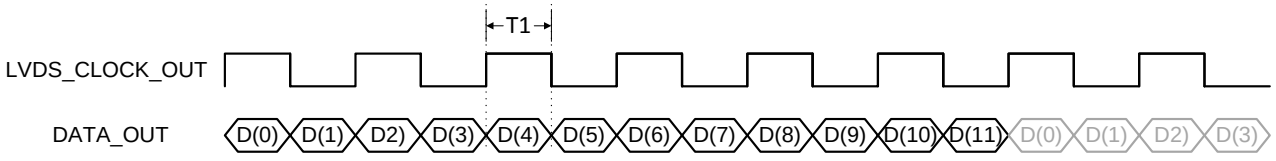


FIGURE 15: 12-BIT PIXEL DATA ON AN LVDS CHANNEL

The time 'T1' in the diagram above is 1/12th of the period of the input clock (CLK_IN) of the CMV300. If a frequency of 40MHz is used for CLK_IN (max), this results in a 240MHz LVDS_CLOCK_OUT.

4.1.2 LVDS READOUT TIMING

The readout of image data is grouped in bursts of 324 pixels per channel (2 rows at the same time). Each pixel is 12 bits of data (see section 4.1.1). One complete pixel period equals one period of the master clock input. For details on pixel remapping and pixel vs channel location please see section 4.1.3 of this document. An overhead time exists between two bursts of 324 pixels. This overhead time has the length of one pixel read-out (i.e. the length of 12 bits at the selected data rate) or one master clock cycle.

4.1.2.1 4 OUTPUT CHANNELS

By default, all 4 data output channels are used to transmit the image data. This means that two entire rows of image data are transferred in one slot of 324 pixel periods (4 x 324 = 1296). Next figure shows the timing for the top and bottom LVDS channels.

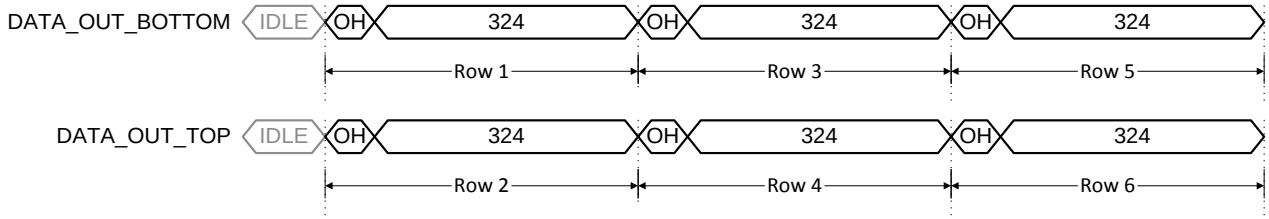


FIGURE 16: OUTPUT TIMING IN DEFAULT 4 CHANNEL MODE

Only when 4 data outputs, running at 300Mbps, are used, the frame rate of 300fps can be achieved (default).

4.1.2.2 2 OUTPUT CHANNELS

The CMV300 has the possibility to use only 2 LVDS output channels. This setting can be programmed in the register with address 57 (see section 5.7). In such multiplexed output mode, only the 2 bottom LVDS channels are used (channel 1 and channel 2). The readout of one row takes 1*324 periods. Next figure shows the timing for the bottom LVDS channels.

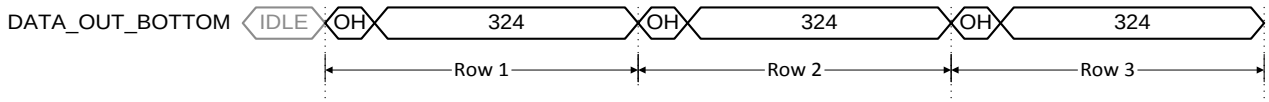


FIGURE 17: OUTPUT TIMING IN 2 CHANNEL MODE

In this 2 channel mode, the frame rate is reduced with a factor of 2 compared to 4 channel mode.

4.1.2.3 1 OUTPUT CHANNEL

The CMV300 has also the possibility to use only 1 LVDS output channel. This setting can be programmed in the register with address 57 (see section 5.7). In such multiplexed output mode, only 1 of the bottom 2 LVDS channels is used (channel 1) and the readout of one row takes 2*324 periods.

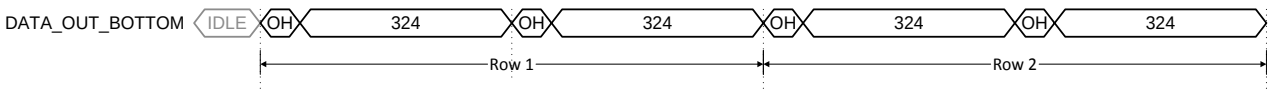


FIGURE 18: OUTPUT TIMING IN OF 1 CHANNEL MODE

In this 1 channel mode, the frame rate is reduced with a factor of 4 compared to 4 channel mode.

4.1.3 PIXEL REMAPPING

Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next sections, the end user is able to remap the pixel values at the output to their correct image array location.

4.1.3.1 4 OUTPUTS

The figure below shows the location of the image pixels versus the output channel of the image sensor.

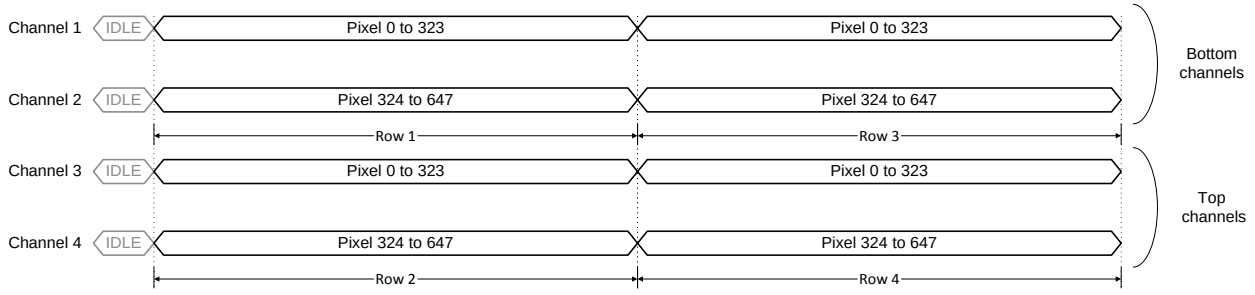


FIGURE 19: PIXEL REMAPPING FOR 4 OUTPUT CHANNELS

4 bursts (2 x 2) of 324 pixels happen in parallel on the data outputs. This means that two complete rows are read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 488 rows being read out.

4.1.3.2 2 OUTPUTS

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in the figure below. 2 bursts of 324 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The time needed to read out two rows is doubled compared to when 4 outputs are used. The top LVDS channels are not being used in this mode, so they can be turned off by setting the correct bits in the register with address 81. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be read out depends on the value in the corresponding register. By default there are 488 rows being read out.

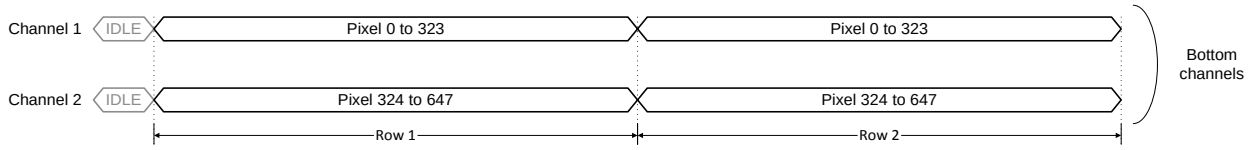


FIGURE 20: PIXEL REMAPPING FOR 2 OUTPUT CHANNELS

4.1.3.3 1 OUTPUT

When only 1 output is used, 1 burst of 324 pixels happens on the data outputs. This means that one complete row is read out in 2 bursts. The time needed to read out one row is 2x longer compared to when 2 outputs are used. The top LVDS channels are not being used in this mode, so these and the remaining bottom channel can be turned off by setting the correct bits in the register with address 81. Turning off these channels will reduce the power consumption of the chip. The amount of rows that will be readout depends on the value in the corresponding register. By default there are 488 rows being read out

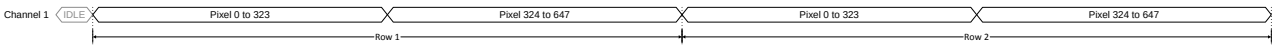


FIGURE 21: PIXEL REMAPPING FOR 1 OUTPUT CHANNEL

4.1.4 CONTROL CHANNEL

The CMV300 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits.

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the readout of a row
[2]	FVAL	Indicates the validity of the readout of a frame
[3]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels) (*)
[4]	INTE1	Indicates when pixels of integration block 1 are integrating (*)
[5]	INTE2	Indicates when pixels of integration block 2 are integrating (*)
[6]	'0'	Constant zero
[7]	'1'	Constant one
[8]	'0'	Constant zero
[9]	'0'	Constant zero
[10]	'0'	Constant zero
[11]	'0'	Constant zero

(*)Note: The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

Pin C6 (Test3 / CLK_OUT) can be programmed to map some control bits for easy measurement. Register 69 is used for this programming:

Register 69 Value	T_dig1
0	DVAL
1	LVAL
2	FVAL
6	FOT
7	INTE1
8	INTE2
9	CLK_OUT

4.1.4.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the readout status. Next figure shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the readout of a frame of 3 rows (default is 488 rows). This example uses the default mode of 4 outputs (2 outputs on each side).

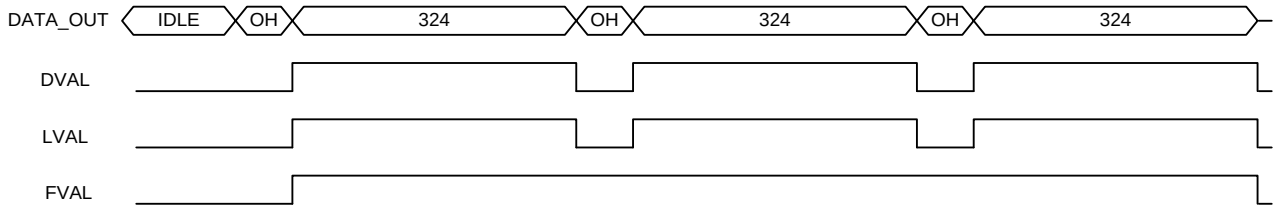


FIGURE 22: DVAL, LVAL AND FVAL TIMING IN 4 OUTPUT MODE

When only 1 output (on one side) is used, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode looks like the diagram below.

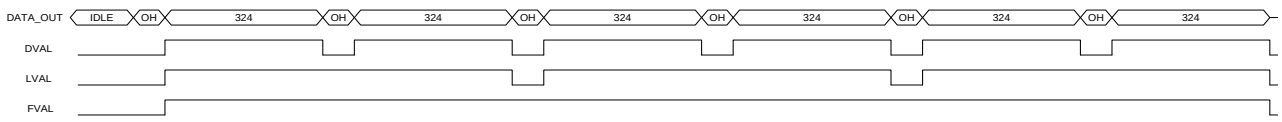


FIGURE 23: DVAL, LVAL AND FVAL TIMING IN 1 OUTPUT MODE

4.1.5 TRAINING DATA

The LVDS outputs are not perfectly edge aligned. This alignment has to be done in the receiving system. You can see the typical output skew in Figure 24. This skew is independent of the clock speed used. To synchronize the receiving

side with the LVDS outputs of the CMV300, a known data pattern can be put on the output channels. This pattern can be used to "train" the LVDS receiver of the surrounding system to achieve correct bit and word alignment of the image data. Such a training pattern is put on all 4 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 324 pixels). The training pattern is a 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 61-62) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

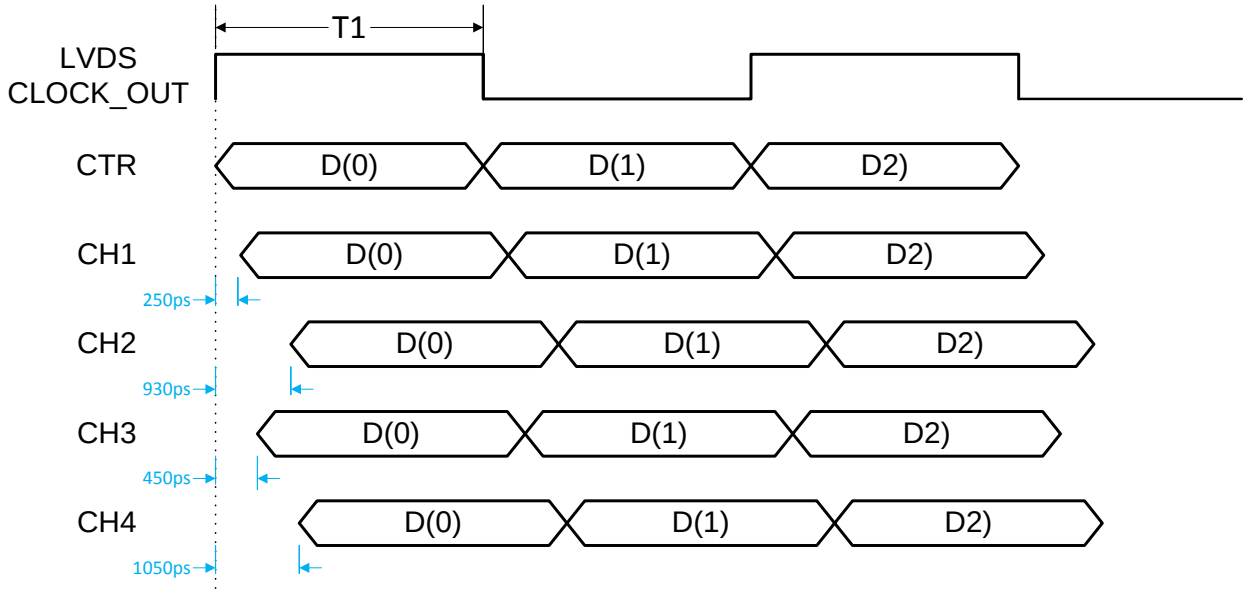


FIGURE 24: LVDS OUTPUT SKEW

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [7].

The figure below shows the location of the training pattern (TP) on the data channels and control channels when the sensor is in idle mode and when a frame of 3 rows is read-out. The default mode of 4 outputs is selected.

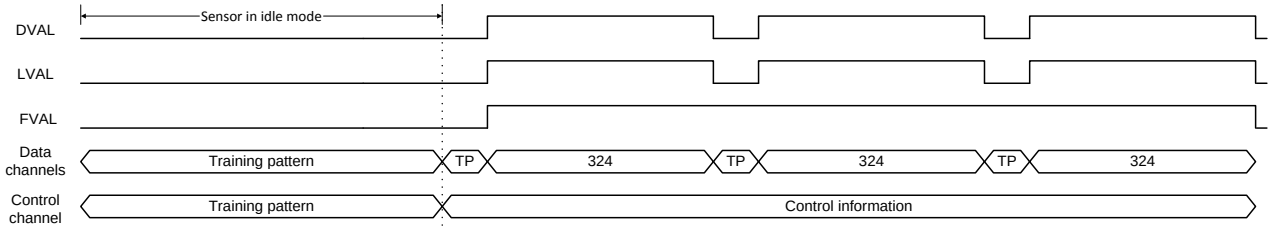


FIGURE 25: TRAINING PATTERN LOCATION IN THE DATA CHANNEL AND CONTROL CHANNEL

4.2 PARALLEL CMOS OUTPUT

When pin B2 is connected to GND, the CMV300 also has one 10 bit digital parallel CMOS output. On this output the pixels of the image array are presented with a frequency of maximum 40MHz resulting in a frame rate of 120 fps. Next to the data channels 3 additional CMOS channels are available for control and synchronization of the image data.

- 10 Data channels (bit[0] to bit[9], 1.8V CMOS)
- 2 Control channels (DVAL and LVAL, 1.8V CMOS)
- 1 Clock channel (CLK_OUT, 3.3V CMOS)

This means that a total of 13 pins of the CMV300 are used for the parallel CMOS output (10 for data + 2 for control channel + 1 for clock channel). See the pin list for the exact pin numbers of the parallel CMOS output. The 10 data channels are used to transfer the 10-bit pixel data from the sensor to the receiver in the surrounding system. The output clock channel transports a clock, synchronous to the data on the data channels. Register 69 has to be set to 9 to output this clock. This clock can be used at the receiving end to sample the data. The data on the control channels contains status information on the validity of the data on the data channels.

4.2.1 PARALLEL OUTPUT TIMING

In parallel output mode, the readout of one row takes 2*324 periods. In this mode, the frame rate is reduced with a factor of 4 compared to 4 LVDS channel mode. The figure below shows the timing for read-out of one line

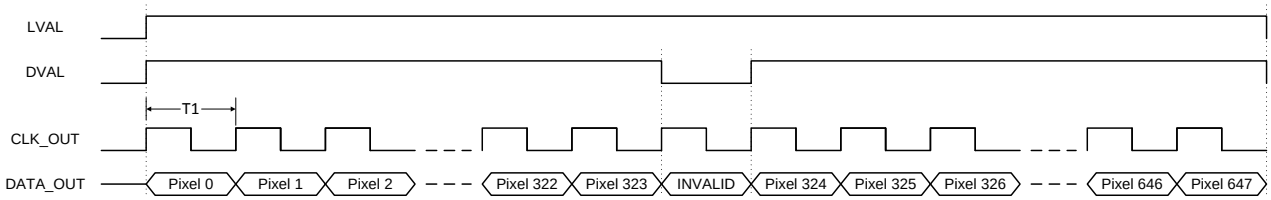


FIGURE 26: PARALLEL OUTPUT TIMING OF ONE LINE

The time of 'T1' from the figure above and below has the same length as the period of the CLK_IN signal. As can be seen in the figure above it is advised to sample the parallel output data on the falling edge of the CLK_OUT.

The figure below details the LVAL and DVAL timing for a frame read-out of tree lines.

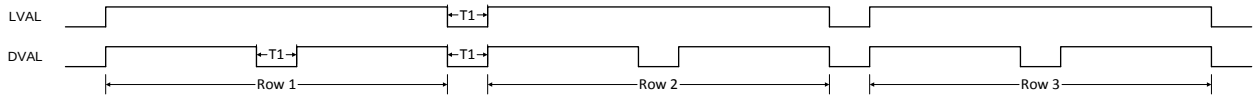


FIGURE 27: LVAL/DVAL TIMING FOR A FRAME OF 3 LINES USING THE PARALLEL OUTPUT

5 IMAGE SENSOR PROGRAMMING

This section explains how the CMV300 can be programmed using the on-board sequencer registers.

5.1 EXPOSURE MODES

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see section 3.10 for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

The table below gives an overview of the registers involved in the exposure mode.

Exposure time settings			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_ext	41[0]	0	0: Exposure time is defined by the value uploaded in the sequencer register (42-44) 1: Exposure time is defined by the pulses applied to the T_EXP1 and FRAME_REQ pins.
Exp_time	42-44	488	When the Exp_ext register is set to '0', the value in this register defines the exposure time according to the following formula: Exp_time x 325 x clk_per, where clk_per is the period of the master input clock. The minimal value for this is 1.

To calculate the exact exposure time when using internal exposure mode (Exp_ext = 0) use:

$$Exposure\ time = \big((Exp\_time - 1) * 325 + 133 + (48 * reg58)\big) * clk\_in\_per$$

Clk_in_per is the period of the input CLK_IN clock.

For external exposure mode (Exp_ext = 1) this becomes:

$$Exposure\ time = \text{Ext\_exp\_time} + (48 * \text{reg58} * clk\_in\_per)$$

Ext_exp_time is the time between the T_EXP1/2 and Frame_req pulses.

The (133 + (48 * reg58)) is the part of the FOT for which the sensor is light sensitive and will therefor determine the minimum exposure time. Below you can see the detailed timing of one frame cycle in internal exposure mode with Exp_time = 244, reg58 = 44, linte time = 325*Tclk and Tclk is the period of the master CLK_IN without multiplexing.

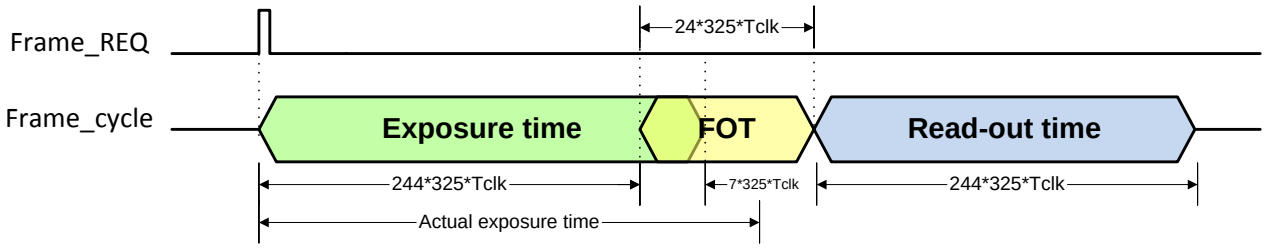


FIGURE 28: FRAME CYCLE TIMING

You can see that the exposure overlap is 7/24th of the FOT.

5.2 HIGH DYNAMIC RANGE MODES

The sensor has different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even columns have a different exposure time
- Piecewise linear response: pixels respond to light with a piecewise linear response curve.

All the HDR modes mentioned above can be used in both the internal- and external-exposure-time mode.

5.2.1 INTERLEAVED READ-OUT

In this HDR mode, the odd and even columns of the image sensors will have a different exposure time. This mode can be enabled by setting the register in the table below.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_dual	41[1]	0	0: interleaved exposure mode disabled 1: interleaved exposure mode enabled

The surrounding system can combine the image of the odd columns with the image of the even columns which can result in a high dynamic range image. In such an image very bright and very dark objects are made visible without clipping. The table below gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

HDR settings – interleaved read-out			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	488	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the even columns according following formula: Exp_time x 325 x clk_per, where clk_per is the period of the master input clock.
Exp_time2	45-47	488	When the Exp_dual register is set to '1', the value in this register defines the exposure time for the odd columns according following formula: Exp_time2 x 325 x clk_per, where clk_per is the period of the master input clock.

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the T_EXP1 and T_EXP2 input pins. T_EXP1 defines the exposure time for the even columns, while T_EXP2 defines the exposure time for the odd columns. See the figure below for more details.

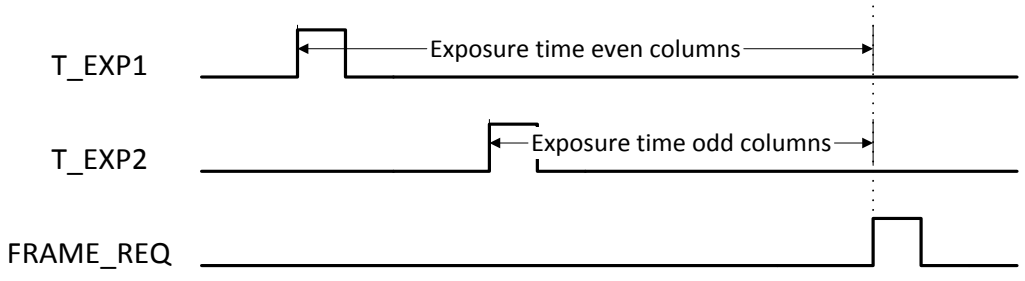


FIGURE 29: INTERLEAVED READ-OUT IN EXTERNAL EXPOSURE MODE

When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate register to '0'.

Color/mono			
Register name	**Register address**	**Default value**	**Description of the value**
Color	39[0]	1	0: color sensor is used 1: monochrome sensor is used

5.2.2 PIECEWISE LINEAR RESPONSE

The CMV300 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This feature will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve. More details can be found in the figure below.

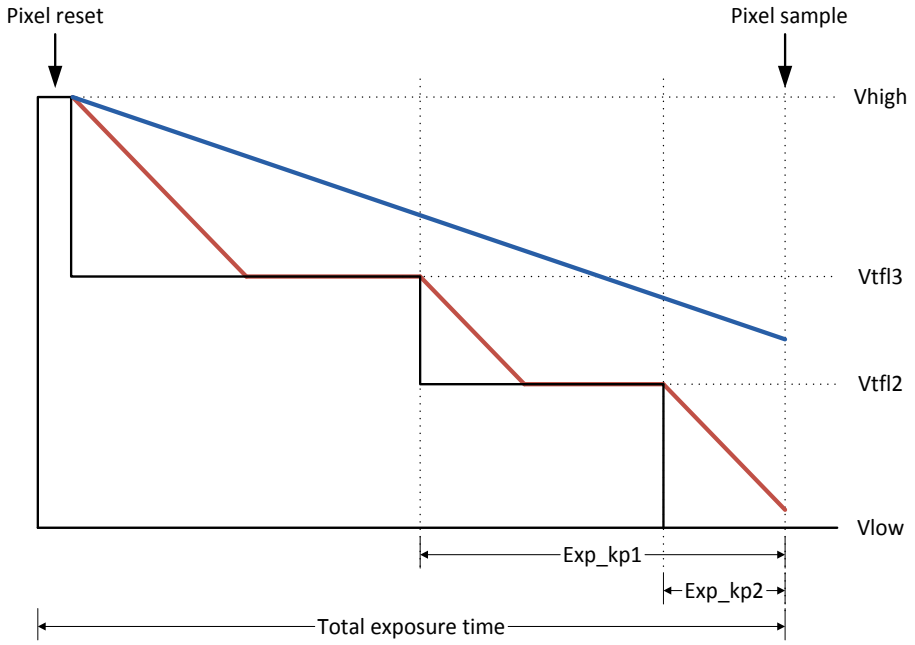


FIGURE 30: PIECEWISE LINEAR RESPONSE DETAILS

In the figure above, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. As shown in the figure, the bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The Vtfl voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in the figure below can be achieved. The placement of the kneepoints in X is controlled by the Vtfl programming, while the slope of the segments is controlled by the programmed exposure times.

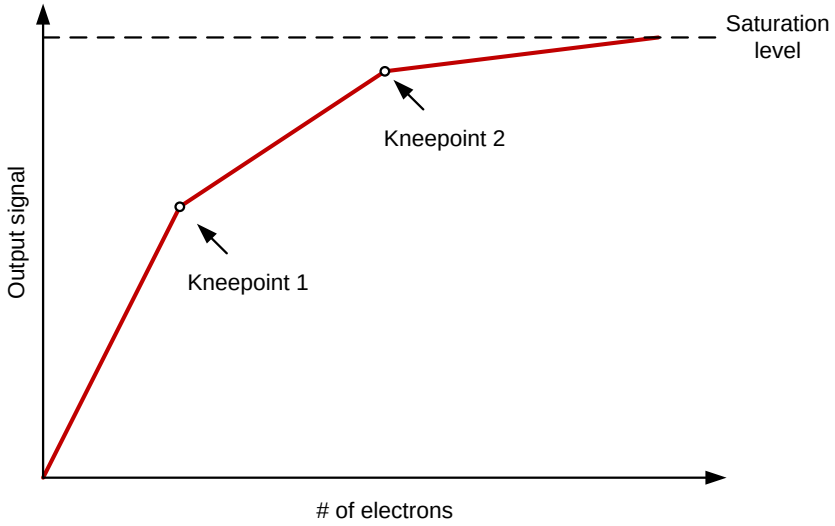


FIGURE 31: PIECEWISE LINEAR RESPONSE

When using the PLR mode, the CDS for the second and third slope is not available anymore, increasing the FPN for these slopes. Also the noise will become higher in this mode.

5.2.2.1 PIECEWISE LINEAR RESPONSE WITH INTERNAL EXPOSURE MODE

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

HDR settings – PLR			
Register name	**Register address**	**Default value**	**Description of the value**
Exp_time	42-44	488	The value in this register defines the total exposure time according following formula: Exp_time x 325 x clk_per, where clk_per is the period of the master input clock.
Nr_slopes	54[1:0]	1	The value in this register defines the number of slopes (min=1, max=3).
Exp_kp1	48-50	1	The value in this register defines the exposure time from kneepoint 1 to the end of the total exposure time. Formula: Exp_kp1 x 325 x clk_per, where clk_per is the period of the master input clock.
Exp_kp2	51-53	1	The value in this register defines the exposure time from kneepoint 2 to the end of the total exposure time. Formula: Exp_kp2 x 325 x clk_per, where clk_per is the period of the master input clock.
Vtfl2	113[6:0]	64	The value in this register defines the Vtfl2 voltage (DAC setting) of kneepoint 1. Bit[6] = enable (=1) Bit[5:0] = value (0-64)
Vtfl3	114[6:0]	64	The value in this register defines the Vtfl3 voltage (DAC setting) of kneepoint 2. Bit[6] = enable (=1) Bit[5:0] = value (0-64)

5.2.2.2 PIECEWISE LINEAR RESPONSE WITH EXTERNAL EXPOSURE MODE

When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed.

HDR settings – PLR			
Register name	**Register address**	**Default value**	**Description of the value**
Nr_slopes	54	1	The value in this register defines the number of slopes (min=1, max=3).
Vtfl2	113[6:0]	64	The value in this register defines the Vtfl2 voltage (DAC setting) of kneepoint 1. Bit[6] = enable (=1) Bit[5:0] = value (0-64)
Vtfl3	114[6:0]	64	The value in this register defines the Vtfl3 voltage (DAC setting) of kneepoint 2. Bit[6] = enable (=1) Bit[5:0] = value (0-64)

The timing that needs to be applied in this external exposure mode looks like the one below.

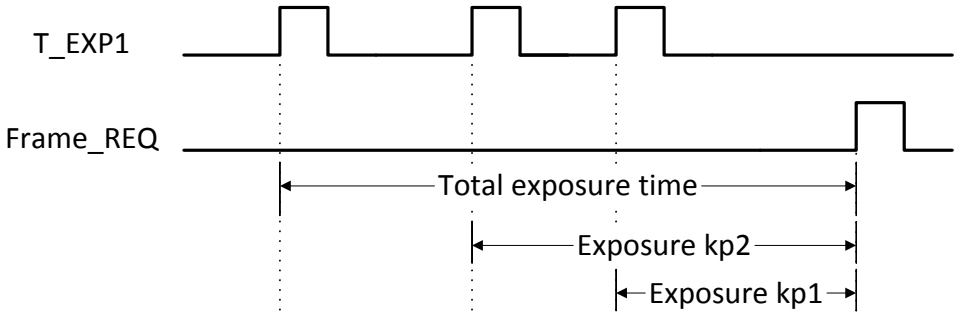


FIGURE 32: PIECEWISE LINEAR RESPONSE WITH EXTERNAL EXPOSURE MODE

In this case the T_EXP1 pulses should be one CLK_IN period wide exactly. When shorter, they might not be detected and when longer, this will be seen as 2 (or more) pulses one after the other, which will not give a useable image.

Please note, that a combination of the piecewise linear response and interleaved read-out is not possible.

5.3 WINDOWING

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The CMV300 has the possibility to read out multiple (max=8) predefined subwindows in one read-out cycle. The default mode is to read-out one window with the full frame size (648 x 488).

5.3.1 SINGLE WINDOW

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 488 (full frame).

Windowing – single window			
Register name	**Register address**	**Default value**	**Description of the value**
start1	3-4	0	The value in this register defines the start address of the window in Y (min=0, max=487)
Number_lines	1-2	488	The value in this register defines the number of lines read out by the sensor (min=1, max=488)

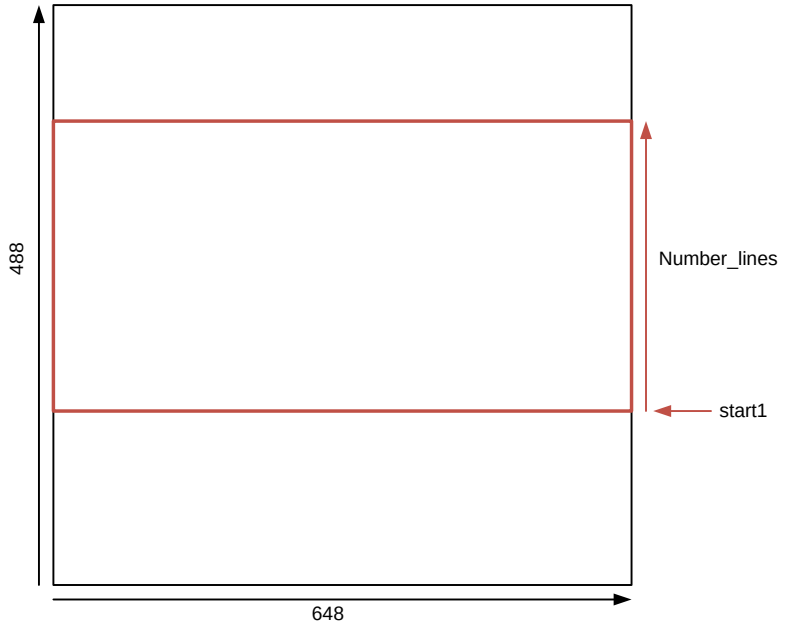


FIGURE 33: SINGLE WINDOW SETTINGS

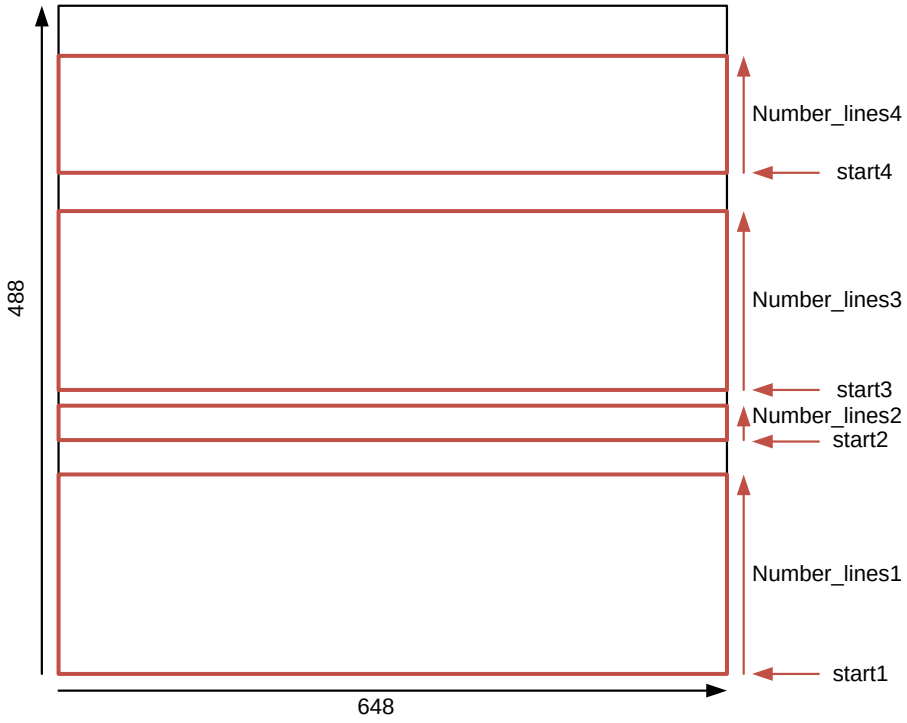
5.3.2 MULTIPLE WINDOWS

The CMV300 can read out a maximum of 8 different subwindows in one read-out cycle. The location and length of these subwindows must be programmed in the correct registers. The total number of lines to be read-out (sum of all windows) needs to be specified in the Number_lines register. The registers which need to be programmed for the multiple windows can be found in the table below.

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	488	The value in this register defines the total number of lines read-out by the sensor (min=1, max=488)
start1	3-4	0	The value in this register defines the start address of the first window in Y (min=0, max=487)
Number_lines1	19-20	0	The value in this register defines the number of lines of the first window (min=1, max=488)
start2	5-6	0	The value in this register defines the start address of the second window in Y (min=0, max=487)
Number_lines2	21-22	0	The value in this register defines the number of lines of the second window (min=1, max=488)
start3	7-8	0	The value in this register defines the start address of the third window in Y (min=0, max=487)
Number_lines3	23-24	0	The value in this register defines the number of lines of the third window (min=1, max=488)
start4	9-10	0	The value in this register defines the start address of the fourth window in Y (min=0, max=487)
Number_lines4	25-26	0	The value in this register defines the number of lines of the fourth window (min=1, max=488)
start5	11-12	0	The value in this register defines the start address of the fifth window in Y (min=0, max=487)
Number_lines5	27-28	0	The value in this register defines the number of lines of the fifth window (min=1, max=488)
start6	13-14	0	The value in this register defines the start address of the sixth window in Y (min=0, max=487)

Windowing – multiple windows			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines6	29-30	0	The value in this register defines the number of lines of the sixth window (min=1, max=488)
start7	15-16	0	The value in this register defines the start address of the seventh window in Y (min=0, max=487)
Number_lines7	31-32	0	The value in this register defines the number of lines of the seventh window (min=1, max=488)
start8	17-18	0	The value in this register defines the start address of the eighth window in Y (min=0, max=487)
Number_lines8	33-34	0	The value in this register defines the number of lines of the eighth window (min=1, max=488)

Note: The default values will result in one window with 488 lines to be read out



Number_lines = Number_lines1 + Number_lines2 + Number_lines3 + Number_lines4

FIGURE 34: EXAMPLE OF 4 SUBWINDOWS READ-OUT

5.4 IMAGE FLIPPING

The image coming out of the image sensor, can be flipped in X and/or Y direction. This means that if flipping is enabled in both directions the upper right pixel is read out first (instead of lower left). The following registers are involved in image flipping

Image flipping			
Register name	**Register address**	**Default value**	**Description of the value**
Image_flipping	40[1:0]	0	0: No image flipping 1: Image flipping in X 2: Image flipping in Y 3: Image flipping in X and Y

5.5 IMAGE SUBSAMPLING

To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. The registers involved in subsampling are detailed below. A distinction is made between a simple and advanced mode (can be used for color devices). Subsampling can be enabled in every windowing mode.

5.5.1 SIMPLE SUBSAMPLING

Image subsampling - simple			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	488	The value in this register defines the total number of lines read out by the sensor (min=1, max=488)
Sub_s	35-36	0	Number of rows to skip (min=0, max=487)
Sub_a	37-38	0	Identical to Sub_s

The figures below give two subsampling examples (skip 4x and skip 1x).

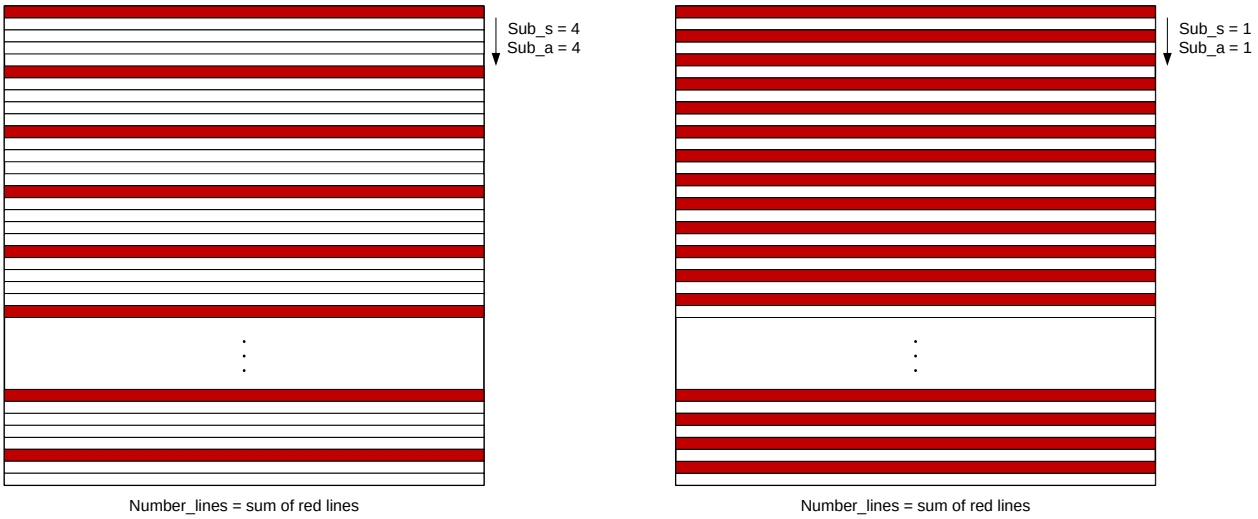


FIGURE 35: SUBSAMPLING EXAMPLES (SKIP 4X AND SKIP 1X)

5.5.2 ADVANCED SUBSAMPLING

When a color sensor is used, the subsampling scheme should take into account that a Bayer color filter is applied on the sensor. This Bayer pattern should be preserved when subsampling is used. This means that the number of rows to be skipped should always be a multiple of two. An advanced subsampling scheme can be programmed to achieve these requirements. Of course, this advanced subsampling scheme can also be programmed in a monochrome sensor. See the table of registers below for more details.

Image subsampling - advanced			
Register name	**Register address**	**Default value**	**Description of the value**
Number_lines	1-2	488	The value in this register defines the total number of lines read out by the sensor (min=1, max=488)
Sub_s	35-36	0	Should be '0' at all times
Sub_a	37-38	0	Number of rows to skip, it should be an even number between (0 and 486).

The figures below give two subsampling examples (skip 4x and skip 2x) in advanced mode.

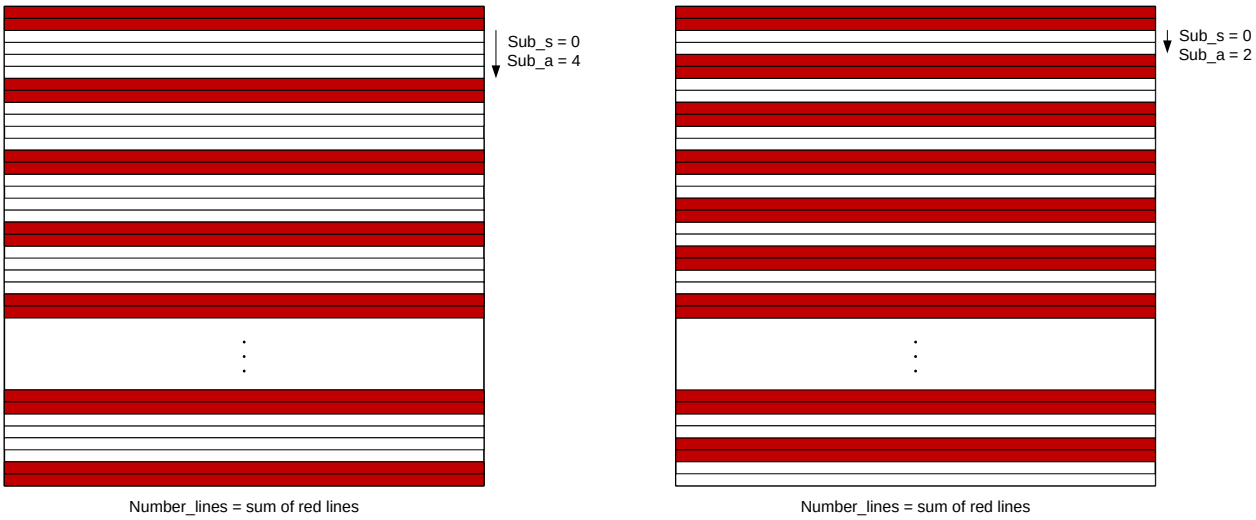


FIGURE 36: SUBSAMPLING EXAMPLES IN ADVANCED MODE (SKIP 4X AND SKIP2X)

5.6 NUMBER OF FRAMES

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Number of frames			
Register name	**Register address**	**Default value**	**Description of the value**
Number_frames	55-56	1	The value in this register defines the number of frames grabbed and sent by the image sensor in internal exposure mode (min =1, max = 65535)

5.7 OUTPUT MODE

When LVDS output mode is selected, the number of LVDS channels can be selected by programming the appropriate sequencer register. The pixel remapping scheme and the read-out timing for each mode can be found in section 4 of this document.

When parallel CMOS output mode is selected, the Output_mode register should be fixed to 3. Also register 69 has to be set at 8 and pin B2 connected to ground. The read-out timing for this mode can be found in section 4 of this document.

Output mode			
Register name	**Register address**	**Default value**	**Description of the value**
Output_mode	57[1:0]	0	0: 4 outputs (LVDS) 2: 2 outputs (LVDS) 3: 1 output (LVDS or parallel CMOS)

5.8 TRAINING PATTERN

As detailed in section 4.1.5, a training pattern is sent over the LVDS data channels whenever no valid image data is sent. This training pattern can be programmed using the sequencer register.

Training pattern			
Register name	**Register address**	**Default value**	**Description of the value**
Training_pattern	61-62[3:0]	85	

5.9 8-BIT, 10-BIT OR 12-BIT MODE

The CMV300 has the possibility to send 8 bits, 10 bits or 12 bits per pixel. The end user can select the desired resolution by programming the corresponding sequencer register.

8-bit, 10-bit or 12-bit mode			
Register name	**Register address**	**Default value**	**Description of the value**
Bit_mode	68[1:0]	0	0: 12 bits per pixel 1: 10 bits per pixel 2: 8 bits per pixel

The sensor will always output words of 12 bit length. So when changing to 10 or 8 bit, the MSB's will be filled with 0's. This means that changing bit mode doesn't affect the frame rate.

Bit mode	Decimal value	Output word
8b	170	0000 1010 1010
10b	682	0010 1010 1010
12b	2730	1010 1010 1010

5.10 DATA RATE

During start-up or after a sequencer reset, the data rate can be changed if a lower speed than 480Mbps is desired. This can be done by applying a lower master input clock (CLK_IN) to the sensor and uploading a new value in the PLL_range register. See section 3.5 for more details on the input clock. See section 3.7 and 3.8 for details on how and when the data rate can be changed.

PLL range			
Register name	**Register address**	**Default value**	**Description of the value**
PLL_range	83	155	155: CLK_IN is between 41.67 and 50MHz 187: CLK_IN is between 20.83MHz and 41.67MHz 251: CLK_IN is between 10 and 20.83MHz

5.11 DISABLING THE PLL

When you do not want to use the internal PLL of the sensor, you can disable it and input an LVDS clock yourself. The output data speed will then be equal to this clock speed, while the output LVDS clock will be half of the LVDS input clock. The LVDS_CLK_IN should be connected to pins D7 (LVDS_CLK_N) and D8 (LVDS_CLK_P) with a 100Ω parallel termination resistor between the two pins.

To disable the PLL set the following registers:

PLL range			
Register name	**Register address**	**Default value**	**Description of the value**
PLL_enable	83[7]	1	0: Disables the PLL 1: Enables the PLL
CLK_LVDS_EXT	84	0	0: Uses the CLK_IN input 1: Uses the LVDS_CLK_IN input
CLK_SEL	63[7]	0	0: Uses the PLL output internally 1: Uses the LVDS clock internally
Channel_en	81[0]	0	0: Disables the LVDS input channel 1: Enables the LVDS input channel
I_LVDS	82[3:0]	0	0: Disables the receiver current 8: Sets the receiver current

When using this mode, the maximum clock speed and therefor frame rate is lower than when using the internal PLL. When disabling the PLL, the maximum LVDS input clock speed will be 430MHz, resulting in a frame rate of 430fps. See Errata Sheet 2 for more detail on this speed limit.

5.12 POWER CONTROL

The power consumption of the CMV300 can be regulated by disabling the LVDS data channels when they are not used (in 2 or 1 channel mode).

Power control			
Register name	**Register address**	**Default value**	**Description of the value**
Channel_en	81[6:0]	126	Bit 1-2 enable/disable the bottom data output channels Bit 3-4 enable/disable the top data output channels Bit 5 enables/disables the output clock channel Bit 6 enables/disables the control channel Bit 0 enables/disables the optional LVDS clock input channel 0: disabled 1: enabled

5.13 OFFSET AND GAIN

5.13.1 OFFSET

A digital offset can be applied to the output signal. A separate offset can be given to the data coming from the top outputs and the data coming from the the bottom outputs. The dark level offset can be programmed by setting the desired value in the sequencer registers. Dark-level @ output = ADC_output + Offset

Offset			
Register name	**Register address**	**Default value**	**Description of the value**
Offset_bot Offset_top	59-60[3:0] 97-98[3:0]	0 0	The value in this register defines the dark level offset applied to the output signal (min = 0, max = 4095) The value must be seen as a two's complement where values higher than 2047 are used to give a negative offset. Example: - 000000000101 = 5 will add 5DN to the signal - 111111111011 = -5 will subtract 5DN from the signal

Both offsets don't have to be the same value.

5.13.2 GAIN

An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied by the ADC.

Gain			
Register name	**Register address**	**Default value**	**Description of the value**
PGA_gain	80[2:0]	0	0: x1 gain 1: x1.25 gain 2: x1.5 gain 3: x1.75 gain 4: x2 gain 5: x2.5 gain 6: x3 gain 7: x3.5 gain
ADC_gain	100[6:0]	96	Bit[6] = 1 (enable) Bit[5:0] = ADC gain value (range 0 to 63)

The ADC value should be adjusted per clock speed to get the same response. The ADC unity gain value for 40MHz is 48, for 35MHz is 49 and for frequencies below 30MHz it is 51. In the plot below you can see the actual gain per ADC gain value. It is advised to keep the ADC value in the bold non-dashed region, otherwise non-linearity and/or FPN will occur.

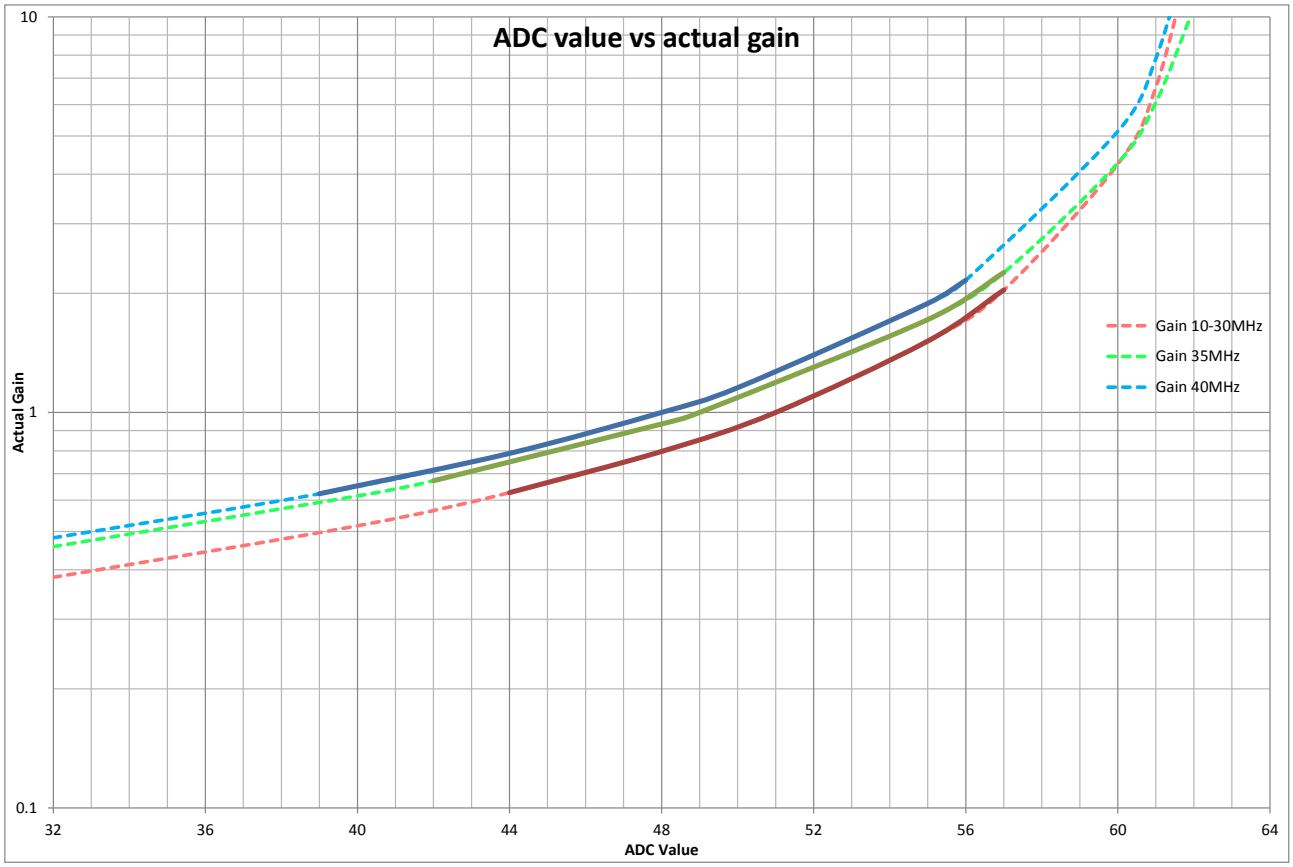


FIGURE 37: ADC VALUE VS ACTUAL GAIN

Also the ADC gain value should be calibrated per device to get the same response.

6 REGISTER OVERVIEW

The table below gives an overview of all the sensor registers. The registers with the remark “Do not change” should not be changed. The required values should be written to the appropriate registers for optimal sensor workings and image performance (at 40MHz).

Register overview										
Address	**Default**	**Value**								**Remark/Required value**
		Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	
0	0									Do not change
1	232	Number_lines[7:0]								
2	1	Number lines [15:8]								
3	0	Start1[7:0]								
4	0	Start1[15:8]								
5	0	Start2[7:0]								
6	0	Start2[15:8]								
7	0	Start3[7:0]								
8	0	Start3[15:8]								
9	0	Start4[7:0]								
10	0	Start4[15:8]								
11	0	Start5[7:0]								
12	0	Start5[15:8]								
13	0	Start6[7:0]								
14	0	Start6[15:8]								
15	0	Start7[7:0]								
16	0	Start7[15:8]								
17	0	Start8[7:0]								
18	0	Start8[15:8]								
19	0	Number_lines1[7:0]								
20	0	Number_lines1[15:8]								
21	0	Number_lines2[7:0]								
22	0	Number_lines2[15:8]								
23	0	Number_lines3[7:0]								
24	0	Number_lines3[15:8]								
25	0	Number_lines4[7:0]								
26	0	Number_lines4[15:8]								
27	0	Number_lines5[7:0]								
28	0	Number_lines5[15:8]								
29	0	Number_lines6[7:0]								
30	0	Number_lines6[15:8]								
31	0	Number_lines7[7:0]								
32	0	Number_lines7[15:8]								
33	0	Number_lines8[7:0]								
34	0	Number_lines8[15:8]								
35	0	Sub_s[7:0]								
36	0	Sub_s[15:8]								
37	0	Sub_a[7:0]								
38	0	Sub_a[15:8]								
39	1								Color	
40	0							Image_flipping[1:0]		
41	0							Exp_dual	Exp_ext	
42	232	Exp_time[7:0]								
43	1	Exp_time[15:8]								
44	0	Exp_time[23:16]								

Register overview										
Address	**Default**	**Value**								**Remark/Required value**
		Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	
45	232	Exp_time2[7:0]								
46	1	Exp_time2[15:8]								
47	0	Exp_time2[23:16]								
48	0	Exp_kp1[7:0]								
49	0	Exp_kp1[15:8]								
50	0	Exp_kp1[23:16]								
51	0	Exp_kp2[7:0]								
52	0	Exp_kp2[15:8]								
53	0	Exp_kp2[23:16]								
54	1							Nr_slopes[1:0]		
55	1	Number_frames [7:0]								
56	0	Number_frames[15:8]								
57	0							Output_mode[1:0]		
58	4									Set to 44
59	0	Offset_bot[7:0]								Set to 240
60	0					Offset_bot[11:8]				Set to 10
61	85	Training_pattern[7:0]								
62	0					Training pattern [11:8]				
63	12									Do not change
64	2									Do not change
65	0									Do not change
66	0									Do not change
67	0									Do not change
68	0							Bit_mode[1:0]		
69	0									Set to 9
70	0									Do not change
71	0									Do not change
72	0									Do not change
73	0									Do not change
74	0									Do not change
75	0									Do not change
76	0									Do not change
77	128									Do not change
78	0	Temp_sensor[7:0]								
79	0	Temp_sensor[15:8]								
80	0						PGA_gain[2:0]			Set to 2
81	126		Channel_en[6:0]							
82	128									Do not change
83	155	PLL_range[7:0]								Set to 187
84	0									Do not change
85	3									Do not change
86	0									Do not change
87	0									Do not change
88	0									Do not change
89	0									Do not change
90	0									Do not change
91	0									Do not change
92	0									Do not change
93	0									Do not change
94	0									Do not change
95	0									Do not change

Register overview										
Address	**Default**	**Value**								**Remark/Required value**
		Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	
96	0									Do not change
97	0	Offset_top[7:0]								Set to 240
98	0					Offset_top[11:8]				Set to 10
99	255									Do not change
100	96		ADC_gain[6:0]							Set to 112*
101	136									Set to 98
102	136									Set to 34
103	136									Set to 64
104	96									Do not change
105	96									Do not change
106	64									94
107	96									Set to 110
108	96									Set to 91
109	96									Set to 82
110	96									Set to 80
111	64									Do not change
112	64									Do not change
113	64		Vtfl2[6:0]							
114	64		Vtfl3[6:0]							
115	96									Do not change
116	96									Do not change
117	96									Set to 91
118	0									Do not change
119	0									Do not change
120	0									Do not change
121	0									Do not change
122	0									Do not change
123	0									Do not change
124	0									Do not change
125	0									Do not change
126	0									Do not change
127	255									Do not change

Note: The default value of the “do not change” registers should not be overwritten.

*Depends per device and clock speed.

7 MECHANICAL SPECIFICATIONS

7.1 PACKAGE DRAWING

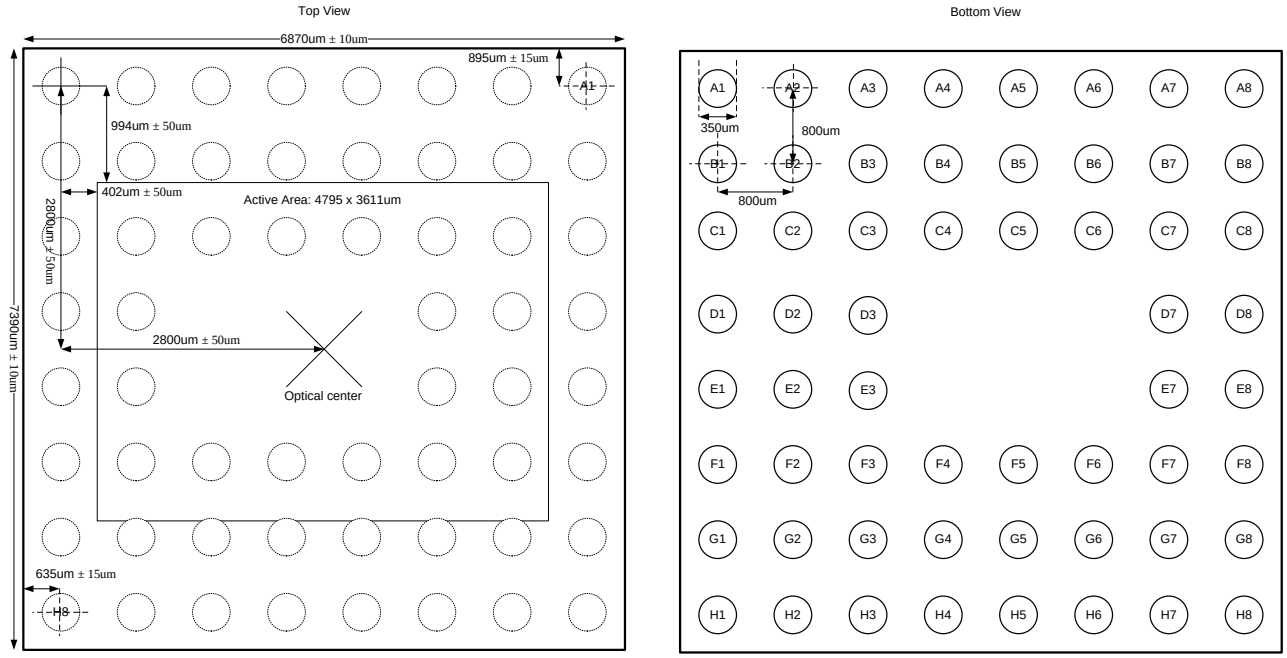


FIGURE 38: PACKAGE DRAWING OF THE CMV300. ALL DISTANCES IN µM

7.2 ASSEMBLY DRAWING

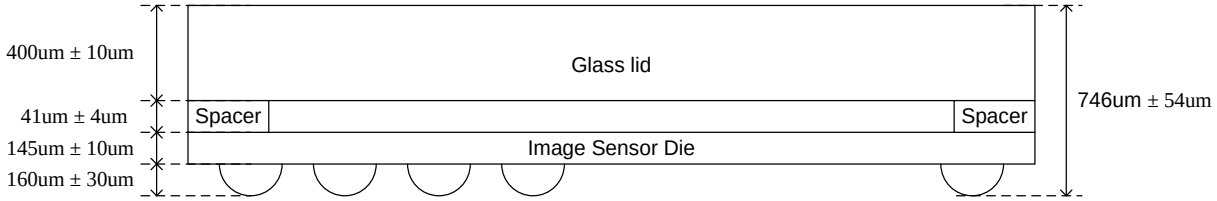


FIGURE 39: ASSEMBLY DRAWING OF CMV300

7.3 COVER GLASS

The cover glass of the CMV300 is plain D263 glass with a transmittance as shown in figure 37. Refraction index of the glass is 1.52. Scratch, bubbles and digs shall be less than or equal to 0.02 mm

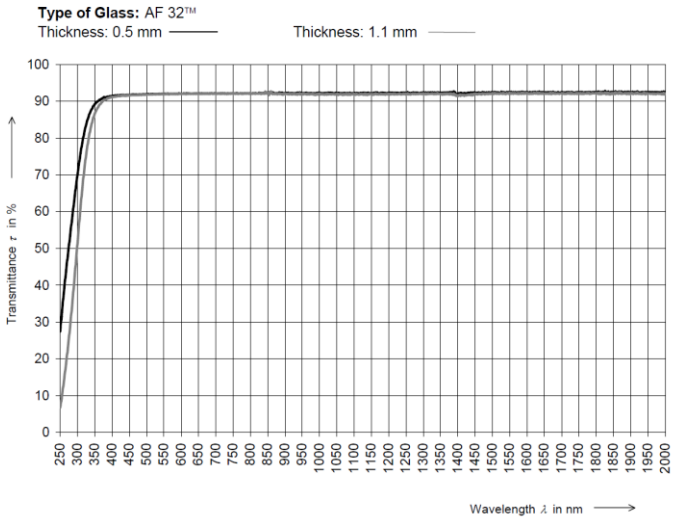


FIGURE 40: TRANSMITTANCE OF D263 GLASS

When a color sensor is used an IR-cutoff filter should be placed in the optical path of the sensor.

7.4 COLOR FILTERS

When a color version of the CMV300 is used, the color filters are applied in a Bayer pattern. The color version of the CMV300 always has microlenses. The typical spectral response of the CMV with color filters and D263 cover glass can be found below. The use of an IR cut-off filter in the optical path of the CMV300 image sensor is necessary to obtain good color separation when using light with an NIR component.

Not available yet

Figure 38: Typical spectral response of CMV300 with RGB color filters and D263 cover glass

A RGB Bayer pattern is used on the CMV300 image sensor. The order of the RGB filter can be found in the drawing below.

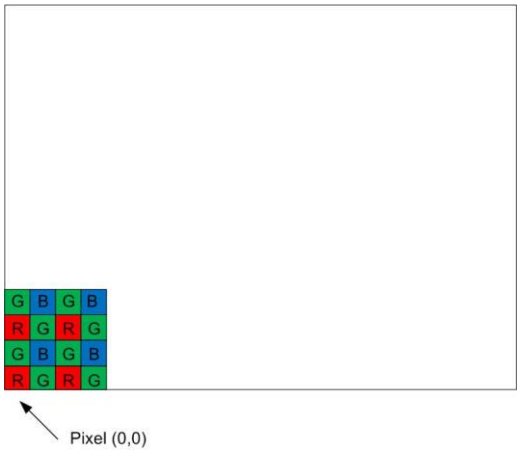


FIGURE 41: RGB BAYER PATTERN ORDER

8 SPECTRAL RESPONSE

The typical spectral response of a monochrome CMV300 with microlenses, with glass lid can be found below.

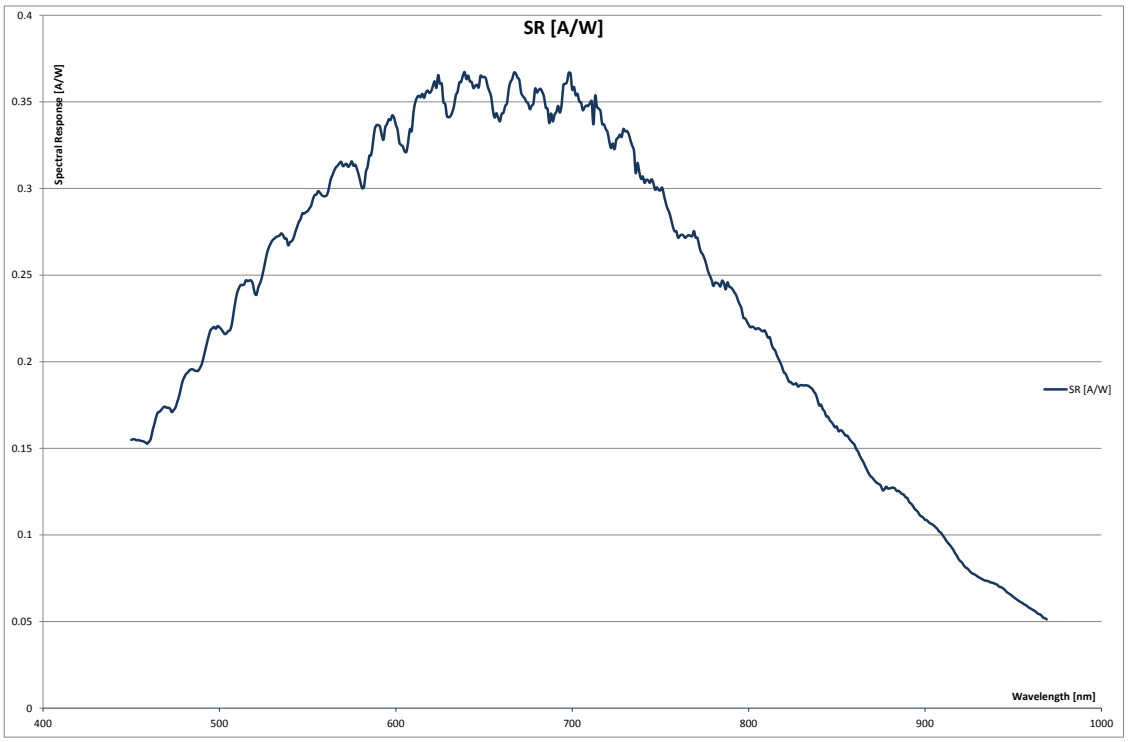


FIGURE 42: TYPICAL SPECTRAL RESPONSE

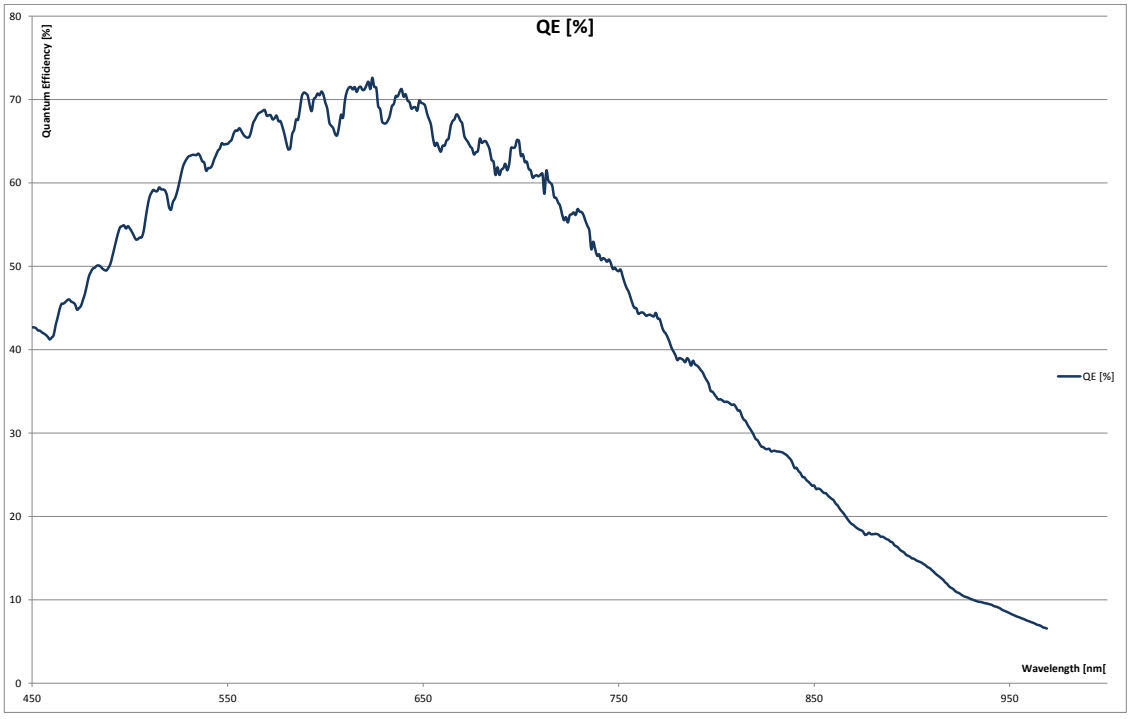


FIGURE 43: TYPICAL QUANTUM EFFICIENCY

9 PIN LIST

A distinction is made when the sensor is used in LVDS output mode or in parallel CMOS output mode.

9.1 LVDS OUTPUT MODE PIN LIST

The pin list of the CMV300 in LVDS output mode can be found below.

Pin number	Pin name	Description	Type
A1	Test1	No need to connect	Test pin
A2	GND	Connect to GND	GND
A3	GND	Connect to GND	GND
A4	VDDpix	Connect to 3.0V supply	Supply
A5	GND	Connect to GND	GND
A6	Output3_P	Image data output	Output
A7	Output4_P	Image data output	Output
A8	SPI_OUT	SPI output, 3.3V signaling	IO
B1	Test2	No need to connect	Test pin
B2	Enable_LVDS	Connect to VDD33	VDD33
B3	VDD18	Connect to 2.0V supply	Supply
B4	VDD33	Connect to 3.3V supply	Supply
B5	Output3_N	Image data output	output
B6	Output4_N	Image data output	Output
B7	Output_clk_P	LVDS clock output	output
B8	SPI_IN	SPI input, 3.3V signaling	IO
C1	VDD33	Connect to 3.3V supply	Supply
C2	VDDpix	Connect to 3.0V supply	Supply
C3	R_adc2	Optional, no need to connect	Bias
C4	R_adc1	Optional, no need to connect	Bias
C5	Output_clk_N	LVDS clock output	output
C6	Test3	No need to connect	Test
C7	SPI_EN	SPI input, 3.3V signaling	IO
C8	GND	Connect to GND	GND
D1	Vref	Decouple with 100nF to GND	Bias
D2	Vramp1	Decouple with 100nF to GND	Bias
D3	Vramp2	Decouple with 100nF to GND	Bias
D4	NC	Not connected	NA
D5	NC	Not connected	NA
D6	NC	Not connected	NA
D7	LVDS_CLK_N	LVDS input clock (N), optional	Input
D8	LVDS_CLK_P	LVDS input clock (P), optional	Input
E1	CMD_ramp	Decouple with with 100nF to VDD33	Bias
E2	Vpch_L	Decouple with with 100nF to GND	Bias
E3	Vbgap	Decouple with with 100nF to GND	Bias
E4	NC	Not connected	NA
E5	NC	Not connected	NA
E6	NC	Not connected	NA
E7	VDD33	Connect to 3.3V supply	Supply
E8	GND	Connect to GND	GND
F1	VDD33	Connect to 3.3V supply	Supply
F2	VDDpix	Connect to 3.0V supply	Supply
F3	VDD33	Connect to 3.3V supply	Supply
F4	FRAME_REQ	Digital input, 3.3V signaling	IO
F5	Output_ctrl_N	LVDS control output	Output
F6	T_EXP2	Digital input, 3.3V signaling	IO

Pin number	Pin name	Description	Type
F7	CLK_IN	Master clock input (max 25MHz), 3.3V signaling	IO
F8	SPI_CLK	SPI input, 3.3V signaling	IO
G1	Vtf_L	Decouple with with 100nF to GND	Bias
G2	Vtf_L2	Decouple with with 100nF to GND	Bias
G3	VDD18	Connect to 2.0V supply	Supply
G4	VDD33	Connect to 3.3V supply	Supply
G5	Output1_N	Image data output	Output
G6	Output2_N	Image data output	Output
G7	Output_ctrl_P	LVDS control output	Output
G8	T_EXP1	Digital input, 3.3V signaling	IO
H1	Vtf_L3	Decouple with with 100nF to GND	Bias
H2	GND	Connect to GND	GND
H3	GND	Connect to GND	GND
H4	VDDpix	Connect to 3.0V supply	Supply
H5	GND	Connect to GND	GND
H6	Output1_P	Image data output	Output
H7	Output2_P	Image data output	Output
H8	SYS_RES_N	Digital input, 3.3V signaling	IO

9.2 PARALLEL CMOS OUTPUT MODE PIN LIST

The pin list of the CMV300 in parallel CMOS output mode can be found below.

Pin number	Pin name	Description	Type
A1	Test1	No need to connect	Test pin
A2	GND	Connect to GND	GND
A3	GND	Connect to GND	GND
A4	VDDpix	Connect to 3.0V supply	Supply
A5	GND	Connect to GND	GND
A6	D4	Image data output, 1.8V signaling	Output
A7	D6	Image data output, 1.8V signaling	Output
A8	SPI_OUT	SPI output, 3.3V signaling	IO
B1	Test2	No need to connect	Test pin
B2	Enable_LVDS	Connect to GND	GND
B3	VDD18	Connect to 2.0V supply	Supply
B4	VDD33	Connect to 3.3V supply	Supply
B5	D5	Image data output, 1.8V signaling	Output
B6	D7	Image data output, 1.8V signaling	Output
B7	D8	Image data output, 1.8V signaling	Output
B8	SPI_IN	SPI input, 3.3V signaling	IO
C1	VDD33	Connect to 3.3V supply	Supply
C2	VDDpix	Connect to 3.0V supply	Supply
C3	R_adc2	Optional, no need to connect	Bias
C4	R_adc1	Optional, no need to connect	Bias
C5	D9	Image data output, 1.8V signaling	Output
C6	CLK_OUT	CMOS output, 3.3V signaling	Output
C7	SPI_EN	SPI input, 3.3V signaling	IO
C8	GND	Connect to GND	GND
D1	Vref	Decouple with 100nF to GND	Bias
D2	Vramp1	Decouple with 100nF to GND	Bias
D3	Vramp2	Decouple with 100nF to GND	Bias
D4	NC	Not connected	NA
D5	NC	Not connected	NA
D6	NC	Not connected	NA
D7	LVDS_CLK_N	LVDS input clock (N), optional	Input

Pin number	Pin name	Description	Type
D8	LVDS_CLK_P	LVDS input clock (P), optional	Input
E1	CMD_ramp	Decouple with with 100nF to VDD33	Bias
E2	Vpch_L	Decouple with with 100nF to GND	Bias
E3	Vbgap	Decouple with with 100nF to GND	Bias
E4	NC	Not connected	NA
E5	NC	Not connected	NA
E6	NC	Not connected	NA
E7	VDD33	Connect to 3.3V supply	Supply
E8	GND	Connect to GND	GND
F1	VDD33	Connect to 3.3V supply	Supply
F2	VDDpix	Connect to 3.0V supply	Supply
F3	VDD33	Connect to 3.3V supply	Supply
F4	FRAME_REQ	Digital input, 3.3V signaling	IO
F5	Data_valid	CMOS output, 1.8V signaling	Output
F6	T_EXP2	Digital input, 3.3V signaling	IO
F7	CLK_IN	Master clock input (max 25MHz), 3.3V signaling	IO
F8	SPI_CLK	SPI input, 3.3V signaling	IO
G1	Vtf_L	Decouple with with 100nF to GND	Bias
G2	Vtf_L2	Decouple with with 100nF to GND	Bias
G3	VDD18	Connect to 2.0V supply	Supply
G4	VDD33	Connect to 3.3V supply	Supply
G5	D1	Image data output, 1.8V signaling	Output
G6	D3	Image data output, 1.8V signaling	Output
G7	Line_valid	CMOS output, 1.8V signaling	Output
G8	T_EXP1	Digital input, 3.3V signaling	IO
H1	Vtf_L3	Decouple with with 100nF to GND	Bias
H2	GND	Connect to GND	GND
H3	GND	Connect to GND	GND
H4	VDDpix	Connect to 3.0V supply	Supply
H5	GND	Connect to GND	GND
H6	D0	Image data output, 1.8V signaling	Output
H7	D2	Image data output, 1.8V signaling	Output
H8	SYS_RES_N	Digital input, 3.3V signaling	IO

10 SPECIFICATION OVERVIEW

Specification	Value	Comment
Effective pixels	648 x 488	Containing 4 dark reference columns and rows.
Pixel pitch	7.4 x 7.4 μm^2	
Optical format	1/3”	
Full well charge	20 Ke-	Pinned photodiode pixel.
Conversion gain	0.185LSB/e-	12 bit mode, unity gain
Sensitivity	6 V/lux.s	With microlenses @ 550nm
Temporal noise (analog domain)	20 e-	Pipelined global shutter (GS) with correlated double sampling (CDS)
Dynamic range	60 dB	
Pixel type	Global shutter pixel	Allows fixed pattern noise correction and reset (kTC) noise canceling through correlated double sampling.
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.
Parasitic light sensitivity - Shutter efficiency	<1/50 000 >99.998%	
Color filters	Optional	RGB Bayer pattern
Micro lenses	Yes	
QE * FF	65%	@ 550 nm with micro lenses.
Dark current signal	125 e/s	@ 25C die temperature
DSNU	12 LSB/s	12 bit mode
Fixed pattern noise	<4 LSB RMS	<0.1% of full swing, 12 bit mode
PRNU	< 1% RMS of signal	
LVDS Output channel	4	Each data output running @ 300 Mbit/s. 2 and 1 outputs selectable at reduced frame rate. Parallel CMOS output available
Frame rate	480 frames/s	Using a 12bit/pixel and 480 Mbit/s LVDS output. Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	4 analog gain settings
Programmable Registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time, flipped readout in x and y direction …
Supported HDR modes	Interleaved integration times Piecewise linear response	Interleaved exposure times for different columns: Odd columns (double rows for color) have a different exposure compared to even columns (double columns for color). Final image is a combination of the two (through interpolation). Response curve with two kneepoints
ADC	12bit	Column ADC
Interface	LVDS or CMOS parallel	Serial output data + synchronization signals

Specification	Value	Comment
I/O logic levels	LVDS = 1.8V Logic levels = 3.3V, 1.8V	
Supply voltages	2.2 & 3.3 V	3.3V for the pixel array and analog circuits 2.2V for digital circuits and the LVDS drivers
Clock inputs	CLK_IN	Between 10 and 40MHz
Power	700 mW	At 40MHz
Package	CSP	Chip scale package (8 x 8 BGA pins)
Operating range	-30C to +70C	Dark current and noise performance will degrade at higher temperature
Cover glass	D263	Plain glass, no IR cut-off filter on color devices

11 ORDERING INFO

Part Number	Chroma	Microlens	Package	Glass	Max speed
CMV300ES-2E7M1WP	Mono	yes	Chip scale package BGA	plain	25MHz
CMV300ES-2E7C1WP	RGB Bayer	yes	Chip scale package BGA	plain	25MHz
CMV300ES-3E7M1WP	Mono	yes	Chip scale package BGA	plain	40MHz
CMV300ES-3E7C1WP	RGB Bayer	yes	Chip scale package BGA	plain	40MHz

On request the package and cover glass can be customized. For options, pricing and delivery time please contact info@cmosis.com.

12 HANDLING AND SOLDERING PROCEDURE

12.1 SOLDERING

12.1.1 WAVE SOLDERING

Wave soldering is possible but not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. See the figure below for the wave soldering profile.

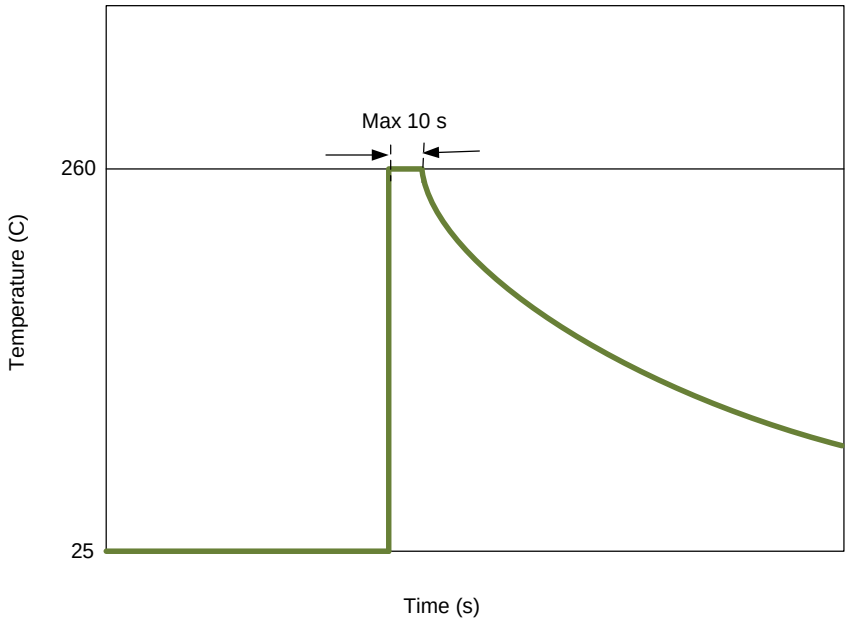


FIGURE 44: WAVE SOLDER PROFILE

12.1.2 REFLOW SOLDERING

The figure below shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

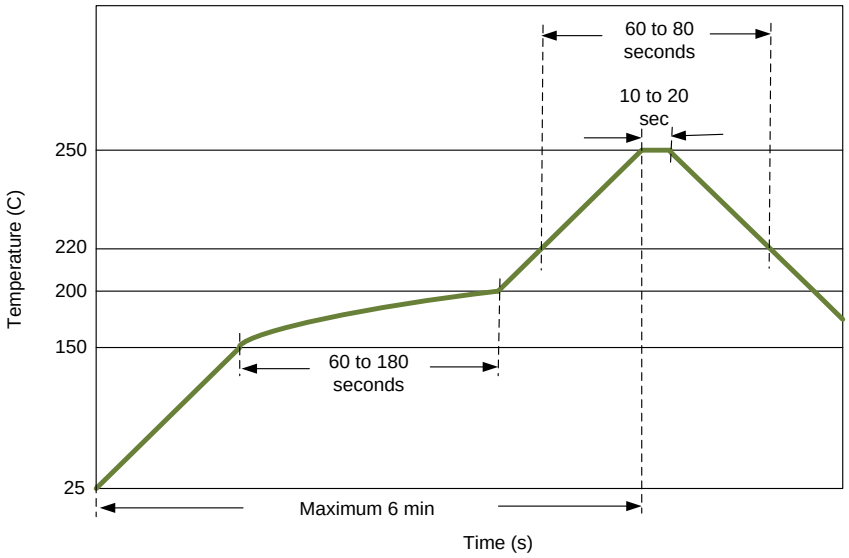


FIGURE 45: REFLOW SOLDER PROFILE

12.1.3 SOLDERING RECOMMENDATIONS

Image sensors with color filter arrays (CFA) and micro-lenses are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. Best solution will be flow soldering or manual soldering of a socket (through hole or BGA) and plug in the sensor at latest stage of the assembly/test process.

12.2 HANDLING IMAGE SENSORS

12.2.1 ESD

The following are the recommended minimum ESD requirements when handling image sensors.

1. Ground workspace (tables, floors…)
2. Ground handling personnel (wrist straps, special footwear…)
3. Minimize static charging (control humidity, use ionized air, wear gloves…)

12.2.2 GLASS CLEANING

When cleaning of the cover glass is needed we recommend the following two methods.

1. Blowing off the particles with ionized nitrogen
2. Wipe clean using IPA (isopropyl alcohol) and ESD protective wipes.

12.2.3 IMAGE SENSOR STORING

Image sensors should be stored under the following conditions

1. Dust free
2. Temperature 20°C to 40°C
3. Humidity between 30% and 60%.
4. Avoid radiation, electromagnetic fields, ESD, mechanical stress

13 ADDITIONAL INFORMATION

For any additional questions related to the operation and specification of the CMV300 imagers or feedback with respect to the present data sheet please contact techsupport@cmosis.com.