ASHUTHOSH M. R.

M. Tech (by Research) Student in Electronics and Communication Engineering

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WORK EXPERIENCE

Research Assistant

CHIPS, PES University Research Foundation

September 2020 – Ongoing Bengaluru, IN

- Worked on projects involving accelerating matrix multiplication on FPGAs, accelerating graph algorithms using RISC-V based FPGA overlays.
- Assisted in RISC-V on FPGA lab sessions for undergraduate students.

Research Assistant - Intern

CAcHe Lab, Amrita Vishwa Vidyapeetham

January 2020 – May 2020 Remote

- This research was conducted as part of the ECHO(Error Correcting Codes in High performance and parallel architectures) Indo-Portugal project.
- Our work focused on creating robust GF(2^m) NB-LDPC decoder designs on FPGA, comparing performance metrics against GPUs

PUBLICATIONS

Patent

- M. Purnaprajna, **A. M. Ravikumar**, and S. Krishna, "Run-time reconfigurable accelerator for matrix multiplication," in US Patent Application US20230029761A1, 2021.

Journal Articles

- S. Subramaniyan, O. Ferraz, **M. R. Ashuthosh**, *et al.*, "Enabling high-level design strategies for high-throughput and low-power NB-LDPC decoders," *IEEE Design Test Journal*, vol. 40, 2022.

Conference Proceedings

- **M. R. Ashuthosh**, S. Krishna, V. Sudarshan, S. Subramaniyan, and M. Purnaprajna, "MAPPARAT: A resource constrained fpga-based accelerator for sparse-dense matrix multiplication," in *35th International Conference on VLSI Design and 21st International Conference on Embedded Systems (VLSID) (Best Paper Award)*, Bengaluru, India, 2022.
- S. Subramaniyan, O. Ferraz, **M. R. Ashuthosh**, *et al.*, "Pushing the limits of energy efficiency for non-binary LDPC decoders on GPUs and FPGAs," in *IEEE Workshop on Signal Processing Systems (SiPS)*, Coimbra, Portugal, 2020.

Poster

- **M. R. Ashuthosh**, A. Vinay, K. K. Nagar, and M. Purnaprajna, "Accelerating BFS algorithm on a RISC-V based many-core cluster," in *30th IEEE International Conference on High Performance Computing, Data, Analytics, Student Research Symposium*, Goa, India, 2023.

SUMMARY

I am a second-year M. Tech student at Centre for Heterogeneous and Intelligent Processing Systems advised by Prof. Madhura Purnaprajna. My research interests include designing digital systems on FPGAs, parallel computer architecture and graph algorithms.

EDUCATION

M. Tech (by Research)

PES University

May 2022 – Ongoing

- Advised by Prof. Madhura Purnaprajna
- Working on accelerating graph algorithms on custom architectures.

B.E. in Electronics and Communication Engineering

PESIT - Bangalore South Campus

August 2016 – July 2020

- Graduated with 7.96/10 CGPA

SKILLS

Verilog HDL & FPGAs | RISC-V | OpenMP | LaTeX | Python | Verilator | Ubuntu

NPTEL CERTIFICATIONS

- Computer Architecture : 80% (Topper's list)
- Introduction to Parallel Programming with OpenMP and MPI : 75% (Topper's list)
- VLSI Design Flow: RTL to GDS : 80%
- C-based VLSI Design : 75%

LEISURE

Astro-Photography | Watching F1, football

LANGUAGES

Kannada
English
Hindi
Tulu
Malayalam
German