MOD -5 SYNCHRONOUS COUNTER

OBJECTIVE :

1.Design a mod-5 synchronous counter using JK Flip Flop.

Criteria :

2.Take PMOS width to be 400nm and NMOS width to be 200nm.

3. 250MHz clock frequency.

 4 Draw a transistor level schematic for each gate and use those gates to create higher level blocks.

5 Verify that the schematic works as intended.

6. Draw a layout for the entire design from scratch.

7. Aim for minimum possible area with rectangular shaped layout with height as 1400nm.

8. Clear the DRC errors ,verify the LVS and perform a PEX analysis.

Components :-

   1) Inverter
   2) NAND Gate(3-input)
   3) NAND Gate(2-input)
   4) AND Gate(To reduce the output states)

Output states of a MOD 5 counter:

1) 000 =0
2) 001 =1
3) 010 =2
4) 011 =3
5) 100 =4

Mod 5 counter specifications:

1) Simulation frequency = 250MHz

   i.e. time period of clock pulse = 4ns

2) Dimensions :

   Height = 1400nm=1.4 micrometer (meeting with criteria)

   Length= 127 micrometer
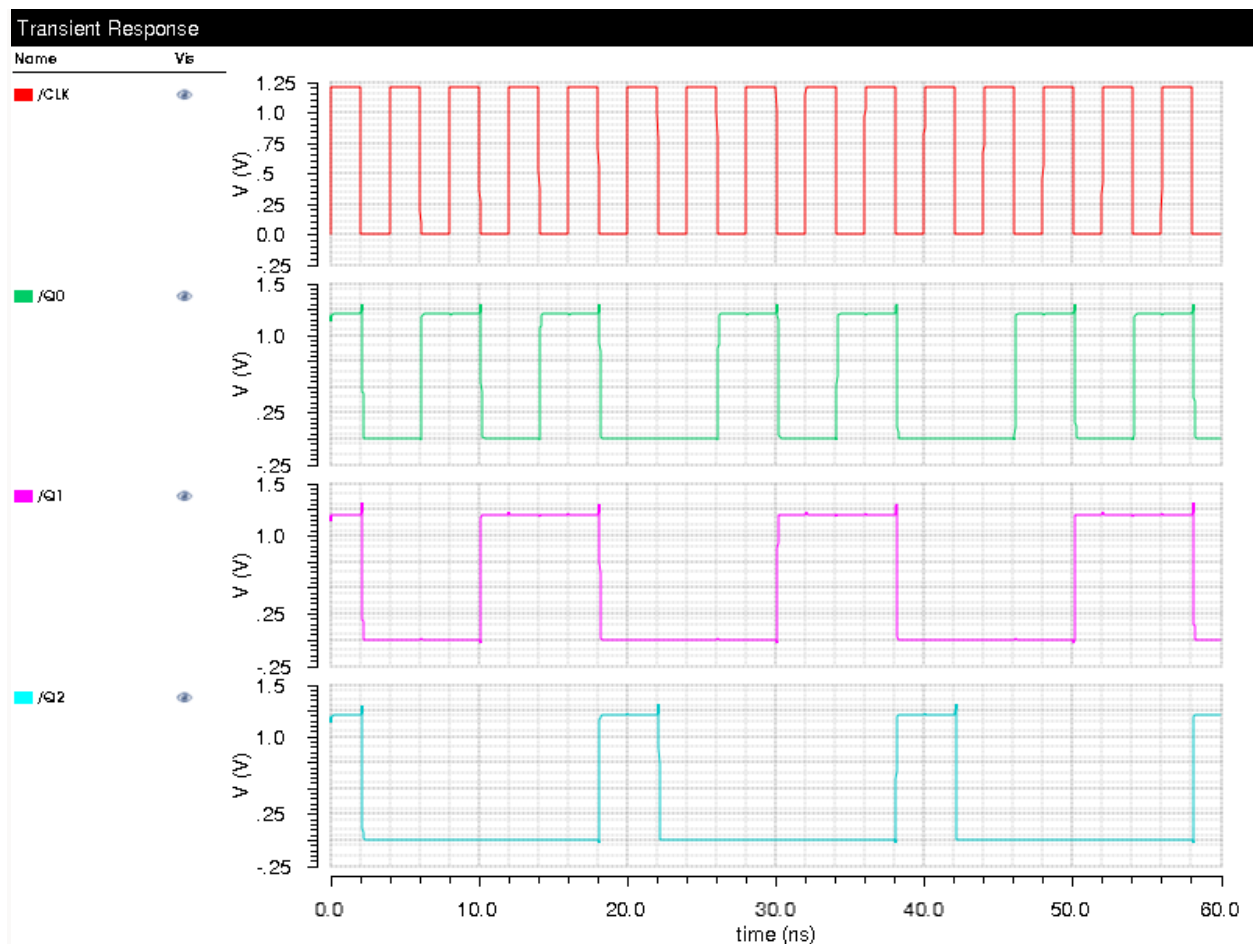
   Area = 177.8 micrometer square.

3) DRC is clear . DRC report is uploaded.

4) LVS is clear. Lvs report is uploaded.

5) PEX analysis and report uploaded.

All basic criteria are fulfilled successfully. And counter works properly.

Transient response of Counter is shown below
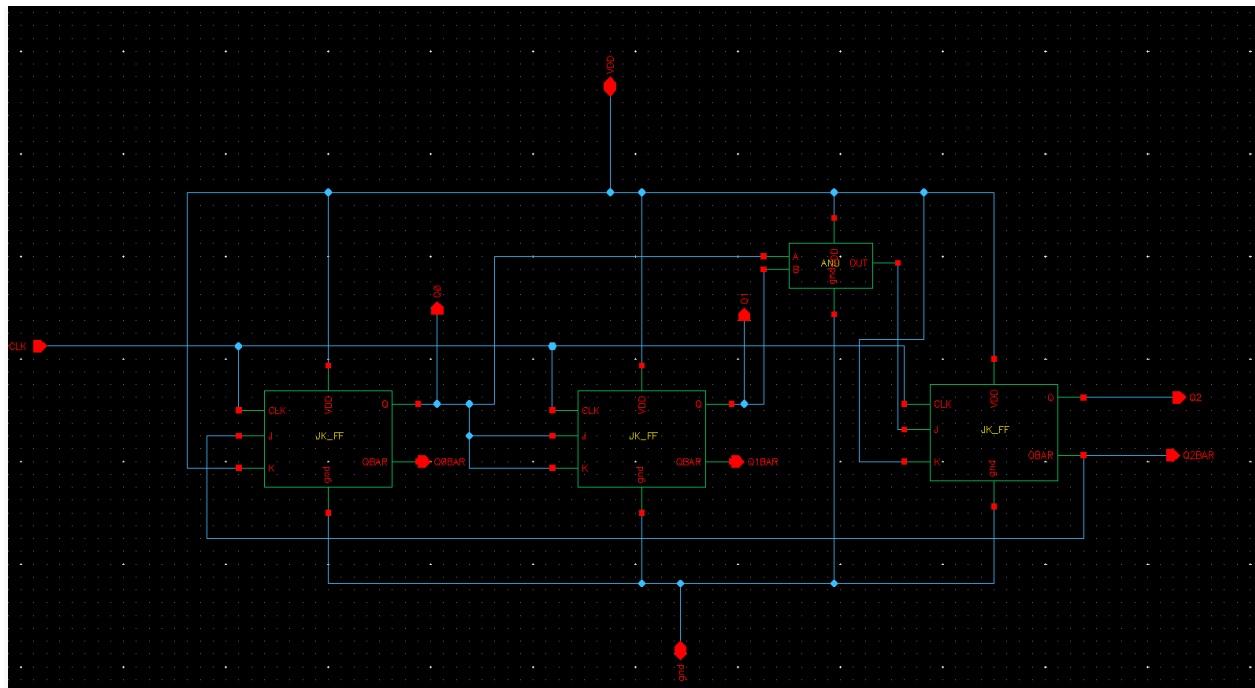

The waveform shows the all 5 states of a MOD 5 counter.

Where,   Q0, Q1, Q2 are the outputs .

    And ,   Q0= LSB and Q2= MSB.

Schematic of counter is shown below:

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