https://eee.uiu.ac.bd/research/cadence-at-uiu/

News

May 6, 2025 Research Opportunity for StudentsFebruary 4, 2025 UIU students successfully visited the United Power Generation and Distribution Company Limited (UPGDCL) Power Plant in the Dhaka Export Processing Zone (DEPZ)January 28, 2025 Successful Completion of Internship program from United Power Plant.January 27, 2025 Seminar on VLSI, Semiconductor Industry, and Career Opportunities with Ulkasemi Successfully Organized at UIUJanuary 21, 2025 Successful Completion of Seminar on Battery Energy Storage Systems (BESS) View more

Notices

June 30, 2025 Advising (Time & Section Selection): Summer 2025 TrimesterJune 30, 2025 Class Routine Summer 2025 BSEEEJune 23, 2025 Notice for Course Evaluation & Instructions Spring 2025June 16, 2025 NOTICE for Course Pre Advising(Summer 2025)June 16, 2025 Exam Template for Summer 2025 Department of EEE View more

Events

April 24, 2025 1:00 pm IEEE PES DAY 2025 at UIUJanuary 19, 2025 2:45 pm Seminar on â€œBESS Solution â€" For Better Energy Flexibility and Controllability,â€January 21, 2025 2:30 pm ð„ð±ðœð¥ð®ð¬ð¢ð¯ ðž ð'ðžð¦ð¢ð§ðšð« ð¨ð§ ð•ð‹ð'ð^, ð'ðžð¦ð¢ðœðžð¨ð§ðð®ðœðð¨ð« ð^ð§ðð®ð¬ðð«ð², ðšð§ð ð"ð¥ð¤ðšð¬ð¬ðžð¦ð¢!January 11, 2025 2:00 pm Seminar on â€œPower Sector Job Opportunities in Bangladesh and Preparation Guidelinesâ€January 1, 2025 2:30 pm ð'ðžð¦ð¢ðœðžð¨ð§ðð®ðœðð¨ð« (ð'ð¢ð¥ð¢ðœðžð¨ð§) ð^ð§ðð®ð¬ðð«ð² ðŽð¯ðžð«ð¬ð¢ðžð°° View more

Cadence at UIU

With large scale global proliferation of electronic devices among consumers, there are numerous opportunities for sustainable growth of the semiconductor design industries in Bangladesh that could create a big job market for design engineers in this country. Bangladesh held bright promise for entrepreneurs in the VLSI field, and with support from the academia and the government VLSI industries would be thriving and would induce investment from multinational companies. In order to train our students properly for the job market, UIU introduced specialized VLSI design courses with support tool like Cadence. UIU purchased Cadence tool suite for Tk. 2.2 M for three yearsâ€™ license and encouraged widespread usage of this tool to generate the future skilled workforce for VLSI design industries. In this context, Dept. of EEE comes forward with different activities and future plans to make the best possible utilization of this costly software for the greater interest of the EEE students as well as of the country.

Activities Taken by the Dept. of EEE:

Department of EEE of UIU took initiatives to motivate the students to enhance their participation in the field of Electronics in general and in the VLSI arena, in particular. Some of these initiatives include 1. Arrangement of three seminars in collaboration with local semiconductor industries like sBIT, ULKASEMI, BaySand and PrimeSilicon to showcase the

prospects of the future job market in IC design 2. Arrangement of two 2-day long workshops on using Cadence tool suite in VLSI and analog IC design respectively for the students who have recently completed the VLSI courses in order to prepare them for the job market 3. A computer laboratory furnished with state-of-the-art computers is completely dedicated for the students who intend to work and practice with the Cadence tool suite in addition to the regular lab activities. This lab is recently named as "VLSI Design Center". 4. Laboratory experiments based on Cadence tool suite are incorporated in the Electronics (EEE 208) and Digital Electronics (EEE 224) courses starting from the Fall 2014 trimester. About ten VLSI and/or analog IC design based topics are offered and carried out as undergraduate thesis/project (EEE 400).

Future Plans:

For the maximum utilization of the purchased Cadence tool suite, the department is working on some activities which include- 1. Arrange multiple training courses and/or sessions on the digital and analog IC design in each trimester. The target audience of these seminars will be the final semester students. 2. Introduce advanced courses on the digital/analog/mixed-signal IC design so that students would be prepared for the changing demand in the semiconductor industry. 3. Commence collaborative Research and Development (R&D) activities with the above-mentioned companies to design new Intellectual Property (IP) and enhance existing IPs 4. Recently sBIT and BaySand requested to work with EEE, UIU to manage financial supports and/or grants from the University Grants Commission as well as from the Science and Information Ministry of Bangladesh. Initiatives and activities are in progress to address the requests. 5. In addition to above-mentioned efforts, EEE also plans to improve the skill of the students of the neighboring universities to help create a very prospective workforce so that the multinational companies would be eager to invest for analog/digital/mixed-signal IC design in Bangladesh 6. of EEE also have plans to arrange workshops on a regular basis to train the faculty members of other universities to keep them updated with advancement of IC design related issues. Following this plan, EEE will host a day long workshop organized by a company (sBIT) in the upcoming 14th March, 2015.

Electronic Course Curriculum

Electronics I

P-N junction as a circuit element: Intrinsic and extrinsic semiconductors, operational principle of p-n junction diode, contact potential, current-voltage characteristics of a diode, simplified dc and ac diode models, dynamic resistance and capacitance. Diode circuits: Half wave and full wave rectifiers, rectifiers with filter capacitor, characteristics of a zener diode, zener shunt regulator, clamping and clipping circuits. Bipolar junction transistor (BJT) as a circuit element: Basic structure. BJT characteristics and regions of operation, BJT as an amplifier, biasing the BJT for discrete circuits, small signal equivalent circuit models, BJT as a switch. Single stage BJT amplifier circuits and their configurations: Voltage and current gain, input and output impedances. Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) as circuit element: structure and physical operation of MOSFETs, body effect, current- voltage characteristics of MOSFETs, biasing discrete and integrated MOS amplifier circuits, single-stage MOS amplifiers, MOSFET as a switch, CMOS inverter. Junction Field-Effect-Transistor (JFET): Structure and physical operation of JFET, transistor characteristics.

Simulation Lab

Simulation laboratory based on EEE 101, EEE 103 and EEE 105 theory courses. Students will verify the theories and concepts learned in EEE 101, EEE 103 and EEE 105 using simulation software like PSpice and Matlab. Students will also perform specific design of DC and AC circuits theoretically and by simulation. Students will learn how to write and debug programs for simulation of different mathematical models.

Electronics II

Frequency response of amplifiers: Poles, zeros and Bode plots, amplifier transfer function, techniques of determining 3 dB frequencies of amplifier circuits, frequency response of single-stage and cascade amplifiers, frequency response of differential amplifiers. Operational amplifiers (Op-Amp): Properties of ideal Op-Amps, non-inverting and inverting amplifiers, inverting integrators, differentiator, weighted summer and other applications of Op-Amp circuits, effects of finite open loop gain and bandwidth on circuit performance, logic signal operation of Op-Amp, dc imperfections. General purpose Op-Amp: DC analysis, small-signal analysis of different stages, gain and frequency response of 741 Op-Amp. Negative feedback: properties, basic topologies, feedback amplifiers with different topologies, stability, frequency compensation. Active filters: Different types of filters and specifications, transfer functions, realization of first and second order low, high and band pass filters using Op-Amps. Signal generators: Basic principle of sinusoidal oscillation, Op-Amp RC oscillators, LC and crystal oscillators. Power Amplifiers: Classification of output stages, class A, B and AB output stages.

Electronics Lab

This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 201 and EEE 207. In the second part, students will design simple systems using the principles learned in EEE 201 and EEE 207.

Digital Electronics

Number systems and codes: number system, arithmetic, base conversion, signed number representation and computer codes. Analysis and synthesis of logic circuits: Boolean algebra, switching functions, switching circuits and combinational logic circuits. Simplification of switching functions: K maps, QuineMcCluskey minimization method and Patrick's algorithm. Modular combinational circuit design: decoders, encoders, multiplexers, demultiplexers, binary arithmetic elements and comparators. Programmable logic devices: logic arrays, field programmable logic arrays, programmable read only memory and programmable array logic. Sequential devices: latches, flip-flops and timing circuits. Modular sequential logic circuits: shift registers, counters and digital fraction rate multipliers. Simple processors: simple digital system design.

Digital Electronics Lab

This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 223. In the second part, students will design simple systems using the principles learned in EEE 223.

Optoelectronics

Optical properties in semiconductor: Direct and indirect band-gap materials, radiative and non-radiative recombination, optical absorption, photo-generated excess carriers, minority carrier life time, luminescence and quantum efficiency in radiation. Properties of light: Particle and wave nature of light, polarization, interference, diffraction and blackbody radiation. Light emitting diode (LED): Principles, materials for visible and infrared LED, internal and external efficiency, loss mechanism, structure and coupling to optical fibers. Stimulated emission and light amplification: Spontaneous and stimulated emission, Einstein relations, population inversion, absorption of radiation, optical feedback and threshold conditions. Semiconductor Lasers: Population inversion in degenerate semiconductors, laser cavity, operating wavelength, threshold current density, power output, optical and electrical confinement. Introduction to quantum well lasers. Photo-detectors: Photoconductors, junction photo-detectors, PIN detectors, avalanche photodiodes and phototransistors. Solar cells: Solar energy and spectrum, silicon and schottky solar cells. Modulation of light: Phase and amplitude modulation, electro-optic effect, acousto-optic effect and magento-optic devices. Introduction to integrated optics.

Analog Integrated Circuits

Review of FET amplifiers: Passive and active loads and frequency limitation. Current mirror: Basic, cascade and active current mirror. Differential Amplifier: Introduction, large and small signal analysis, common mode analysis and differential amplifier with active load Noise: Introduction to noise, types, representation in circuits, noise in single stage and differential amplifiers and bandwidth. Band-gap references: Supply voltage independent biasing, temperature independent biasing, proportional to absolute temperature current generation and constant trans-conductance biasing. Switch capacitor circuits: Sampling switches, switched capacitor circuits including unity gain buffer, amplifier and integrator. Phase Locked Loop (PLL): Introduction, basic PLL and charge pumped PLL.

Semiconductor Device Theory

Lattice vibration: Simple harmonic model, dispersion relation, acoustic and optical phonons. Band structure: Isotropic and anisotropic crystals, band diagrams and effective masses of different semiconductors and alloys. Scattering theory: Review of classical theory, Fermi-Golden rule, scattering rates of different processes, scattering mechanisms in different semiconductors, mobility. Different carrier transport models: Drift-diffusion theory, ambipolar transport, hydrodynamic model, Boltzmann transport equations, quantum mechanical model, simple applications.

Solid State Devices

Semiconductors in equilibrium: Energy bands, intrinsic and extrinsic semiconductors, Fermi levels, electron and hole concentrations, temperature dependence of carrier concentrations and invariance of Fermi level. Carrier transport processes and excess carriers: Drift and diffusion, generation and recombination of excess carriers, built-in-field, Einstein relations, continuity and diffusion equations for holes and electrons and quasi-Fermi level. PN junction: Basic structure,

equilibrium conditions, contact potential, equilibrium Fermi level, space charge, non-equilibrium condition, forward and reverse bias, carrier injection, minority and majority carrier currents, transient and ac conditions, time variation of stored charge, reverse recovery transient and capacitance. Bipolar junction transistor: Basic principle of pnp and npn transistors, emitter efficiency, base transport factor and current gain, diffusion equation in the base, terminal currents, coupled-diode model and charge control analysis, Ebers-Moll equations and circuit synthesis. Metal-semiconductor junction: Energy band diagram of metal semiconductor junctions, rectifying and ohmic contacts. MOS structure: MOS capacitor, energy band diagrams and flat band voltage, threshold voltage and control of threshold voltage, static C-V characteristics, qualitative theory of MOSFET operation, body effect and current-voltage relationship of a MOSFET. Junction Field-effect-transistor: Introduction, qualitative theory of operation, pinch-off voltage and current-voltage relationship.

VLSI Design

VLSI technology: Top down design approach, technology trends and design styles. Review of MOS transistor theory: Threshold voltage, body effect, I-V equations and characteristics, latch-up problems, NMOS inverter, CMOS inverter, pass-transistor and transmission gates. CMOS circuit characteristics and performance estimation: Resistance, capacitance, rise and fall times, delay, gate transistor sizing and power consumption. CMOS circuit and logic design: Layout design rules and physical design of simple logic gates. CMOS subsystem design: Adders, multiplier and memory system, arithmetic logic unit. Programmable logic arrays.I/O systems.VLSI testing.

VLSI Design Laboratory

This course consists of two parts. In the first part, students will perform experiments to verify practically the theories and concepts learned in EEE 441. In the second part, students will design simple systems using the principles learned in EEE 441.

Semiconductor Processing and Fabrication technology

Substrate materials: Crystal growth and wafer preparation, epitaxial growth technique, molecular beam epitaxy, chemical vapor phase epitaxy and chemical vapor deposition (CVD). Doping techniques: Diffusion and ion implantation. Growth and deposition of dielectric layers: Thermal oxidation, CVD, plasma CVD, sputtering and silicon-nitride growth. Etching: Wet chemical etching, silicon and GaAs etching, anisotropic etching, selective etching, dry physical etching, ion beam etching, sputtering etching and reactive ion etching. Cleaning: Surface cleaning, organic cleaning and RCA cleaning. Lithography: Photo-reactive materials, pattern generation, pattern transfer and metalization. Discrete device fabrication: Diode, transistor, resistor and capacitor. Integrated circuit fabrication: Isolation â€" pn junction isolation, mesa isolation and oxide isolation. BJT based microcircuits, p-channel and n-channel MOSFETs, complimentary MOSFETs and silicon on insulator devices. Testing, bonding and packaging.

Licensed Cadence Tool Set

Brief List of Cadence Tool Suites, Licensed for 3 Years: 1. The Custom IC Bundle (including Analog/RF/AMS) 1. Virtuoso AMS Designer Environment 2. Virtuoso Analog Design Environment -XL 2. Device Modeling 1. Virtuoso Advanced Device Modeling (for Eldo / HSPICE) 3. Digital Integrated Circuits Bundle 1. First Encounter â€"XL 2. ETS Advanced Analysis GXL Option 4. Verification Bundle 1. Conformal 2. Assura 3. Incisive 5. DFM Bundle 1. Voltage Storm 2. Encounter Power System 6. DFT Bundle 1. RC â€" DFT Architect Basic/Advanced 2. Encounter Trur Time ATPG Basic 7. Characterization Bundle 1. Virtuoso Liberate 2. Virtuoso Variety 3. Virtuoso AMS Designer Verification 4. Virtuoso MM Simulation 5. Virtuoso Power System XL 8. Chip Planning Bundle 1. Cadence InCyte Chip Estimator -XL 9. Signal Integrity Bundle 1. Encounter Timing System -XL 2. PACIFIC61 3. Encounter Library Characterizer -XL 10. PCB Bundle 1. Allegro 2. PCB Design Studio 3. PCB Librarian Expert 11. Synthesis 1. Encounter RTL Compiler

Faculty Biographies

Dr Md. Iqbal Bahar Chowdhury is currently working as an Associate Professor in the Department of Electrical and Electronic Engineering at United International University (UIU). He has been teaching at various positions in different Universities since 1997. He received his B.Sc., M.Sc. and Ph.D. degrees from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, in 1996, 2000 and 2011 respectively, all in Electrical and Electronic Engineering (EEE). His Doctoral thesis topic was â€œEffect of Majority Carrier Current Density on the Base Transit Time of Bipolar Junction Transistorsâ€. He has published about forty journal and conference papers and has attended more than fifteen training sessions, conferences and workshops. He worked as reviewer for many international conferences and journals including IEEE Transaction. He has supervised more than thirty undergraduate thesis works. He is a member of Institute of Engineers, Bangladesh (IEB). Usually he conducs research in the field of modeling solid state devices which include

MOSFETs, BJTs and solar cells of modern structures. But recently he focuses his research to design various digital and analog integrated circuits by applying and/or developing models of various modern MOS structures using Cadence.
Monjurul Feeroz Meem has received his B. Sc. degree in Electrical and Electronic Engineering from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 2014. He is currently pursuing his M. Sc degree at Bangladesh University of Engineering and Technology. His undergrad thesis was on â€œModeling and Performance Analysis of GrapheneNanoribbon Interconnectâ€ under the supervision of Dr. A.B.M. Harun-Ur-Rashid, Professor, Dept. of Electrical and Electronic Engineering, BUET. He is serving as a Lecturer in the Department of Electrical and Electronic Engineering of United International University since September, 2014. He had taught Electrical Properties of Materials and Programming courses at UIU. His research interests are in the areas of Graphenenanoribbon interconnect, GNR FET, Nanotechnology and VLSI circuits. **Salahuddin Ahmed** has received his BS and MS degrees from Wright State University, USA in 1996 and 1998 respectively, both in Computer Engineering. He worked as Software Engineer in corporate R&D of Lexis-Nexis, USA for two years where he co-invented five US patents and developed a smart query processing engine. Then he joined Qualcomm Inc, USA as place and route (P&R) engineer. During his eight year service there, he has done tapeouts of many baseband MSM (Mobile Station Modem) chips from 180nm process down to 45nm process. He worked as the technical lead of the P&R team while migrating from 65nm to 45nm process. While at Qualcomm he has done extensive work on power saving techniques such as clock gating, power shut down of hard macros using head switch/foot switch methodologies etc. He had developed the SOC flows for stack-die, flip-chip etc. using Cadence and Synopsys tool suites. He had written many scripts to automate the tapeout flow that reduced the tapeout time and human error significantly. He moved to Bangladesh in 2008 and joined EEE department of United International University (UIU) as Assistant Professor. He had taught Microprocessor, Digital Electronics, Programming and VLSI courses at UIU. His research interest includes deep sub-micron process, low-power design and computer aided design (CAD) tools development. **Dr. Raqibul Mostafa** is currently a Professor in the Electrical and Electronic Engineering (EEE) department at the United International University (UIU) where he has been teaching and conducting research since June 2009. He received his Ph.D. and M.S. degrees in Electrical and Computer Engineering from Virginia Tech (VT) in 2003, and 1995 respectively. His Doctoral thesis topic was â€œFeasibility of Smart Antennas for Small Wireless Terminalsâ€, supervised by Dr. Jeffrey H. Reed. Dr. Mostafa obtained his B.Sc. degree in EEE from Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh in 1991 with First class Honors and served as a lecturer in the EEE Dept., BUET from January 1992 to July 1993. Prior to joining UIU, he worked as Senior Engineer in corporate R&D of Qualcomm Inc, USA for five years where he was involved in Standardization Efforts, Performance Specifications regarding UMTS and cdma2000 wireless standards. He served as a Director of Bangladesh Submarine Cable Company Limited (BSCCL) from 2010 to 2014. He is currently serving as the Head of EEE Dept of UIU. He participated in different wireless communications projects sponsored by ITT, National Science Foundation (NSF), Texas Instrument (TI), LGIC, Samsung and US Navy. He has published over 35 papers in journals and in peer reviewed conference proceedings. Dr. Mostafa served as a reviewer for many international conferences and journals including IEEE Transactions on Wireless Communications and IEEE Transactions on Vehicular Technology. His research interests include Wireless communications with focus on smart antenna applications, Signal processing and DSP prototyping of communications systems, Software radio, LTE Networks, wireless communications standards and biomedical signal processing. Dr. Mostafa is a Senior Member of IEEE.

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