CHAPTER 19

Electronic Devices

CHAPTER HIGHLIGHTS

Semiconductors; semiconductor diode: I-V characteristics in forward and reverse bias; diode as a rectifier; I-V characteristics of LED, photodiode, solar cell and Zener diode; Zener diode as a voltage regulator. Junction transistor, transistor action, characteristics of a transistor; transistor as an amplifier (common emitter configuration) and oscillator. Logic gates (OR, AND, NOT, NAND and NOR). Transistor as a switch.

BRIEF REVIEW

We can have four types of conductors:

(a) super conductors
(b) good conductors
(c) semiconductors
(d) bad conductors or insulators

Superconductivity was first discovered by K. Onnes in 1911.

Super conductors have zero resistance at low temperatures below a certain maximum called critical temperature. They are perfect diamagnets (Meissner effect). If temperature is greater than a critical temperature T_C, they become normal conductors. They become normal conductor even if a magnetic field greater than critical magnetic field is applied. BCS (Bardeen Cooper Schereffer) theory, according to this theory current is carried by electron pair called cooper pair instead of individual electrons. The highest temperature at which superconductor is known is 160 K. Note that cooper pair is a boson. Though, yet new theory has not arrived but there is little evidence that at high temperature electron pair could exist.

Good conductors are metals. Their resistivity increases with rise in temperature according to

$$\rho\,(T) = \rho_{(o)}\,[1 + \alpha\, T]$$

Semiconductors have a unique property that their conductivity increases with rise in temperature. Fig. 19.1 illustrates how resistivity falls with rise in temperature. This phenomenon can be explained on the basis of band theory. The energy bands which are completely filled at 0 *K* are called valence bands. The bands with higher energy are called conduction bands. We will refer to valence band as the top most filled band and conduction band as lowest conduction band. E_v is the topmost energy of valence band and E_c is the bottom most energy of conduction band, the $E_g = E_c - E_v$ represents forbidden energy gap.

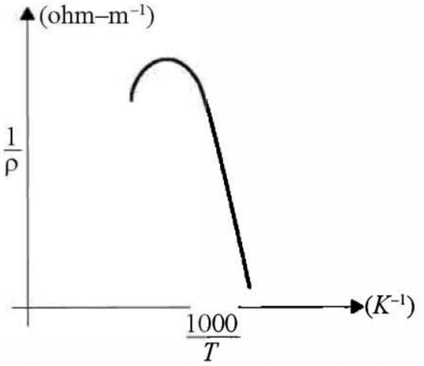


Fig. 19.1 Variation of resistivity vs temperature in a semiconductor

In metals $E_g \to 0$, that is, valence band and conduction band overlap so that a large number of electrons lie in the conduction band.

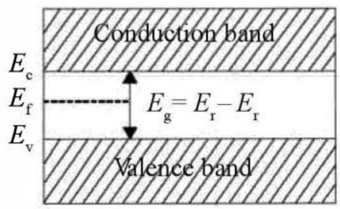


Fig. 19.2 Energy band diagram of a semiconductor

In semiconductors $E_g \sim 1$ eV. At room temperature it is about 1–2 % filled. At 0 K semiconductor is a perfect insulator. Fermi level is an imaginary level which lies between valence band and conduction band such that the probability of finding an electron is 50 % or $\frac{1}{2}$.

At 0 K Fermi level is the highest filled level. Fermi level is used as reference level.

E_g (for Ge) = 0.71 eV and E_g (for Si) = 1.12 eV

In insulator, $E_g \sim 6$ eV. For example, E_g (for diamond) = 6.3 eV

Semiconductors are of two types (a) intrinsic (b) extrinsic or doped semiconductors.

In intrinsic semiconductor no impurity, from 13th or 15th group of the periodic table has been added. So that density of holes in valence band is equal to density of electrons in conduction band, that is, $n_i = h_i$ where n is electron density and h is hole density (subscript 'i' stands for intrinsic).

Extrinsic semiconductor is of two types p-type and n-type. In p-type majority carriers are holes. Thus, $h_p > n_p$. Impurities from 13th group (*B, Al, Ga, In*) is added to make a semiconductor p-type. Such a type of impurity is called acceptor impurity. Acceptor level E_A lies very close to valence band (VB).

In n-type semiconductor majority carriers are electrons. It is made by doping donor impurity, i.e., impurity from 15th group of periodic table like P, As, Bi, Sb. Thus, $n_n > h_n$. Donor level lies very close to conduction band (CB).

In thermal equilibrium condition $n_e h_e = n_i^2$ (subscript e denotes extrinsic). Fig. 19.3 (a) and 19.3 (c) show energy band diagram for p- and n-type semiconductor. In heavily doped p- or n-type acceptor or donor impurity level lies inside *VB* and *CB* respectively. Fig. 19.3 (b) shows heavily doped p-type.

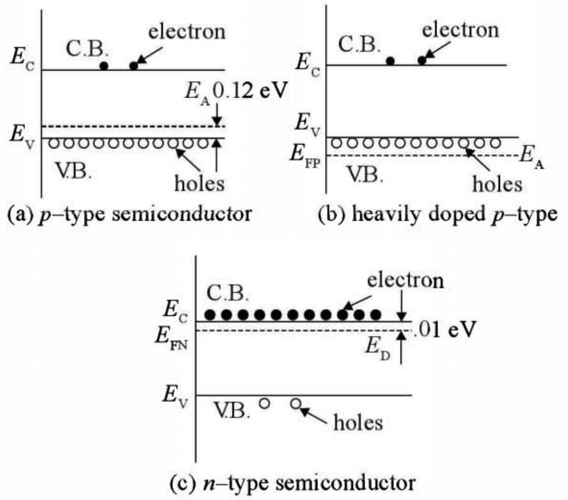


Fig. 19.3 Energy band diagram of extrinsic semiconductors.

Conductivity in semi conductors is due to holes and electrons both. Moreover, total conduction is due to diffusion and drift currents. In an intrinsic semiconductor, conductivity $\sigma = ne\,\mu_n + he\,\mu_h$

where μ_n and μ_h are mobility of electrons and holes respectively. For n-type semiconductor.

Assuming $n \cong N_D$

$\sigma = ne\,\mu_n = N_D e \mu_n$

For p-type semiconductor

Assuming $h \cong N_A$

$\sigma = he\,\mu_n = N_A e \mu_h$

pn junction When p- and n-type semiconductors of same material, either both of Si or both of *Ge* are fused together, or, n-type is grown on p-type, then such a device is called *pn* junction or semiconductor diode.

Potential barrier and Depletion layer Due to charge density gradient, electrons from n-type move towards p-type close to the junction and are accepted by acceptor impurity atoms present there. Similarly, holes from p-type ionize impurity atoms present close to the junction forming a **fictitious battery** V_B or **potential barrier** V_B. Potential barrier and depletion layer are illustrated in Fig. 19.4 (a) and 19.4 (b).

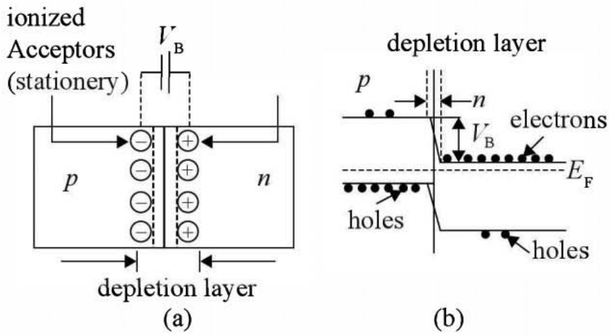


Fig. 19.4 (a) *pn* junction (b) Energy band diagram of a *p-n* junction

Depletion layer is the layer close to the junction devoid of carriers due to migration of charge carriers (electrons and holes) and acceptance by acceptor and donor impurity atoms.

Forward biasing If positive terminal of an external battery is connected to p-type and its negative terminal to n-type of the *pn* junction then such a biasing is called forward biasing. Forward biasing reduces potential barrier and hence, depletion layer width decreases. The current is due to majority carriers. See Fig. 19.5 (a) and Fig. 19.6. Current is quite large when applied, with forward voltage > V_B or V_r.

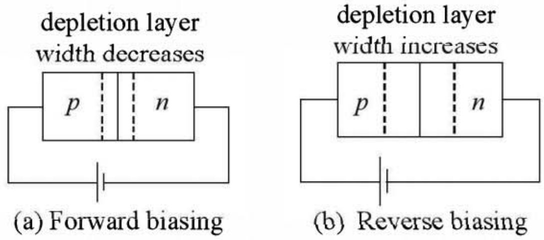


Fig. 19.5 Biasing of *p-n* junction

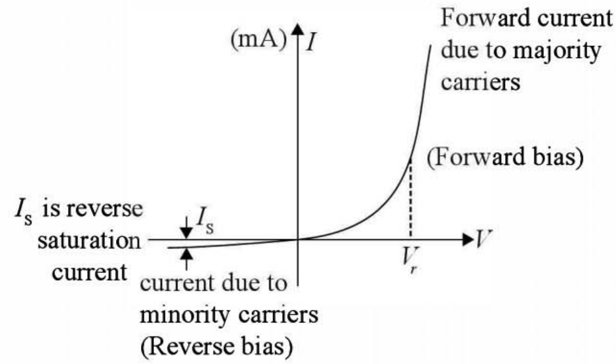


Fig. 19.6 Characteristics of pn junction

Reverse biasing If positive terminal of external battery is connected to n-type and negative terminal to *p*-type as shown in Fig. 19.5 (b), then such a biasing is called **reverse biasing** or **back biasing**. It increases the barrier potential and hence, depletion layer width. Extremely low current due to minority carrier flows. The current is nearly constant and is termed as reverse saturation current as shown in Fig. 19.6. Fig. 19.7 shows circuit symbol for an ideal diode. It is clear from characteristic curve shown in Fig. 19.6 that *pn* junction acts very closely like a valve.

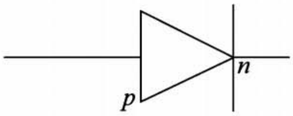


Fig. 19.7 Circuit symbol of an ideal pn junction

Equation of current in a *pn* junction $I = I_S\left[e^{V/V_T} - 1\right]$ where I_S is reverse saturation current, V is applied potential, V_T = thermal voltage $V_T = \dfrac{kT}{e} = 0.026$ V at 300 K where k is Boltzmann's constant, T is temperature (Kelvin) and e is charge on an electron.

Dynamic or Incremental Resistance

$r = \dfrac{\Delta V}{\Delta I} = \dfrac{dV}{dI}$ is called dynamic resistance. It may be determined from the characteristic curve as shown in Fig. 19.8. Its value is different at different points. From the diode equation $\dfrac{dI}{dV} = \dfrac{I_S}{V_T}e^{V/V_T} = \dfrac{I}{V_T}$

$$\text{or } r_f = \frac{dV}{dI} = \frac{V_T}{I} = \frac{26mV}{\text{Im}A} = 26\,\Omega$$

In forward bias I = 1 mA r_f = 26 Ω (low).

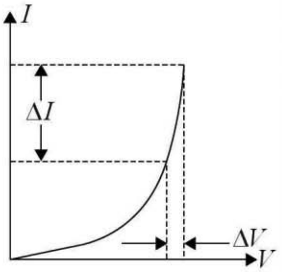


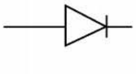
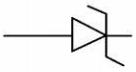
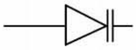
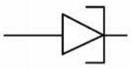
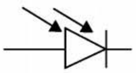
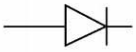
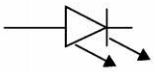
Fig. 19.8 Dynamic resistance determination

In reverse bias case $r_r = \dfrac{V_T}{I}$ as $I \to 0$, $r_r \to \infty$. In an actual diode $r_r \geq 10^4\ \Omega$.

Ideal diode Ideal diode is like a voltage controlled switch. When forward biased it acts like an ON switch (zero resistance) and when reverse biased it acts like an OFF switch (infinite resistance).

Table 19.1 lists some of important types of diodes and their applications along with their circuit symbols.

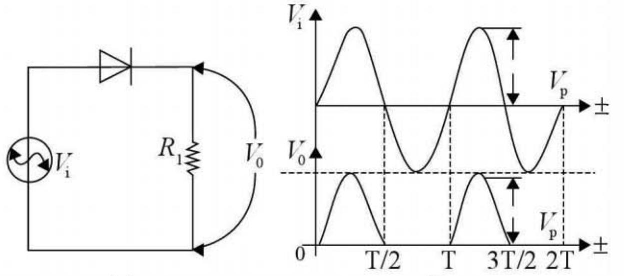
Table 19.1 Types of p-n junctions

Type of diode	*Circuit symbol*	*Applications*
1. General purpose diode		Demodulator, voltage multiplier clipping, clamping, rectifier, peak detector, waveshaping.
2. Avalanche or Zener or breakdown diode		Load regulator, reference voltage formation.
3. Varactor or Varicap		Frequency modulation (FM) voltage to frequency converter.
4. Tunnel diode or Esaki diode		Oscillator, Astable/ monostable multivibrator
5. Photo diode		Burglar alarm, fire alarm, remote sensing, automatic switching of light, nuclear detector, communication system
6. Switching diode		Logic gates
7. Light emitting diode (LED)		Indicator, remote control, optical fiber communication, system alpha-numeric (7-segment, 14-segment displays) devices.

Rectifier It converts AC to unidirectional pulsating output. In other words it converts AC to DC.

Rectifiers are of Two Types

(a) Half Wave Rectifier (b) Full Wave Rectifier



(a) Half wave rectifier (b) Its input/output characteristics

Fig. 19.9

Half-wave rectifier Fig. 19.9 (a) illustrates half wave rectifier and Fig. 19.9 (b) shows the input/output characteristics.

In a Half-Wave Rectifier

$$V_o = V_i = V_P \sin \Omega t \; 0 < t < \frac{T}{2}$$

$$V_o = 0 \quad \frac{T}{2} < t < T$$

$$V_{\text{out}}\,(dc) = \frac{V_P}{\pi}$$

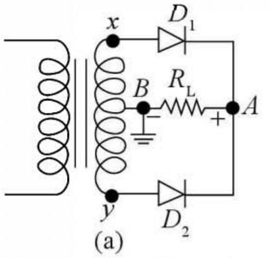
$$V_{\text{out}}\,(rms) = \frac{V_P}{2}.$$

$$\text{Ripple factor } \gamma = \frac{V_{AC}}{V_{DC}} = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1} = 1.21$$

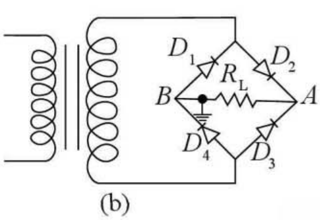
$$\text{Rectification efficiency } \eta = \frac{P_{DC}}{P_{rms}} \times 100 = 40.6\%$$

Frequency of output signal = frequency of input signal

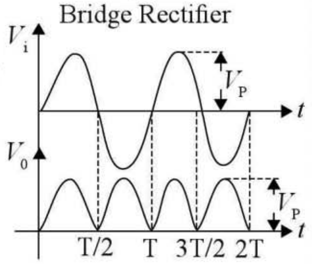
Full-wave rectifier gives output in both the half cycles. Circuit and input/output characteristic are shown in Fig. 19.10 (a), 19.10 (b) and 19.10 (c) respectively.



(a) Full-wave Rectifier using centre tapped transformer



(b) Bridge Rectifier



(c) Input/output characteristics

Fig. 19.10

Note that a full-wave rectifier can be made using a centre tapped transformer or a bridge rectifier.

For a Full-Wave Recitifier

$$V_o = V_i = V_P \sin \Omega t \quad 0 < t < \frac{T}{2}$$

$$V_o = -\,V_P \sin \Omega t \qquad \frac{T}{2} < t < T$$

$$V_{\text{out}}\,(\text{DC}) = \frac{2V_P}{\pi};$$

$$V_{\text{out}}\,(rms) = \frac{V_P}{\sqrt{2}}$$

$$\text{Ripple factor } \gamma = \frac{V_{AC}}{V_{DC}} = 0.48$$

$$\text{Rectification efficiency } \eta = \frac{P_{DC}}{P_{rms}} \times 100 = 81.2\,\%$$

Frequency of output signal = 2 × Frequency of input signal. Fig. 19.10 (c) or the characteristics mentioned suggest we shall prefer a full wave rectifier.

Bridge Rectifier is preferred as the diodes used shall have peak inverse voltage (PIV) half that of the value needed in full wave rectifier, made using centre tapped transformer.

Negative Resistance See Fig. 19.11. In the region AB.

$I \propto \frac{1}{V}$. This region is termed as negative resistance region. The devices which show negative resistance are

(a) tunnel diode.

(b) tetrode (vacuum tube).

(c) thyristors.

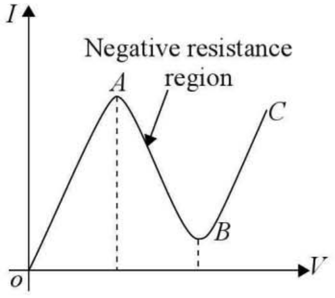


Fig. 19.11 Negative resistance illustration

Photo diodes are operated in **reverse bias.** If frequency of incident radiation is such that $hf \geq E_g$ then conductivity will increase as electrons from valence band jump to conduction band creating conduction electrons (in CB) and holes (in V.B.).

Thus, if $hf \geq E_g$ or $\frac{hc}{\lambda} \geq E_g$ or $\lambda \leq \frac{hc}{E_g}$ conductivity will increase.

LED (Light emitting diode) If the diode is forward biased and band gap E_g is such that $\lambda = \frac{hc}{E_g}$ lies in visible region for a transition of electron from conduction band to valence band then light will be emitted. The band gap E_g of *Ge* or *Si* does not warrant visible light emission. Therefore, GaAs, GaAlAs. GaInP, GaAlP, InP etc. are used to make LEDs which emit light in visible region. By varying % contents band gap E_g in such compounds can be varied.

Drawback of diode Note from Table 19.1 pn junction or diode cannot be used as an amplifier.

Transistor is made of words TRANSfer + resISTOR (TRANS from transfer and ISTOR from resistor). Thus, transistor is a device which gives transfer of resistor without changing the current at input or output, i.e., same current flows through input and output while resistance at the two places are different. This device is designed to make amplifier. Obviously if $R_{out} > R_{input}$ then $P = I^2 R$ gives us clue that output power is more than input power. This is the principle of amplifier.

Transistor is basically of three types (a) UJT (uni junction transistor), (b) BJT (bipolar junction transistor), (c) FET (Field effect transistor). BJT is of two types *npn* and *pnp*. FET is of three types JFET (Junction field effect transistor), MOSFET (Metal oxide semiconductor field effect transistor), IGFET (Insulated gate field effect transistor).

In a BJT, emitter is heavily doped, base should be extremely thin. Fig. 19.12 (a) shows *pnp*-transistor and its circuit symbol, and Fig. 19.12 (b) shows *npn*-transistor and its circuit symbol.

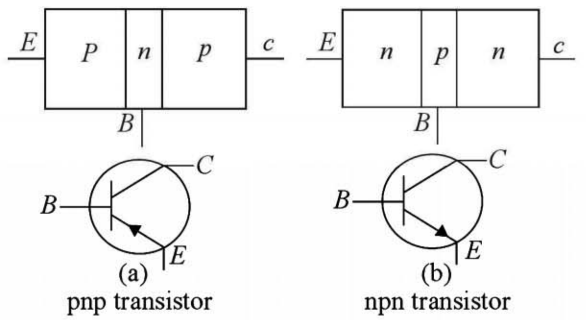


Fig. 19.12 Bipolar junction transistor

A transistor can be considered as a junction. Then,

$$I_E = I_B + I_C$$

$$I_C = \beta I_B + (\beta + 1)\, I_{CBO}$$

$I_C = \alpha I_E + I_{CBO}$. I_{CBO} is collector base Junction current when emitter is open.

The term I_{CBO} is temperature dependent. I_{CBO} doubles for every 8-10°C rise in temperature.

α is current gain for common base amplifier and $\alpha < 1$. β is current gain for common emitter amplifier and $\beta > 1$. Each transistor circuit requires temperature compensation. Therefore, self bias arrangement is used which automatically, adjusts/bias to compensate the effect of temperature.

$$\beta = \frac{I_C}{I_B} (> 1) ; \qquad \alpha = \frac{I_C}{I_E} (< 1);$$

$$\beta = \frac{\alpha}{1-\alpha}; \qquad \alpha = \frac{\beta}{1+\beta}.$$

A transistor can operate in three regions. In saturation region, transistor acts like an ON switch (dynamic resistance is 8Ω). In cut off region, transistor behaves as an OFF switch (resistance $\geq 10^4$ Ω). In active region transistor acts as an amplifier. See Fig. 19.13 to understand these regions. Note that in active region characteristics are equidistant and parallel for equal change in input, i.e., output is directly proportional to input. Hence, active region is also called linear region.

Cut off region is achieved when both collector base junction and emitter base junction are reverse biased. Saturation region is achieved when both collector base (CB) junction and emitter base (EB) junction are forward biased.

In active region emitter base junction is forward biased and collector base junction is reverse biased. Cut off and saturation regions are used in logic gates.

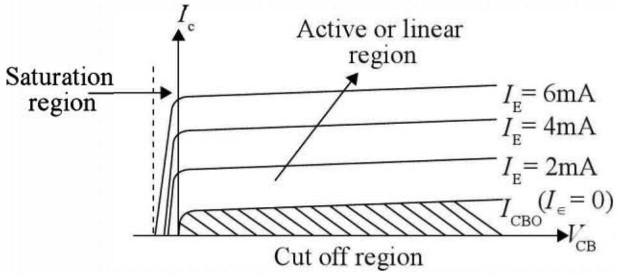


Fig 19.13 Output characteristics of common base

Transconductance or transfer conductance or mutual conductance $g_m = \frac{\partial I_C}{\partial V_{BE}}$.

Amplifier is a circuit which gives power gain. Table 19.2 shows characteristic of common base (CB) Amplifier, common emitter (CE) and common collector (CC) Amplifiers.

One can note from Table 19.2 that

(i) **CB Amplifier** is a **voltage amplifier** as it amplifies only voltage.

(ii) **CC Amplifier** is a **current amplifier** as it amplifes only current.

(iii) **CE Amplifier** amplifies both current and voltage. It gives a **phase shift of 180°** between input and output signal. This is the reason, it is used to make a NOT gate or inverter. Do not get the notion that CE amplifier is the best as it gives A_i and A_v both > 1.

Common collector amplifier is also known as a **buffer amplifier** or an **emitter follower.**

In another classification amplifiers may be of four types: class A, class B, class AB and class C.

Class A amplifier It amplifies complete signal (0–360°) using a single transistor. It is used when the signal is

Table 19.2 Characteristics of Amplifiers

Property	***Common base Amplifier***	***Common emitter Amplifier***	***Common collector Amplifier***
Input impedance (Z_i)	Low	medium high	medium high
Output impedance (Z_o)	high	high	low
Current gain (A_i)	$A_i = \alpha < 1$	$A_i = \beta > 1$	$A_i = (\beta + 1) > 1$
Voltage gain (A_v)	$A_v = A_i \frac{R_L}{r_e} > 1$	$A_v = A_i \frac{R_L}{r_b} > 1$	$A_v = A_i \frac{R_L}{r_b} < 1.$
	$= \alpha \frac{R_L}{r_e} > 1$	$= \beta \frac{R_L}{r_b} > 1$	$= (\beta + 1) \frac{R_L}{r_b} < 1$
Power gain ($A_p = A_v \cdot A_i$)	$A_p = \alpha^2 \frac{R_L}{r_e} > 1$	$A_p = \beta^2 \frac{R_L}{r_b} > 1$	$A_p = (\beta + 1)^2 \frac{R_L}{r_b} > 1.$
Phase shift between input and output signal	nil	180° or π-rad	nil

Key words → Low ~ 25-30 Ω, medium high ~ 200 Ω, high ≥ 10^4 Ω r_e = dynamic resistance of emitter, r_b = dynamic resistance of base.

small, i.e., at the input or first stage or preamplifier stage. The transistor is biased in the active region in the midway as illustrated in Fig. 19.14. Q-point or operating point shows the bias point.

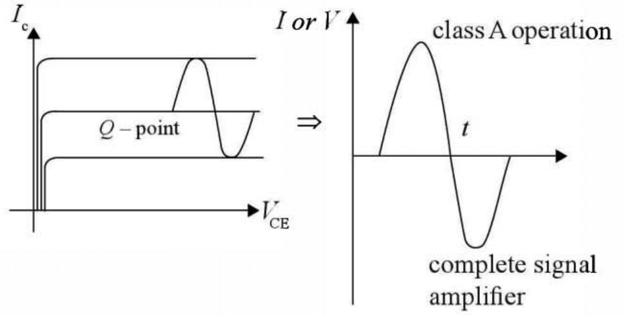


Fig. 19.14 Class A amplifier

Class B amplifier As shown in Fig. 19.15 Q-point in class B amplifiers is in cut off region. Therefore, they amplify only half the signal 0–180° or 180–360°.

Therefore, two transistors are required to amplify complete signal. At the output stage of amplifier system signal becomes large and is amplified using class B push-pull amplifier (two transistors one amplifier 0-180° and the other 180°–360°).

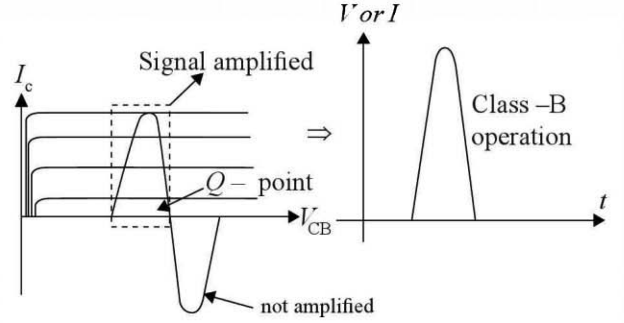


Fig. 19.15 Class B amplifier

Class AB Amplifier It amplifies > 180° but less than 360° using a single transistor as illustrated in Fig. 19.16(a). Q-point is slightly above cut off region. So a part of the back half signal is also amplified.

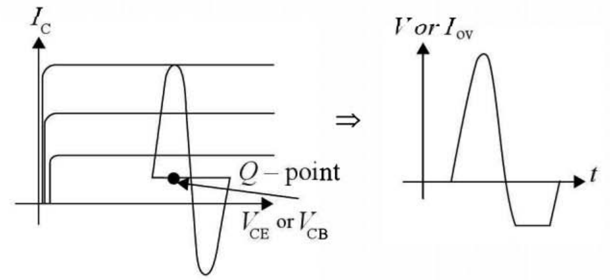


Fig. 19.16(a) Class AB amplifier

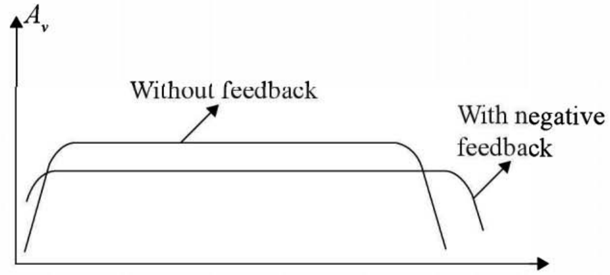


Fig. 19.16(b)

Class C amplifier They amplify only pulses when the signal is large. Class C amplifiers are used in transmitters. The figure shows amplifier frequency response curve. Note band-width increases with negative feedback.

Oscillator LC tank circuit is a basic oscillator. Due to dissipative element (internal resistance of the coil), the oscillations are damped. Hence, positive feedback or negative resistance is required to achieve sustained oscillations.

Barkhausen criterion should be satisfied to achieve sustained oscillation

$\beta A_v \geq 1$ where β is feedback factor and A_v is voltage gain. The criterion lists two points:

(a) there should be positive feedback.

(b) feedback factor $\beta \geq \frac{1}{A_V}$.

Therefore, a frequency selective feedback network is employed so that at a particular frequency called the frequency of oscillation $\beta A_v \geq 1$. This frequency is frequency of oscillation. Oscillators may be of two types (a) Audio-frequency oscillators (AFO) (b) Radio frequency oscillator (RFO).

To design an AF oscillicator, one requires an RC circuit. RC phase shift oscillator and Wein's bridge oscillator are popular AF oscillators. Now-a-days, normally operational amplifier (op-amp) is used to design amplifiers and oscillators. AF oscillators have frequency $\leq$ 20 kHz.

Radio frequency oscillators are LC oscillators. Hartley, Colpitt's, Clapp's, Crystal oscillators are popular RF oscillators. RF oscillators operate at high frequency > 100 kHz. They are used to generate carrier wave and as a local oscillator in a radio receiver.

In another categorization, oscillators may be of two types a) sinusoidal or sine/cosine wave generator b) relaxation oscillators. Relaxation oscillators generate any wave other than sine or cosine, that is, square, rectangular, triangular, sawtooth etc.

Logic gates Logic is of two types (a) positive logic (b) negative logic.

In positive logic high state +5V is assigned a '1' and low state (0V) a value '0' as illustrate in Fig. 19.17. In **negative logic** high state is assigned a '0' while a low state is assigned a '1'.

AND gate A positive logic AND gate assumes high state if and only if all the inputs are high. Circuit symbol of two input AND gate is shown in Fig. 19.17 (a) and circuit implementation using switching diodes in Fig. 19.17 (b). Operation symbol is '.' as it behaves like multiplication.

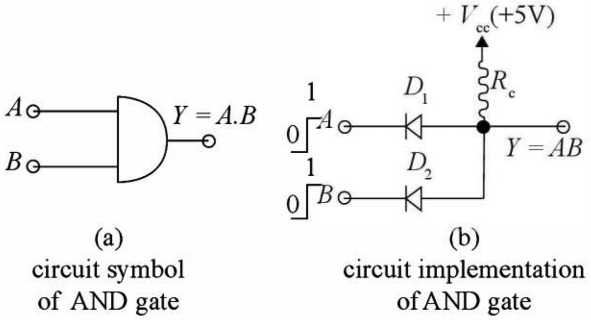


Fig. 19.17

Table 19.3 Truth Table of AND gate

A	B	$Y = A . B$
0	0	0
0	1	0
1	0	0
1	1	1

OR gate A positive logic OR gate assumes a high state if any of the input is high. Fig. 19.18 (a) shows circuit symbol and Fig. 19.18 (b) shows the circuit implementation of OR using switching diodes. Operation symbols of OR is '+'.

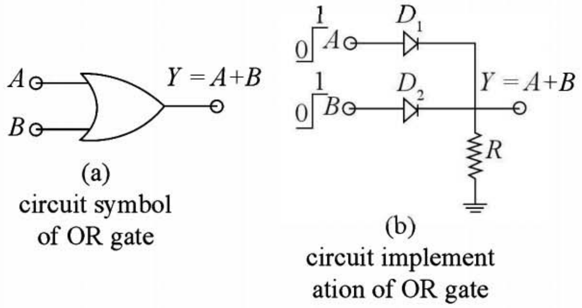


Fig. 19.18

Table 19.4 Truth Table of OR gate

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate or Inverter A NOT gate inverts the input, i.e., *a* '0' input appears as *a* '1' or vice versa Fig. 19.19 (a) shows circuit symbol and Fig. 19.19 (b) circuit implementation using a switching transistor. Operator symbol a bar or a complement.

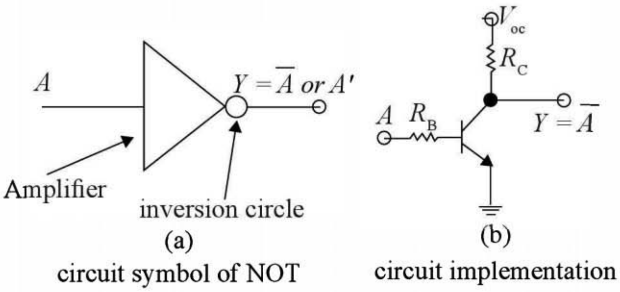


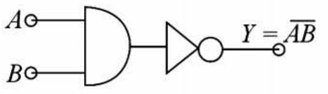
Fig. 19.19

Table 19.5 Truth Table of NOT gate

A	$Y = \bar{A}$
0	1
1	0

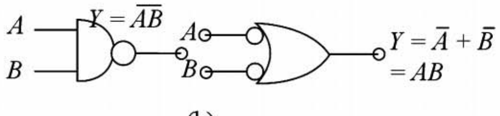
Note that NOT gate is a unary gate. All other gates are binary gates.

NAND (Negated AND) Output of AND is negated or inverted. Fig. 19.20 shows NAND gate implementation and its circuit symbols.



(a)

NAND = AND + NOT or NOT of AND



(b)

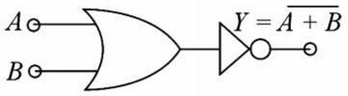
circuit symbol of NAND

Fig. 19.20

Table 19.6 Truth table of NAND

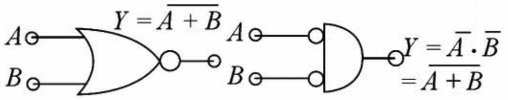
A	**B**	**Y =**
0	0	1
0	1	1
1	0	1
1	1	0

NOR (Negated OR) Output of OR gate is negated or inverted. Fig. 19.21 shows NOR gate implementation and its circuit symbols.



(a)

NOR = OR + NOT or NOT of OR



(b)

circuit symbol of NOR

Fig. 19.21

Table 19.7 Truth Table of NOR

A	**B**	**Y =** $\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Universal gate A gate which possesses following properties is called a universal gate

(a) Any gate/logic can be developed using a single gate or combination of similar gates.

(b) They follow associative or commutative laws.

(c) They can be manufactured economically.

NAND and NOR qualify these properties and hence, are termed as universal gates.

De-Morgan Laws

(i) $\overline{A+B} = \overline{A}\,\overline{B}$ (ii) $= \overline{AB} + \overline{A}+\overline{B}$.

Duality principle When positive logic is changed to negative logic or vice versa AND changes to OR; OR changes to AND; NAND changes to NOR and NOR changes to NAND. Note a change of 0 with 1, and, 1 with 0 in a truth table will reveal this result.

Phantom OR or wired OR Fig 19.22 shows Phantom OR or wired OR.

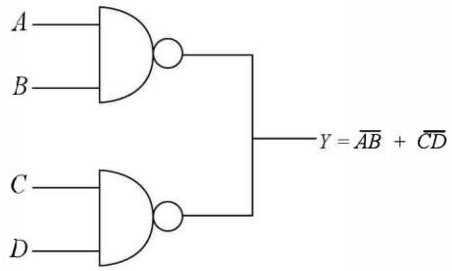
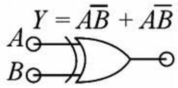
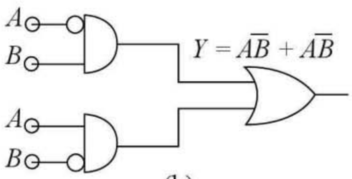


Fig. 19.22 Wired OR

XOR (Exclusive OR) Fig. 19.23 shows XOR gate. The output of XOR acts as sum bit of half Adder.





(a) circuit symbol of XOR (b) implemeutation of XOR

Fig. 19.23

Conversion of gates Fig. 19.24 shows NOT from NAND. Fig. 19.25 shows NOT from NOR.

NOT from NAND

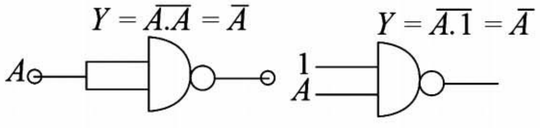


Fig. 19.24

NOT from NOR

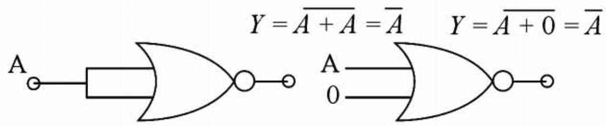


Fig. 19.25 Short both the inputs of NAND to get NOT

AND from NAND

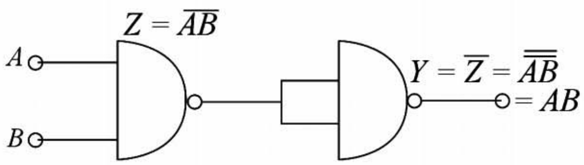


Fig. 19.26

AND from NOR

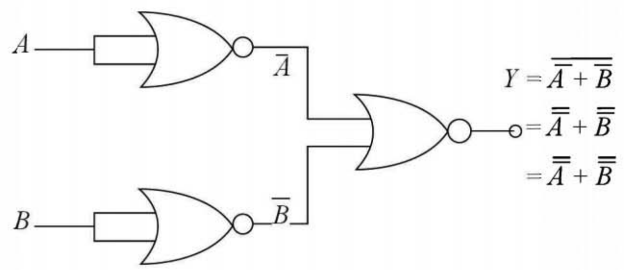


Fig. 19.27

OR from NAND

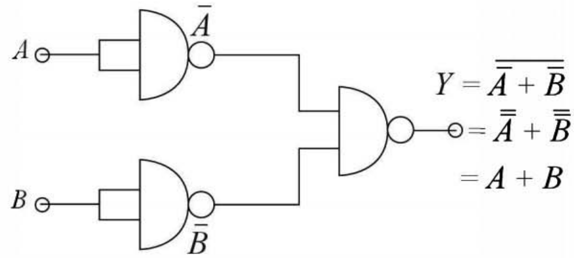


Fig. 19.28

OR from NOR

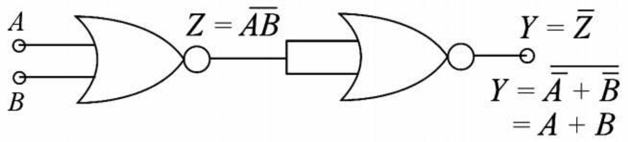


Fig. 19.29

Half Adder It is used to add two bits Augend and Addend. Sum bit S can be implemented using XOR and carry bit can be implemented using AND. Fig. 19.30 (a) shows circuit symbol of Half Adder and Fig. 19.30 (b) shows its gate implementation.

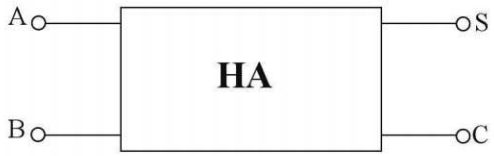


Fig. 19.30 (a) Half Adder

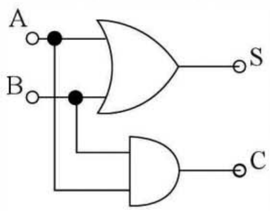


Fig. 19.30 (b) Gate implementation of half adder

Table 19.8 Truth Table of half adder

Augend ***A***	***Addend*** ***B***	***Sum*** ***S***	***Carry*** ***C***
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder It is used to add 3 bits—Augend (A_n), Addend (B_n) and carry from previous state (C_{n-1}). Sum (S_n) and carry to next state (C_n) are outputs. Fig. 19.31 (a) shows circuit symbol and Fig. 19.30 (b) shows gate implementation of Full Adder.

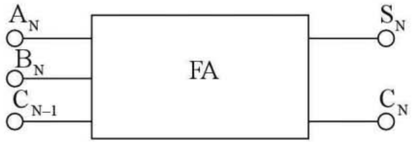


Fig. 19.31 (a)

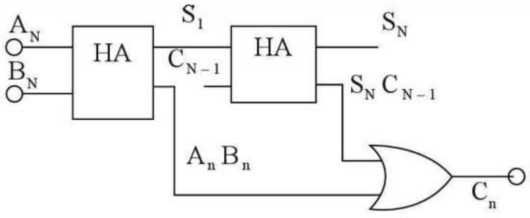


Fig. 19.31 (b)

Table 19.9 Truth Table of full adder

Augend A_n	***Addend*** B_n	***Carry from previous state*** C_{n-1}	***Sum*** S_n	***Carry*** C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

From the table

$$S_n = \overline{A_n}\ \overline{B_n}\ C_{n-1} + \overline{A}_n\ B_n\ \overline{C}_{n-1} + A_n\ B_n + \overline{C}_{n-1}$$
$$+ A_n B_n C_{n-1}$$
$$= \left(\overline{A}_n \overline{B}_n + A_n B_n\right) C_{n-1} + \left(\overline{A}_n B_n + A_n \overline{B}_n\right) C_{n-1}$$
$$= A_n \oplus B_n \oplus C_{n-1}$$
$$C_n = \overline{A}_n B_n C_{n-1} + A_n \overline{B}_n C_{n-1} + A_n B_n \overline{C}_{n-1} + A_n B_n C_n$$
$$= S_1 C_{n-1} + A_n B_n$$

Integrated Circuit (IC) If all the circuit elements like transistor, diode, capacitor resistor are built on a single chip and inter connected to form a complete circuit, then such a circuit is called an integrated circuit or an IC. ICs are in general of two types

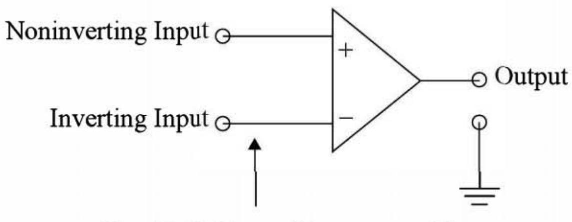


Fig. 19.32 Linear IC or op-amplifier

(a) Analog or linear or op-amplifier

and (b) digital or binary or logic families.

Analog ICs contain operational amplifiers (op-amp) These are direct coupled differential amplifiers. Fig. 19.32 shows circuit symbol of op-amp. Note, it has an inverting input terminal (–) and a non inverting input terminal (+). The difference between inverting and non inverting inputs is amplified. Gain of such amplifiers is very high ($10^5 - 10^8$). Therefore, an external feedback system is used to curtail gain. This amplifier can be used for any mathematical operation like addition, subtraction, multiplication, log, antilog, differentiation and integration.

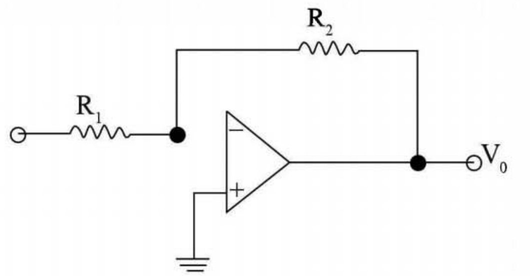


Fig. 19.33 Inverting amplifier or scale changer

In Fig. 19.34 configuration

$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$. The Ratio $\frac{R_2}{R_1}$ decides the voltage gain under feedback condition.

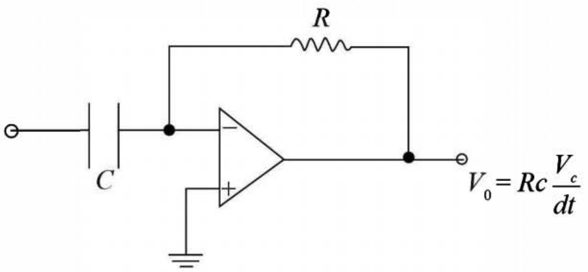


Fig. 19.34 (a) Differentiation circuit

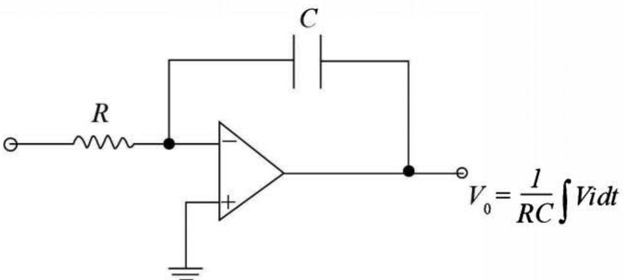


Fig. 19.34 (b) Integrating circuit

Fig. 19.34 (a) and Fig. 19.34 (b) show differentiation and integration implementation using op-amp.

Now-a-days, CMOS technology, biCMOS, GaAs and opto electronic ICs are being made. biCMOS, GaAs and opto-electronics ICs are very high speed devices.

Short Cuts and Points to Note

1. Energy bands are formed due to degenerated energy levels in a crystal structure or bulk of the material.
2. The property of the semiconductor that resistivity falls with rise in temperature can be explained using band theory.
3. A semiconductor is a perfect insulator at 0 *K*.
4. In a semiconductor, conduction is due to drift as well as diffusion currents.
5. The mobility of electrons is 2–3 times higher than that of holes. Therefore, *npn* devices or n-channel MOSFET are faster than *pnp* devices or p-channel MOSFET.
6. In intrinsic or pure semiconductors $n_i = h_i$.
7. In extrinsic semiconductor, if n_e is the electron density and h_e is the hole density the material will be *n*-type if $n_e > n_i$ or $n_e > h_e$. The material will be p-type if $h_e > n_e$ or $h_e > n_i$. Moreover, in thermal equilibrium $n_e h_e = n_i^2$.
8. In metals, valence band and conduction band overlap therefore, $E_g = 0$. In semiconductors $E_g \sim 1$ eV and insulators have $E_g \sim 6$ eV.
9. In *n*-type semiconductor, conductivity

   $\sigma_n = ne\,\mu_n \cong N_D\, e\,\mu_n$.

   In *p*-type semiconductor conductivity

   $\sigma_p = he\,\mu_h \cong N_A\, e\,\mu_h$.

   In intr]insic semiconductor conductivity

   $\sigma_{\text{intrinsic}} = n_i\, e\,\mu_n + h_i\, e\,\mu_n$.
10. A *pn* junction or a diode may be assumed ideal diode. It may be assumed to act like an ON switch when forward biased and like an OFF switch when reverse biased. That is, diode shows full conduction ($r = 0$) when forward biased and no conduction ($r = \infty$) when reverse biased.
11. On forward biasing the diode resistance $r \to 0$, depletion layer width decreases. Current is mostly diffusion. (Actual current is diffusion current + drift current).

    On Reverse biasing the diode $r \to \infty$, depletion layer width increases. Current is drift current only.
12. In photo diodes conduction will increase (They are operated reverse biased) if wavelength of incident radiation $\lambda \leq \frac{hc}{E_g}$.
13. In an LED light will be emitted f a wavelength $\lambda = \frac{hc}{E_g}$. Since, *Ge* and *Si* will emit IR they can be used

in remote sensing, Robots etc. LEDs emitting light in visible region are made from Ga As, Ga In P, Ga In As, Ga Al As etc, i.e., it is an alloy of 13_{th} and 15_{th} group element forming a semiconductor where E_g depends on concentration of their constituents.

14. 60 Carbon atoms forming a football like structure behave as a semiconductor.

15. Diode cannot be used as an amplifier since it is a two terminal device.

16. Transistor amplifies by converting power of dc source into AC (of the signal applied). It uses the principle $P = I^2R$. If $R_{in} << R_{out}$ and current at input and output remains unchanged then power gain is obtained.

17. $$\left.\begin{array}{l}\text{Current gain } A_i = \alpha < 1 \\ \text{Voltage gain } A_v = \alpha \dfrac{R_L}{r_e} > 1 \\ \text{Power gain } A_p = \alpha^2 \dfrac{R_L}{r_e} > 1 \\ \text{No phase shift between} \\ \text{input and output.}\end{array}\right\} \begin{array}{l}\text{In common base (CB)} \\ \text{amplifier} \\ \alpha = h_{FB}\end{array}$$

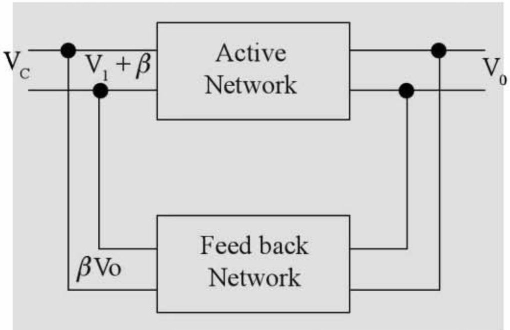
18. $$\left.\begin{array}{l}\text{Current gain } A_i = \beta < 1 \\ \text{Voltage gain } A_v = \beta \dfrac{R_L}{r_b} > 1 \\ \text{Power gain } A_p = \beta^2 \dfrac{R_L}{r_b} > 1 \\ \text{Phase shift} = 180° \text{ or } \pi \text{ rad.}\end{array}\right\} \begin{array}{l}\text{In common} \\ \text{emitter (CE)} \\ \text{amplifier} \\ \beta = h_{FE}\end{array}$$

19. $$\left.\begin{array}{l}\text{Current gain } A_i = \beta + 1; \text{Power} \\ \text{gain } A_p = (\beta+1)^2 \dfrac{R_\ell}{r_b} > 1 \\ \text{Voltage gain } A_v = (\beta+1)\dfrac{R_\ell}{r_b} < 1; \\ \text{Phase shift nil}\end{array}\right\} \begin{array}{l}\text{In common} \\ \text{collecter (CC)} \\ \text{amplifier}\end{array}$$

Common collector amplifier is also called Power amplifier, Buffer amplifier, Current booster or Emitter follower.

20. $I_E = I_C + I_B$; $\alpha = \dfrac{I_C}{I_E}$; $\beta = \dfrac{I_C}{I_B}$, $\beta = \dfrac{\alpha}{1-\alpha}$ and $\alpha = \dfrac{\beta}{1+\beta}$.

21. Oscillator can be designed with any of the two techniques. Either use negative resistance device or positive feedback. When in the frequency selective network, Barkhausen criterion is satisfied then oscillations are generated. ($\beta A_v \geq 1$). The Figure shows block diagram of an oscillator. *LC* oscillators are high frequency of *RF* oscillators while *RC* oscillators are low frequency or Audio frequency oscillators.



22. Use the relations in order to simplify logical expressions.
   (i) $A + A = A$ its dual $A \cdot A = A$
   (ii) $A + \overline{A} = 1$ its dual $A \cdot \overline{A} = 0$
   (iii) $A + 1 = A$ its dual $A \cdot 1 = A$
   (iv) $A + AB = A$ its dual $A(A + B) = A$
   (v) $A + \overline{A}B = A + B$ its dual $A(\overline{A} + B) = AB$
   (vi) $\overline{A+B} = \overline{A}.\overline{B}$; $\overline{A.B} = \overline{A} + \overline{B}$.
   (vii) $\overline{\overline{A}} = A$; $1 + 1 = 1 + 0 = 1$
   $1.0 = 0$; $1.1 = 1$

23. NAND and NOR gates are universal gates. NOT gate is unipolar. All other gates are bipolar.

24. Devices like tunnel diode, thyristor, tetrode have negative resistance.

25. Transistors may operate in 3 regions. (a) Cut off region is obtained if both emitter base junction and collector base junction are reverse biased. It acts like an OFF switch. (b) Active or linear region is achieved when EB junction is forward biased (V_{EB} > 0.6 V) and collector base (CB) junction is reverse biased. Amplifiers can be made only in this region. (c) Saturation region is achieved when both EB and CB junction are forward biased. In this region transistor acts like an ON switch.

26. Logic circuit are of two types combinational and sequential. Sequential circuits possess memory. In combinational circuit output depends only on the present inputs. In sequential circuits output depends not only on present input but on past inputs in chronological order.

27. Integrated circuits are of two types. a) Analog b) digital or logic family. Analog ICs has op-amps

used in amplifiers, oscillators, D/A converter, timer circuits, power supplies–regulated and SMPS, function enerator filters, modulation and demodulation, phase locked loops etc.

Digital ICs contain simple logic gates, Adders, multiplexers, CPU, ASIC (Application specific integrated circuits). RAMs, ROMs, combinational locks, registers, counters, decoders, code converters etc. Digital circuits in general can be divided into SSI, MSI, LSI, VLSI and ULSI.

28. Op-amps are high gain dc coupled differential amplifiers and can be used even in mathematical operation like addition, difference, multiplication, log, antilog, differentiation, integration, scale changer etc.

29. If n amplifiers are connected in tandem having individual gains $A_1, A_2, ... A_n$. Then, the overall gain is $A_{net} = A_1 A_2 ... A_n$.

30. High speed ICs are made with GaAs, BICMOS. Optical fibers are even added to increase the speed.

Caution

1. Forgetting the valve action of pn junction diode.

⇒ In pn junction current flow from p to n side p▷|n, i.e.; arrow mark side.

2. Assuming that output of rectifier is dc, hence, its frequency is zero.

⇒ Frequency of output of half wave rectifier is same as that of input signal and frequency of output of full wave rectifier is twice that of input signal.

3. Assuming that rectification efficiency of a half wave rectifier is 50% and that of a full wave rectifier is 100% as in half wave rectifier half of the signal and in full wave rectifier complete signal is obtained.

⇒ Rectification efficiency of half wave rectifier is 40.6% and that of a full wave rectifier is 81.2%.

4. Assuming amplification means increasing the amplitude of current or of voltage.

⇒ Amplitude should be increased along with increase in power.

5. Not able to recall current gain in CE amplifier and CB amplifiers.

⇒ In CB amplifier current gain $A_i < 1$. $A_i = \alpha = h_{FB} = \dfrac{I_C}{I_E}$.

In CE amplifier current gain $A_i > 1$. $A_i = \beta = h_{FE} = \dfrac{I_C}{I_B}$.

6. Considering transistor cannot be used as Rectifier.

⇒ If only collector base or emitter base junction is considered then rectifier can be designed.

7. Assuming that Kirchhoff's laws cannot be applied in electronic circuits.

⇒ Kirchhoff's laws can be applied in circuits containing transistors or pn junction. A transistor can be considered a junction, therefore, $I_E = I_C + I_B$.

8. Not remembering the formulae for voltage gain and power gain.

⇒ Voltage gain $A_v = \alpha \dfrac{R_L}{r_e} > 1$ in CB amplifier.

Power gain $A_p = A_v \cdot A_i - \alpha^2 \dfrac{R_L}{r_e} > 1$ in CB amplifier.

Voltage gain $A_v = \beta \dfrac{R_L}{r_b} > 1$ in CE amplifier.

Power gain $A_p = A_v \cdot A_i = \beta^2 \dfrac{R_L}{r_b}$ in CE amplifier.

Note A_i, A_v or A_p is a ratio, therefore, they are dimensionless.

9. Assuming that the oscillator can be developed only with L and C.

⇒ Low frequency or audio frequency oscillators are made with R and C. Remember that basic requirement to make an oscillator is to fulfil the Barkhausen criterion ($\beta A_v \geq 1$).

10. Assuming in binary/logic circuits 1 + 1 = 2.

⇒ 1 + 1 is OR operation ∴ 1 + 1 = 1

and in binary number addition 1 + 1 = 10 (2 written in binary numbers).

11. Assuming in a circuit V_i = 10 mV, gain $A_v = 10^6$ then output must be 10^4 V.

⇒ Output in no case can exceed the dc biasing voltage applied.

12. Assuming amplifiers do not have internal source of distortion of signal.

⇒ Temperature dependence of minority carriers, causes thermal runaway. Moreover, the characteristics do not remain parallel and equidistant for large signal variation. Self bias system are to be used to prevent thermal runaway and large signals are amplified using Push-pull class B amplifiers.

13. Assuming mobility of hole and electron are equal.

⇒ Mobility of electron is 2-3 times larger than that of holes.