Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**06/10/2025**	**Batch No:**	**B2**
Faculty Name:		**Roll No:**	**16010124107**
Faculty Sign & Date:		**Grade/Marks:**	___/25

Experiment No: 5
Title: Flip Flops

Aim and Objective of the Experiment:

To Verify truth table of JK Flip flop using IC 7476 and study conversion of JK FF to D FF and T FF

COs to be achieved:

CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

Trainer kits

Theory:

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

JK-flip flop: has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

D Flip Flop: tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

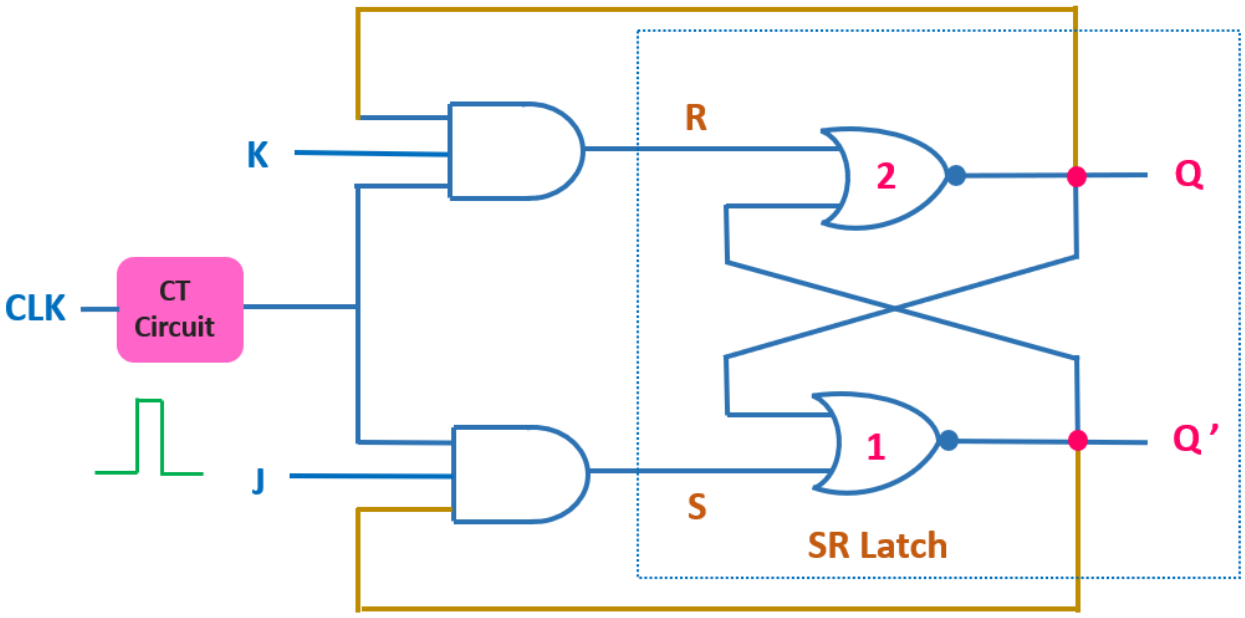
T Flip Flop: T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inp uts high.

Implementation Details:

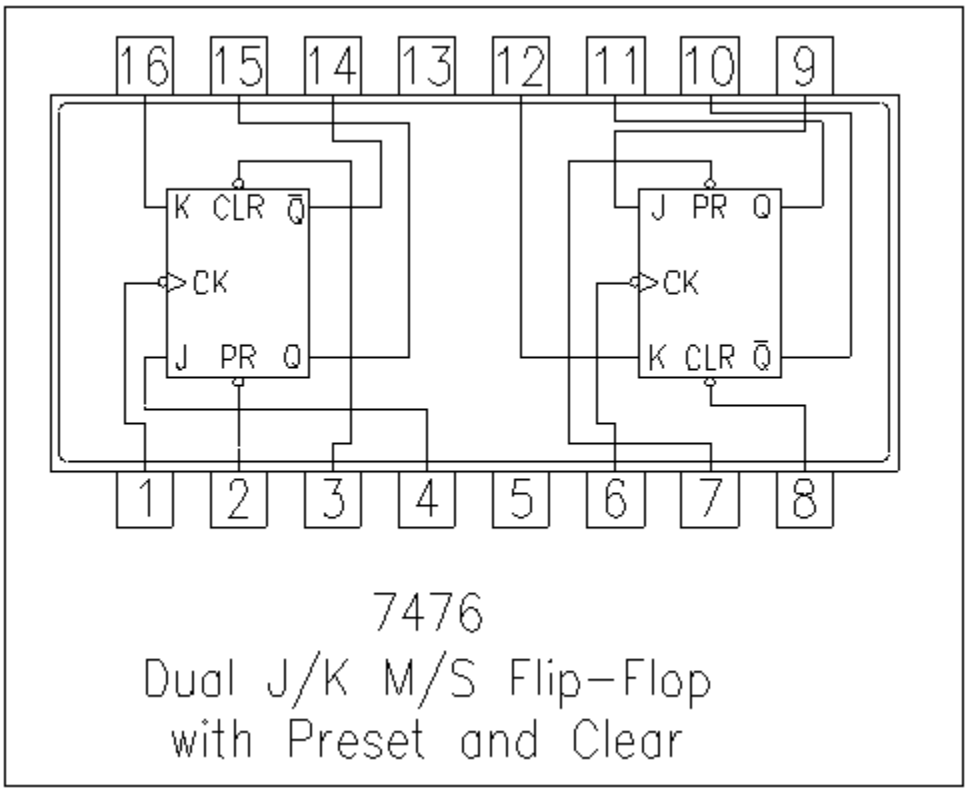
Procedure

1) Locate IC 7476 on Digital trainer kit
2) Apply various inputs to J & K pins by means of the output on logic output indicator.
3) Connect a pulsar switch to the clock input.
4) Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

Logic Symbol



Pin Diagram of IC 7476



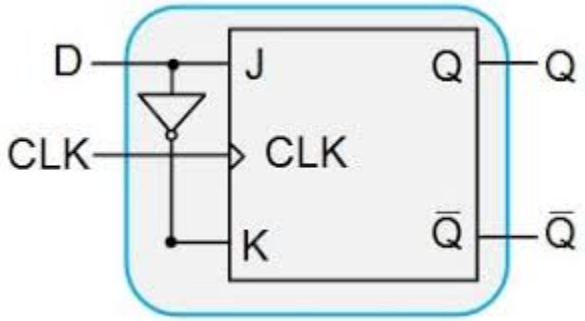
Truth Table of JK FF

Trigger	Inputs		Output				State
			Present State		Next State		
CLK	J	K	Q	Q'	Q	Q'	
	x	x	-		-		Latched
	0	0	0	1	0	1	No Change
			1	0	1	0	
	0	1	0	1	0	1	Reset
			1	0	0	1	
	1	0	0	1	1	0	Set
			1	0	1	0	
	1	1	0	1	1	0	Toggle
			1	0	0	1	

Conversion of FFs

1) JK to D FF

Conversion Diagram

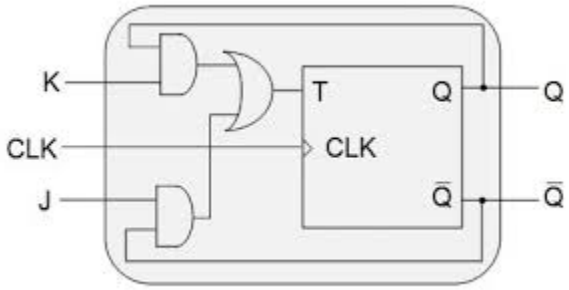


Truth Table of D FF

D	Qn	Qn+1	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

1) JK to T FF

Conversion Diagram



Truth Table of T FF

T	Qn	Qn+1	J	K
0	0	0	0	x
0	1	1	x	0
1	0	1	1	x
1	1	0	x	1

Implementation Details

Procedure:

1) Locate the IC 7476 and place the IC on trainer kit.
2) Connect VCC and ground to respective pins of IC trainer kit.
3) Implement the circuit as shown in the circuit diagram.
4) Connect the inputs to the input switches provided in the trainer kit.
5) Connect the outputs to the switches of O/P LEDs
6) Apply various combinations of inputs according to the truth table and observe the condition of LEDs.
7) Note down the corresponding output readings for various combinations of inputs.

Post Lab Subjective/Objective type Questions:

1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

Parameters	JK	SR
Input	Has two inputs J and K	Has two inputs Set and Reset
Toggling	When J and K are high, JK changes its state	When both inputs are high, the SR is in invalid state
Race condition	When J and K=1, it may develop a race condition	No race condition.
Usage	More versatile and can also perform SR flip flop functions	Less complex in design but not flexible
Complexity	More complex	Less complex

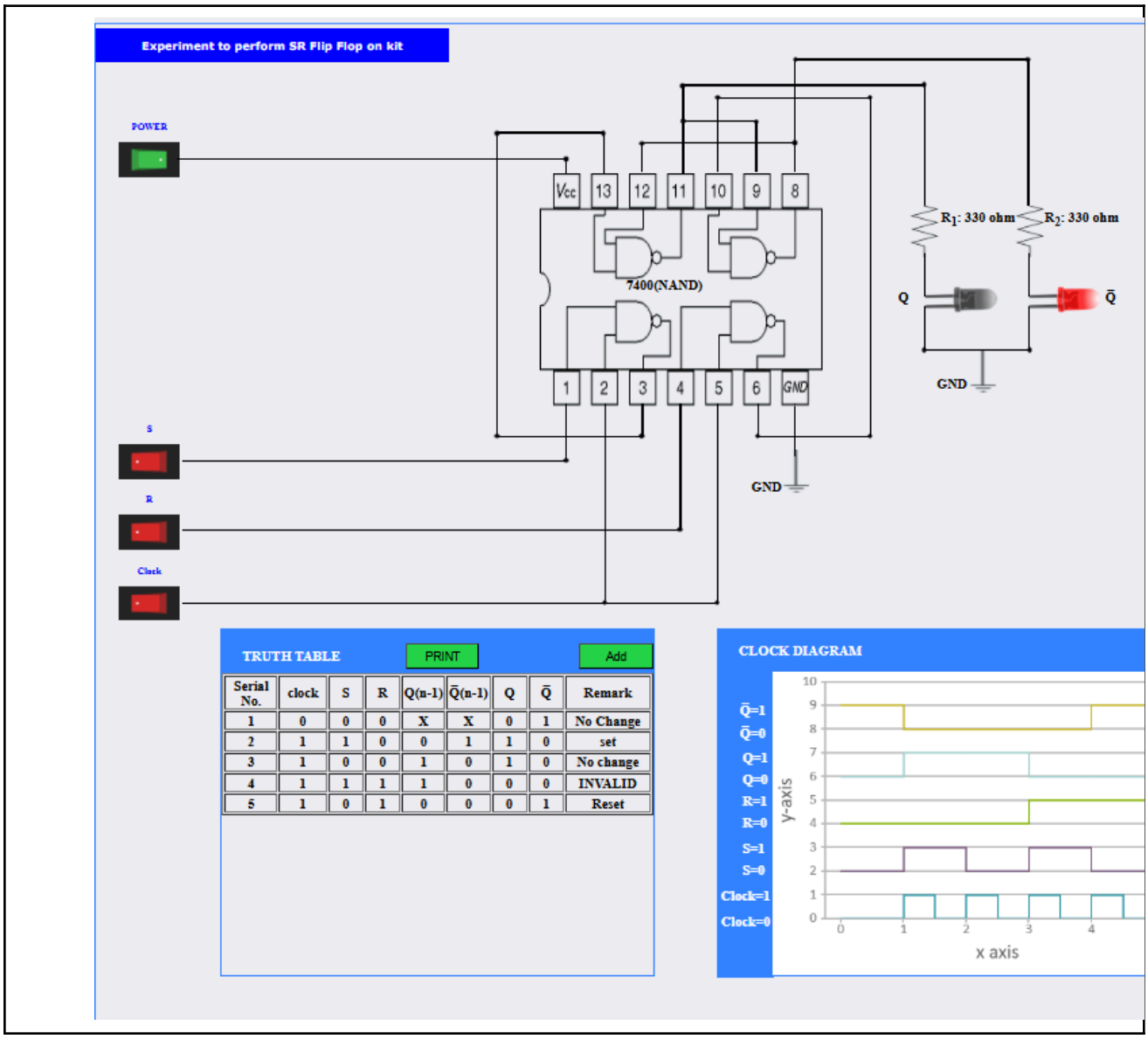
2. What is the use of characteristic and excitation table?

The characteristic table defines a flip-flop's next state based on its current state and input, used for analysis. The excitation table is used for design, showing the specific input conditions needed to transition from a current state to a desired next state.

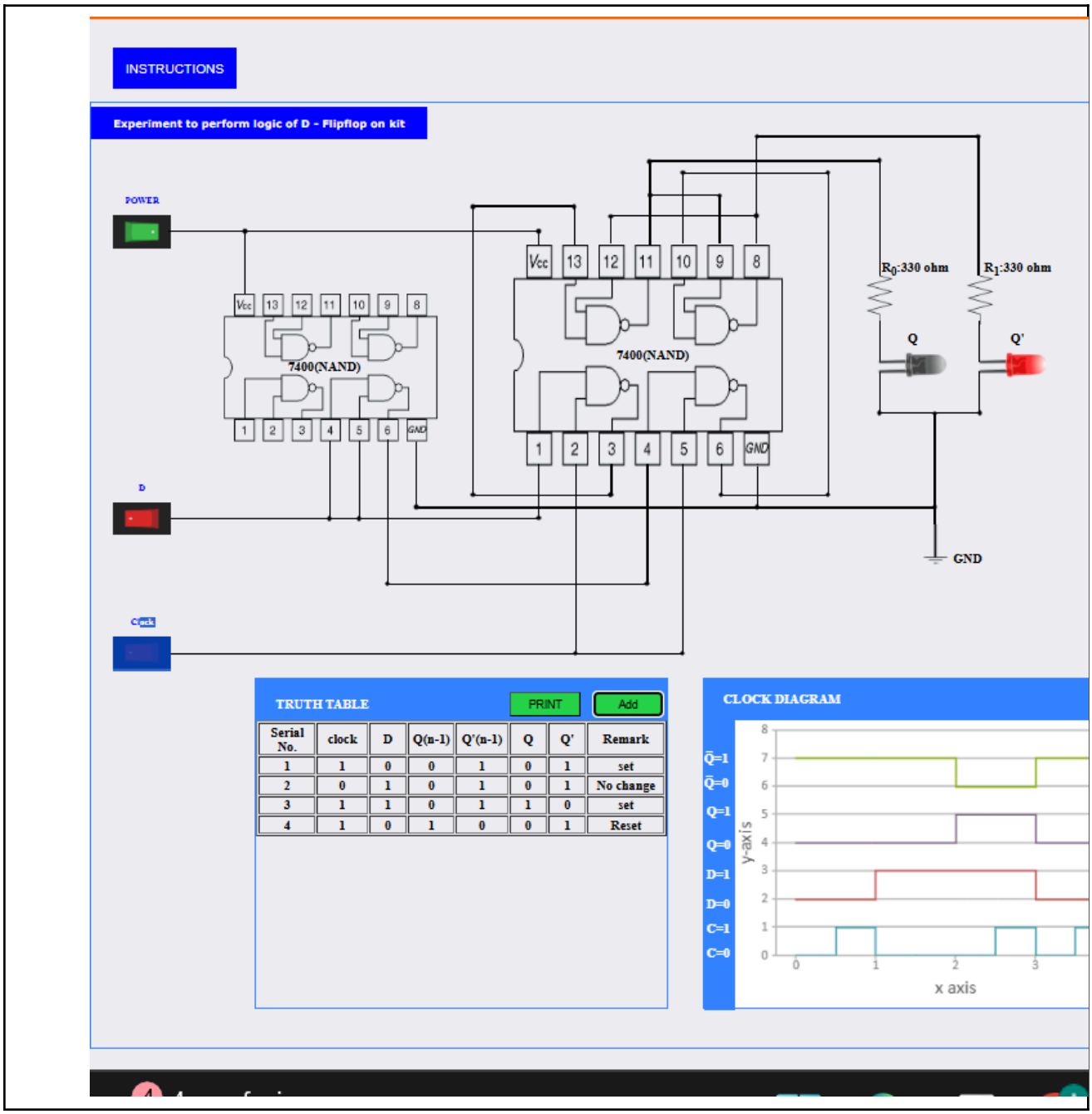
3. How many flip flops do you require storing the data 1101?

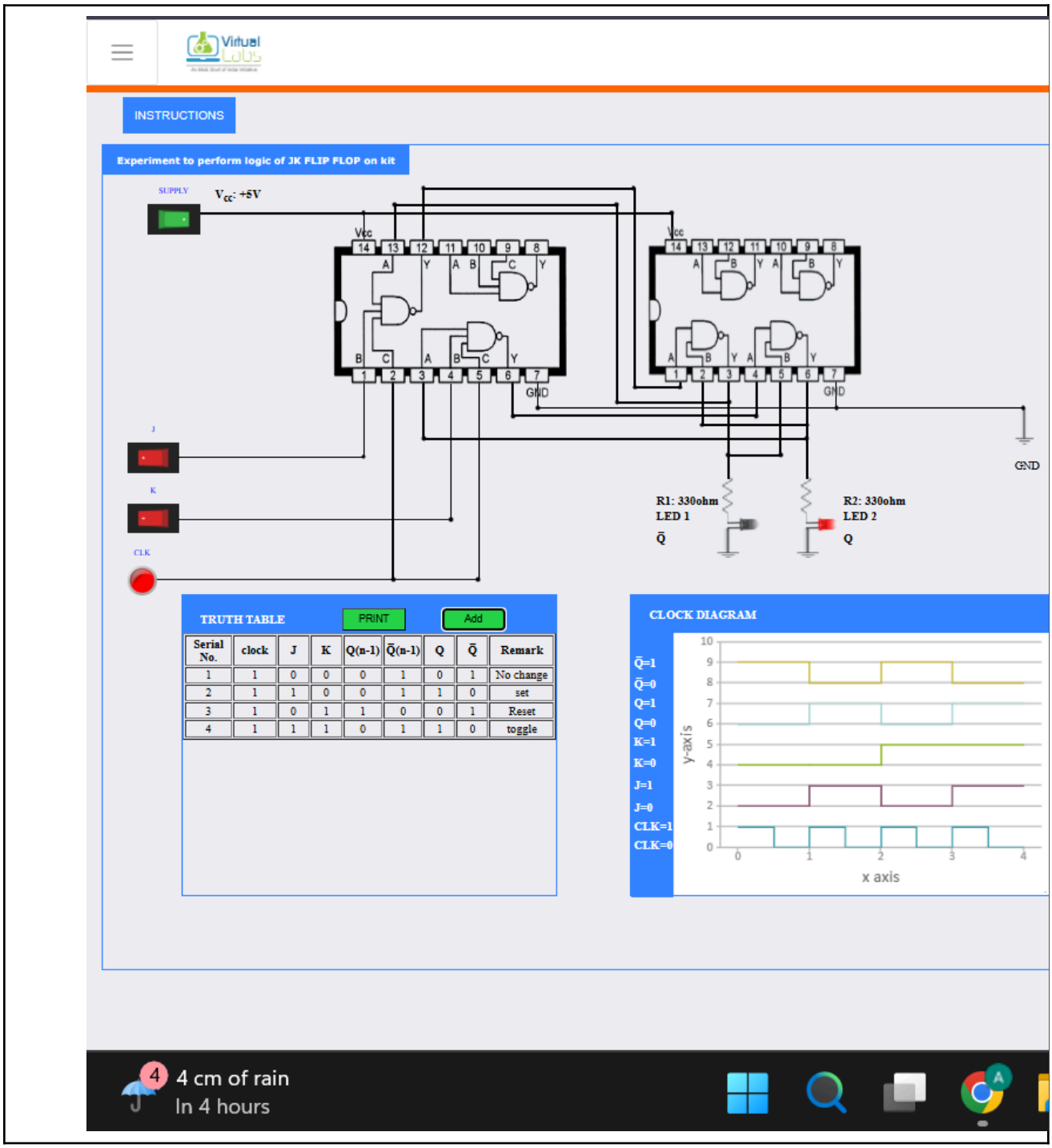
We need four flip flops since 1101 is four bits.

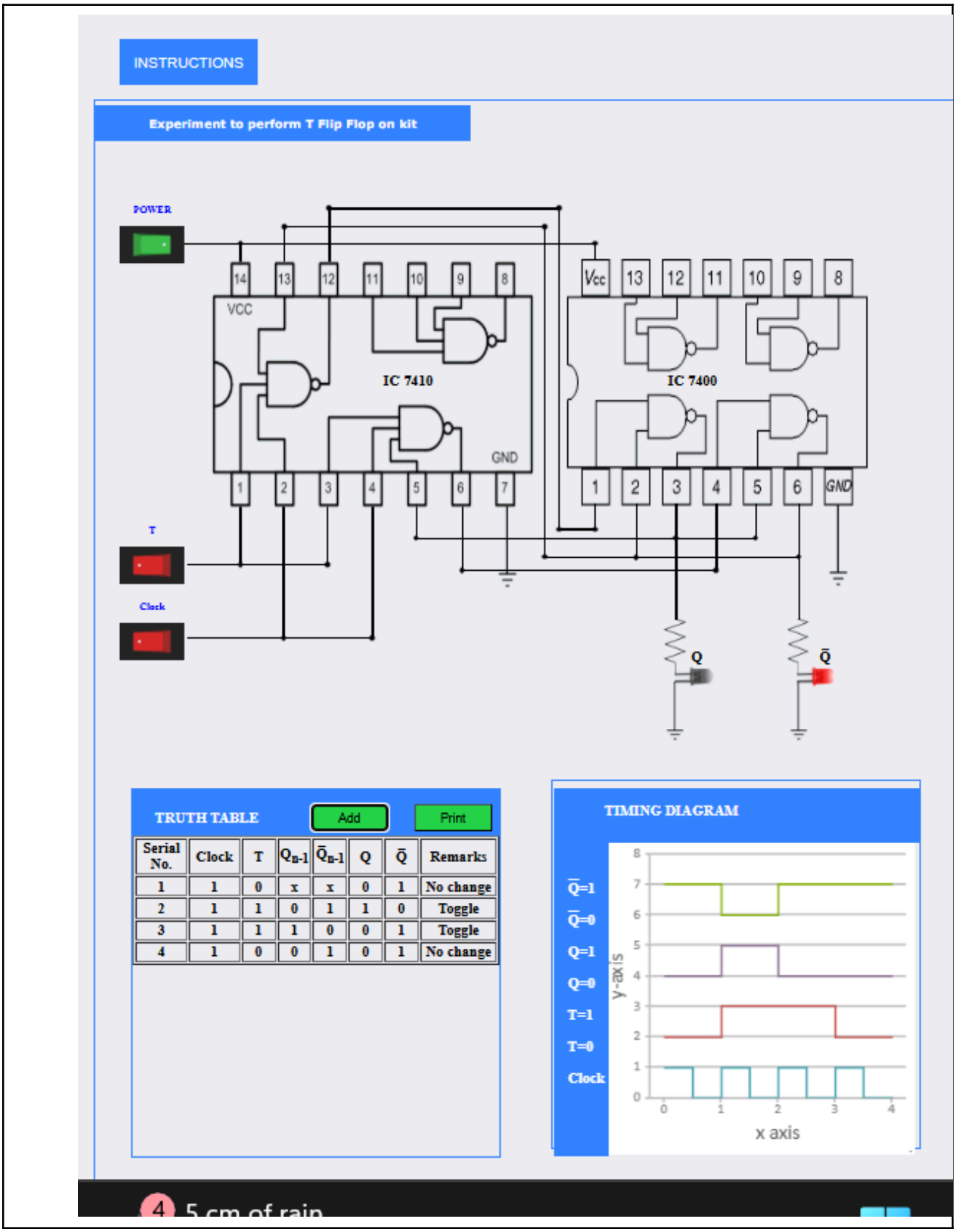
4. Virtual Lab for Flipflop. Perform Simulation give feedback.
   https://de-iitr.vlabs.ac.in/exp/truth-tables-flip-flops/simulation.html



Serial No.	clock	S	R	Q(n-1)	Q̄(n-1)	Q	Q̄	Remark
1	0	0	0	X	X	0	1	No Change
2	1	1	0	0	1	1	0	set
3	1	0	0	1	0	1	0	No change
4	1	1	1	1	0	0	0	INVALID
5	1	0	1	0	0	0	1	Reset


INSTRUCTIONS
Experiment to perform logic of D - Flipflop on kit
POWER
D
Clock
7400(NAND)
7400(NAND)
Vcc
GND
R0:330 ohm
R1:330 ohm
Q
Q'
TRUTH TABLE
PRINT
Add
Serial No. | clock | D | Q(n-1) | Q'(n-1) | Q | Q' | Remark
1 | 1 | 0 | 0 | 1 | 0 | 1 | set
2 | 0 | 1 | 0 | 1 | 0 | 1 | No change
3 | 1 | 1 | 0 | 1 | 1 | 0 | set
4 | 1 | 0 | 1 | 0 | 0 | 1 | Reset
CLOCK DIAGRAM
Q̄=1
Q̄=0
Q=1
Q=0
D=1
D=0
C=1
C=0
y-axis
x axis


INSTRUCTIONS
Experiment to perform logic of JK FLIP FLOP on kit
SUPPLY
Vcc: +5V
Vcc
GND
J
K
CLK
R1: 330ohm
LED 1
Q̄
R2: 330ohm
LED 2
Q
TRUTH TABLE
PRINT
Add
Serial No. | clock | J | K | Q(n-1) | Q̄(n-1) | Q | Q̄ | Remark
1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | No change
2 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | set
3 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | Reset
4 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | toggle
CLOCK DIAGRAM
Q̄=1
Q̄=0
Q=1
Q=0
K=1
K=0
J=1
J=0
CLK=1
CLK=0
y-axis
x axis
4 cm of rain
In 4 hours



Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	1	0	x	x	0	1	No change
2	1	1	0	1	1	0	Toggle
3	1	1	1	0	0	1	Toggle
4	1	0	0	1	0	1	No change

Conclusion:
The experiment successfully verified the truth table of JK flip-flop using IC 7476 and demonstrated conversion of JK flip-flop into D and T flip-flops. It enhanced understanding of sequential circuits, flip-flop operations, and their applications in digital memory systems.

Signature of faculty in-charge with Date: