

Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	16/10/2025	Batch No:	B2
Faculty Name:		Roll No:	16010124107
Faculty Sign & Date:		Grade/Marks:	/25

Experiment No: 7
Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

CO3: Design synchronous and asynchronous sequential circuits.

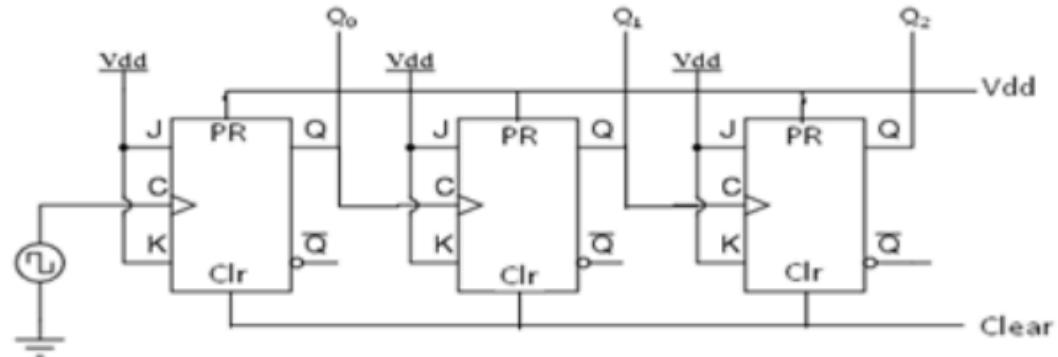
Tools used:

Trainer kits

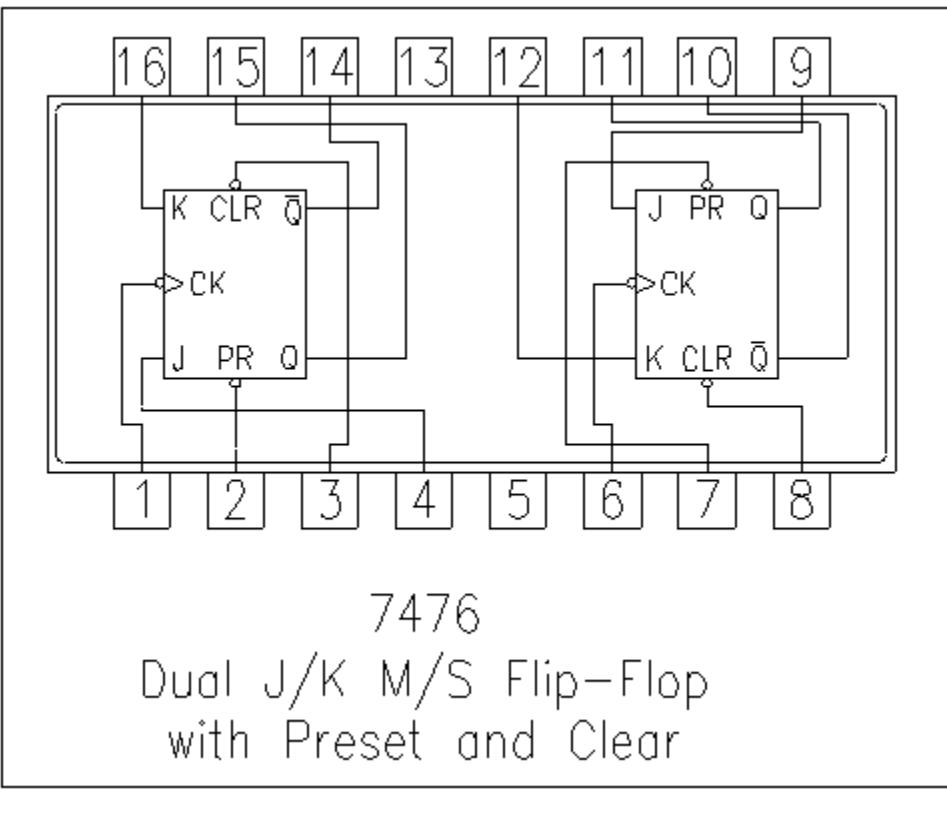
Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)

Logic Diagram for 3-bit Up Counter:



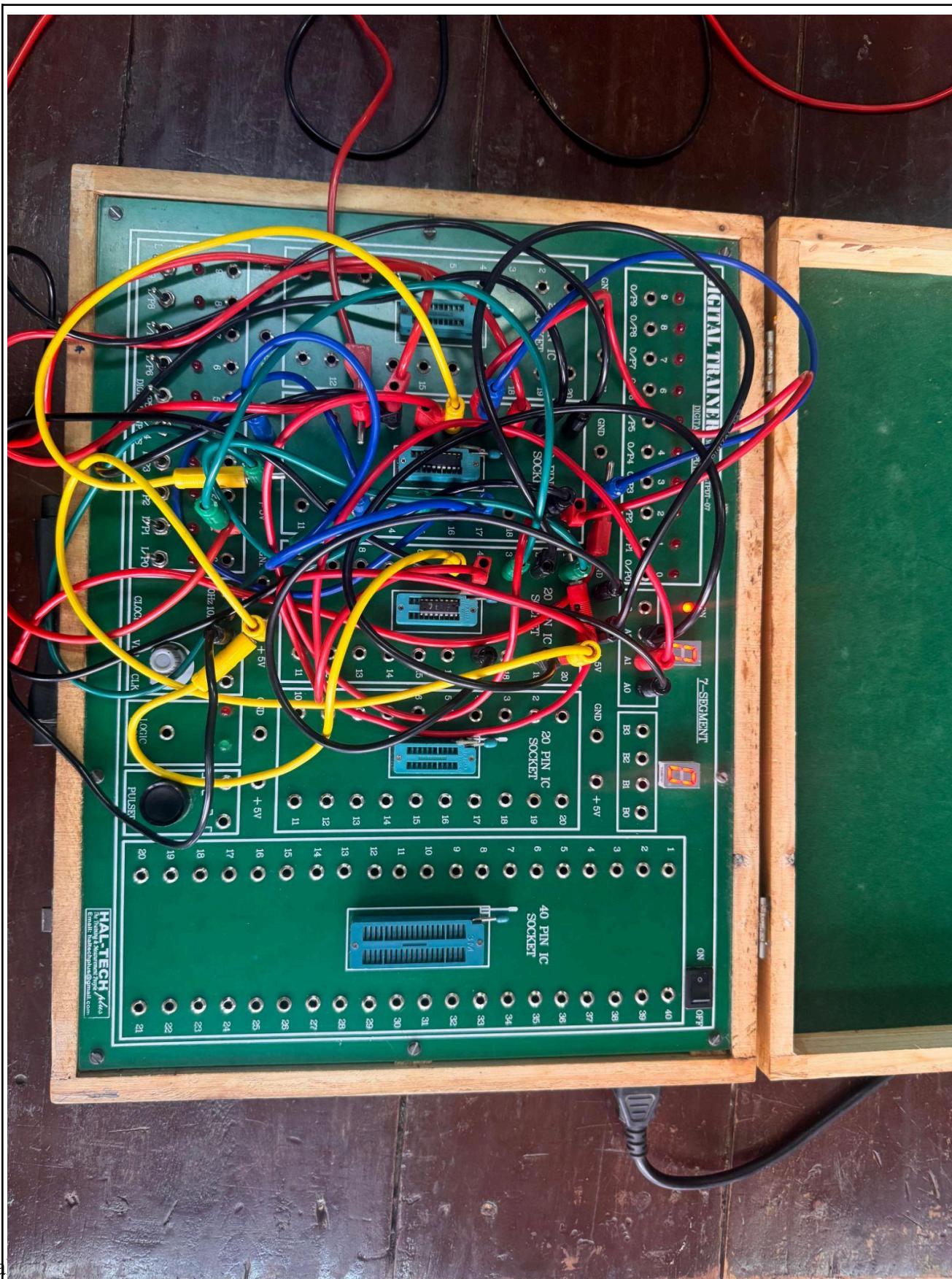
Pin diagram of JK FF (IC 7476)

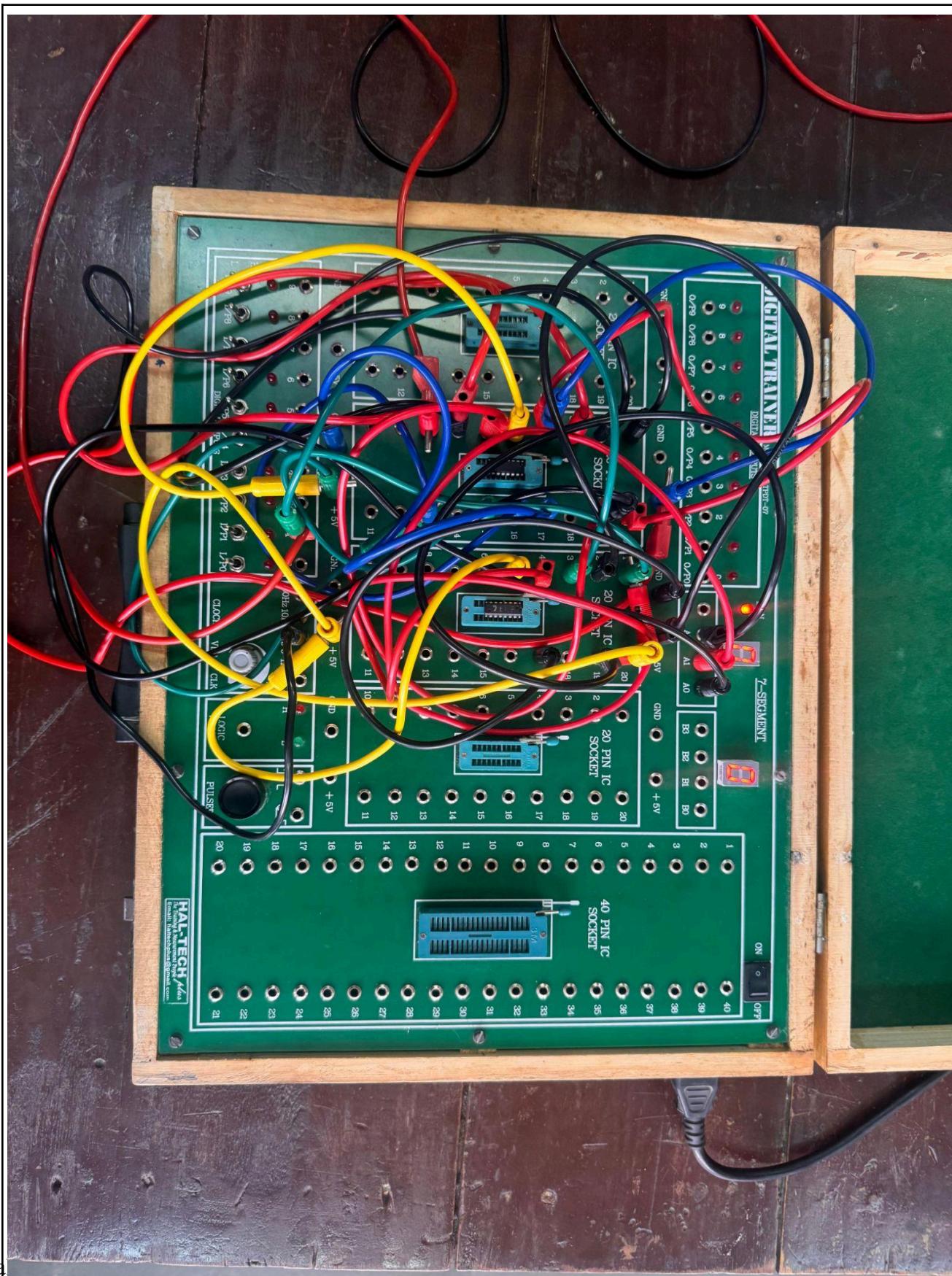


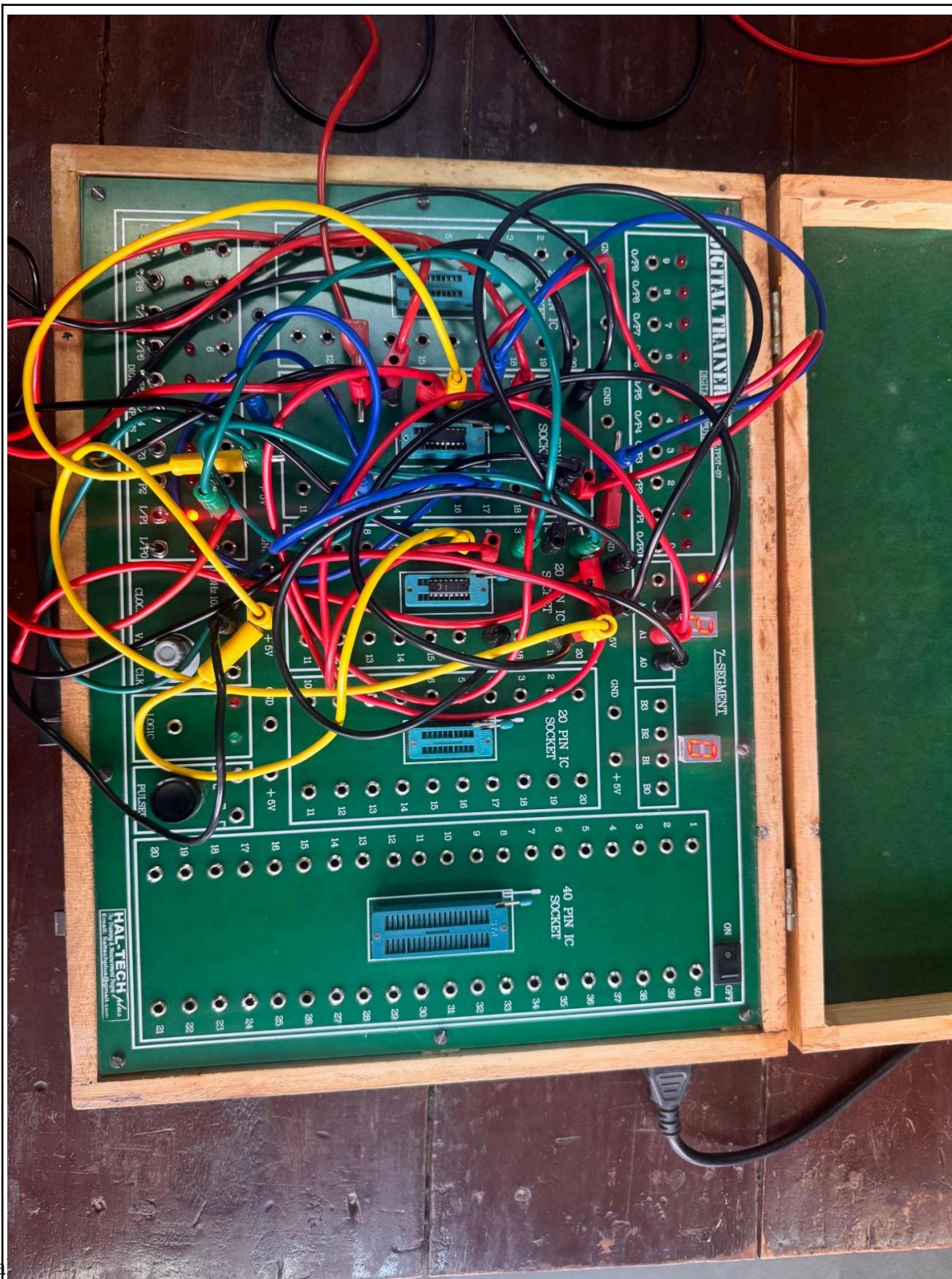
Implementation Details

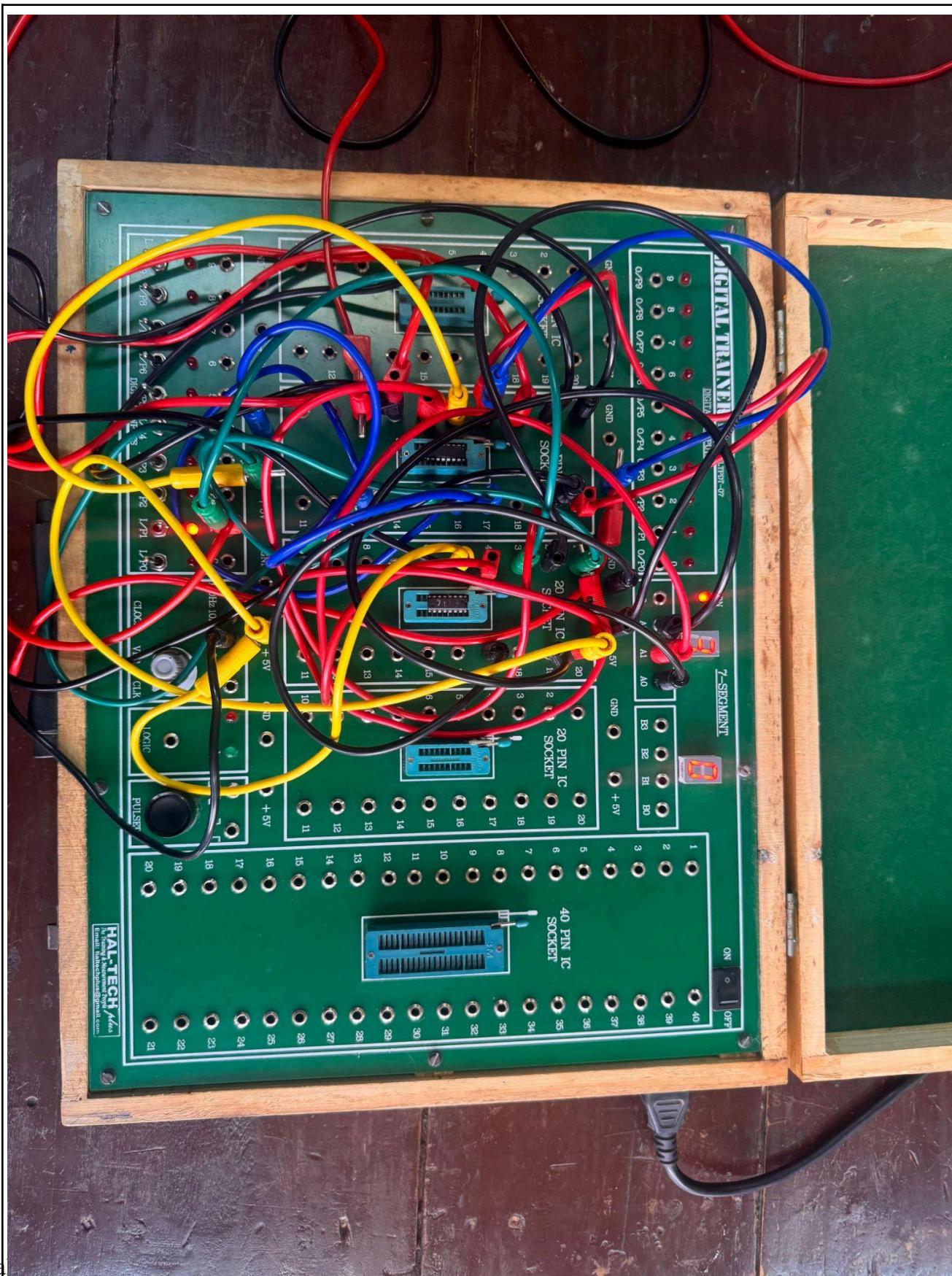
Procedure

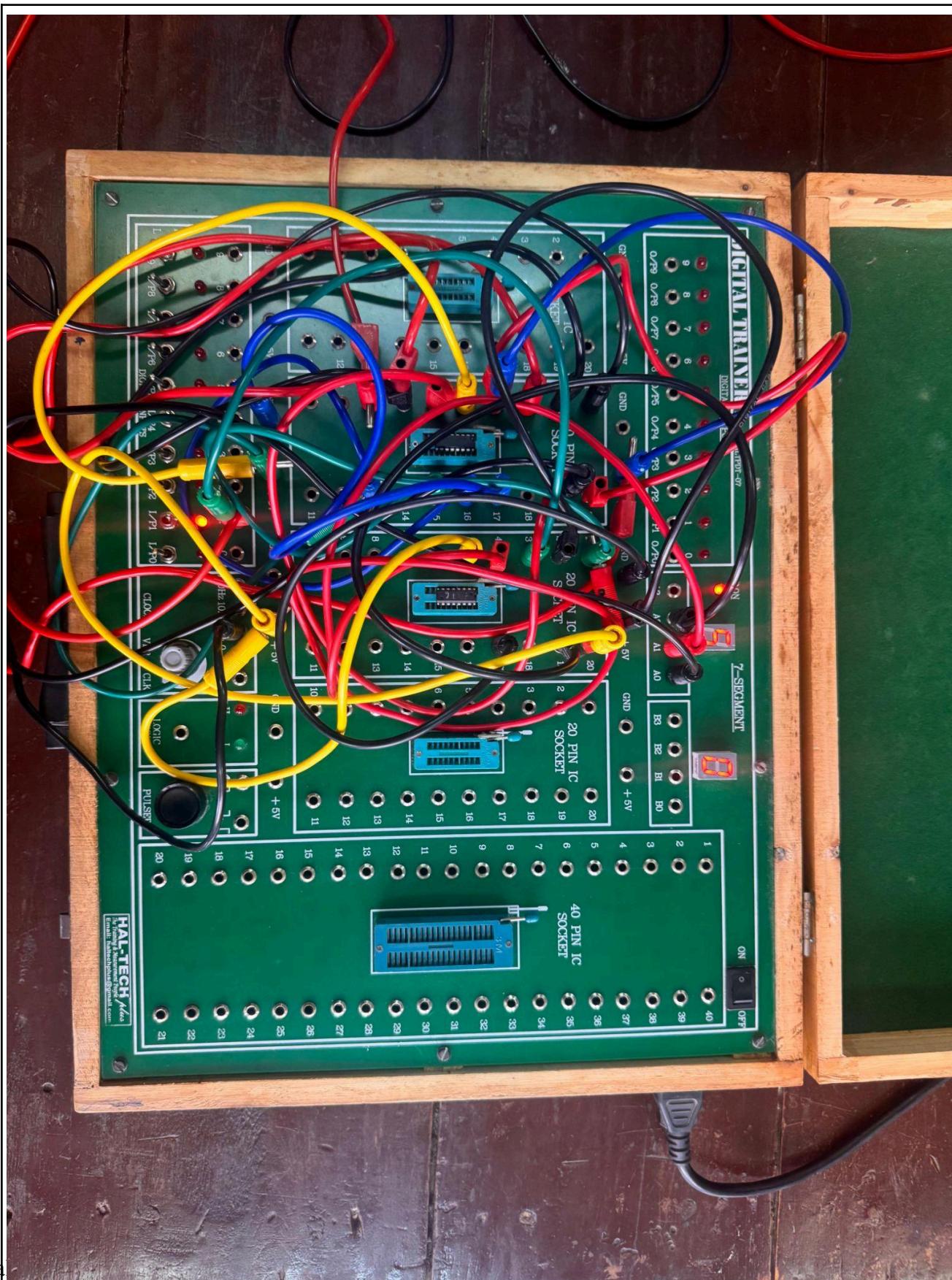
- 1) Locate IC 7476 JK FF on Digital trainer kit
- 2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
- 3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
- 4) Connect a pulsar switch to the clock input.
- 5) Verify the working and prepare a truth table.

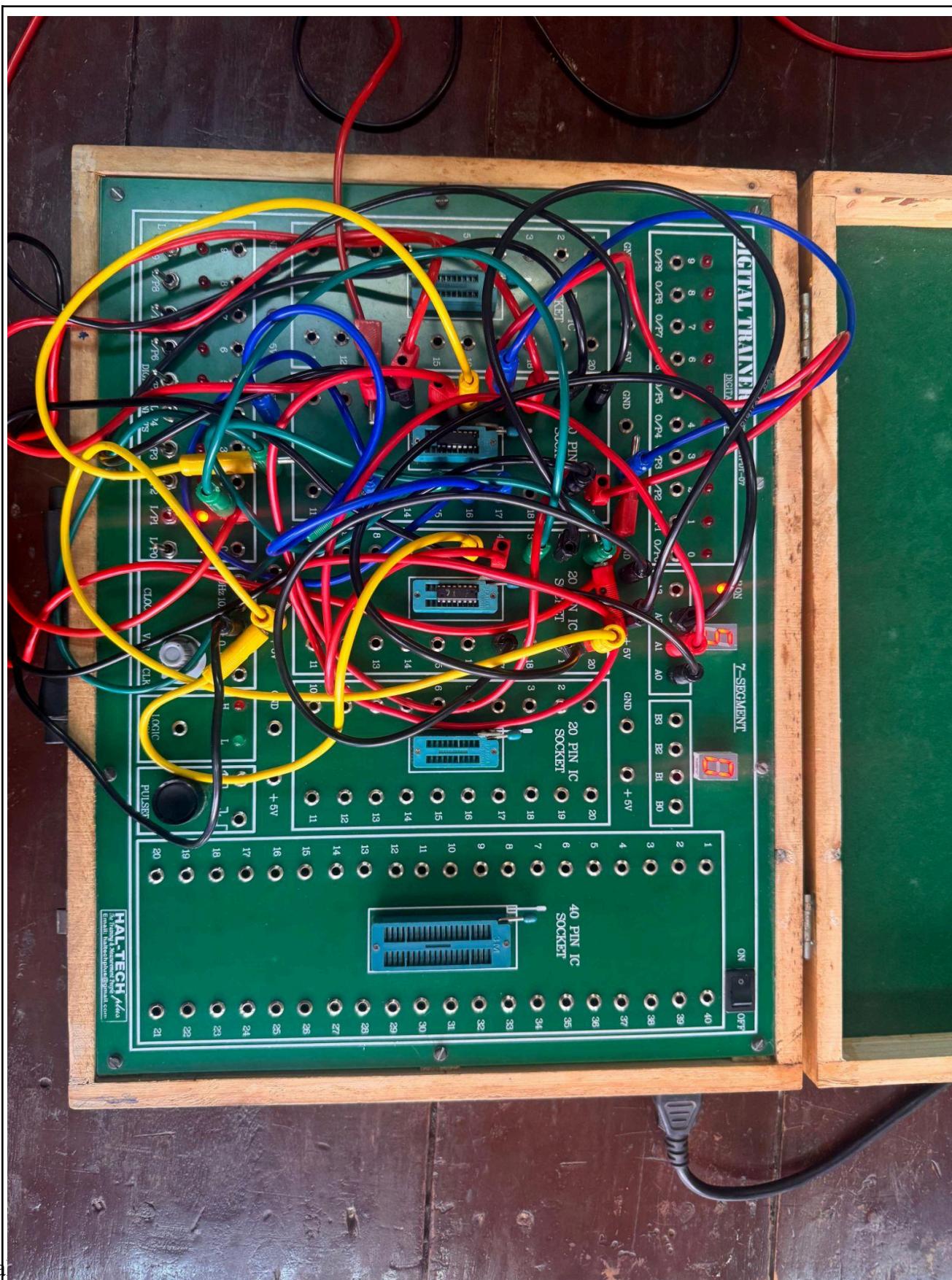


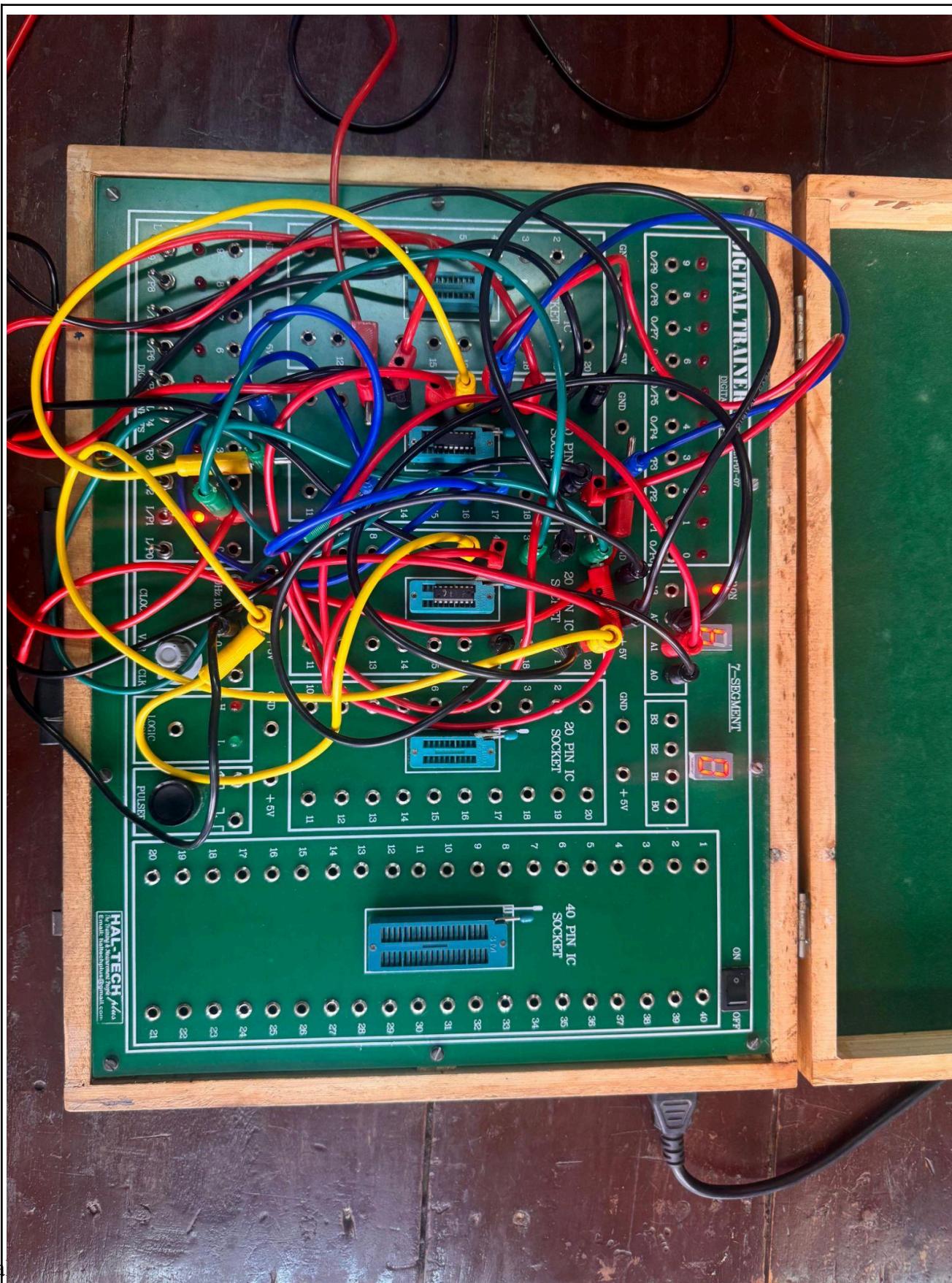


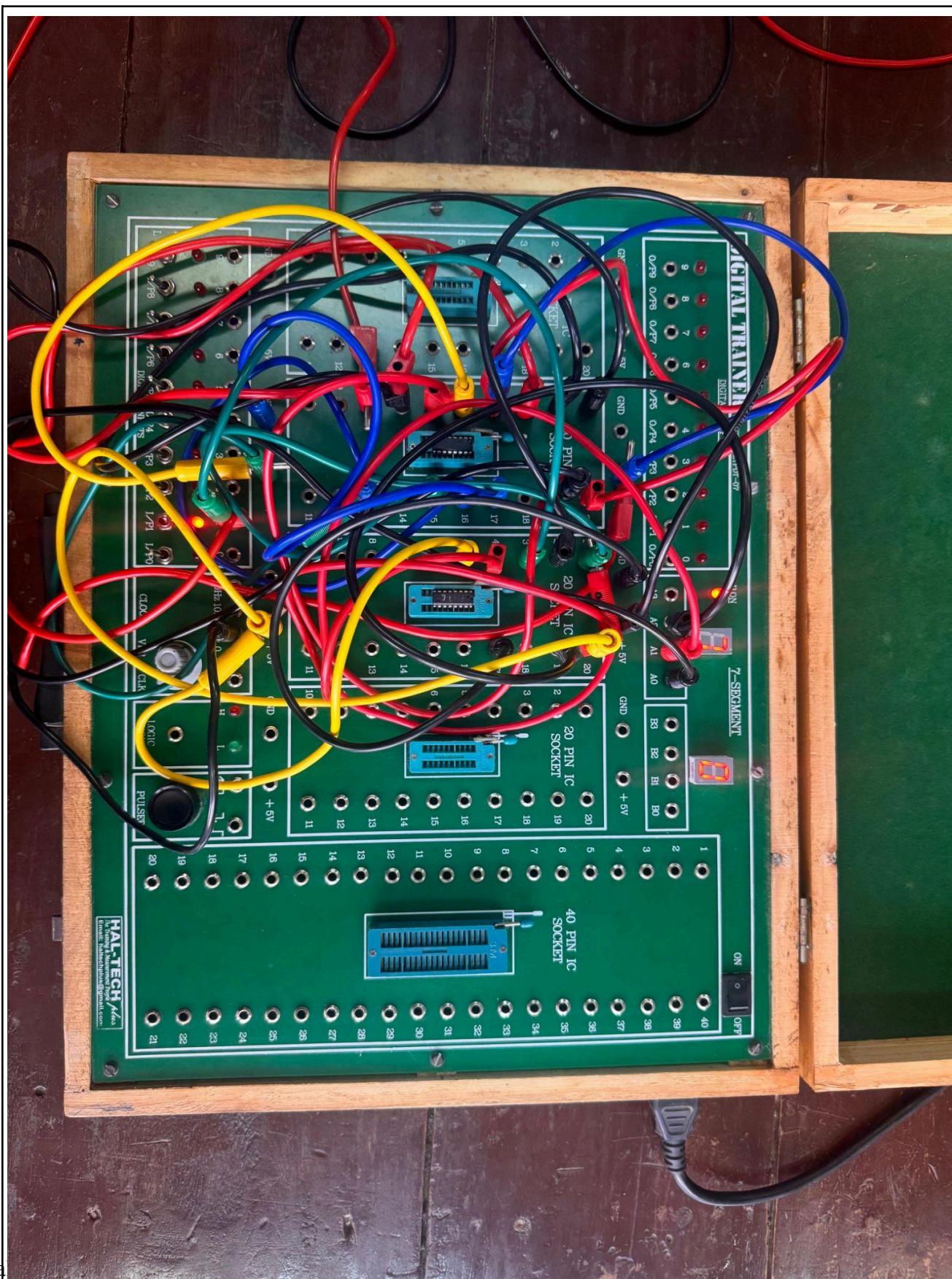


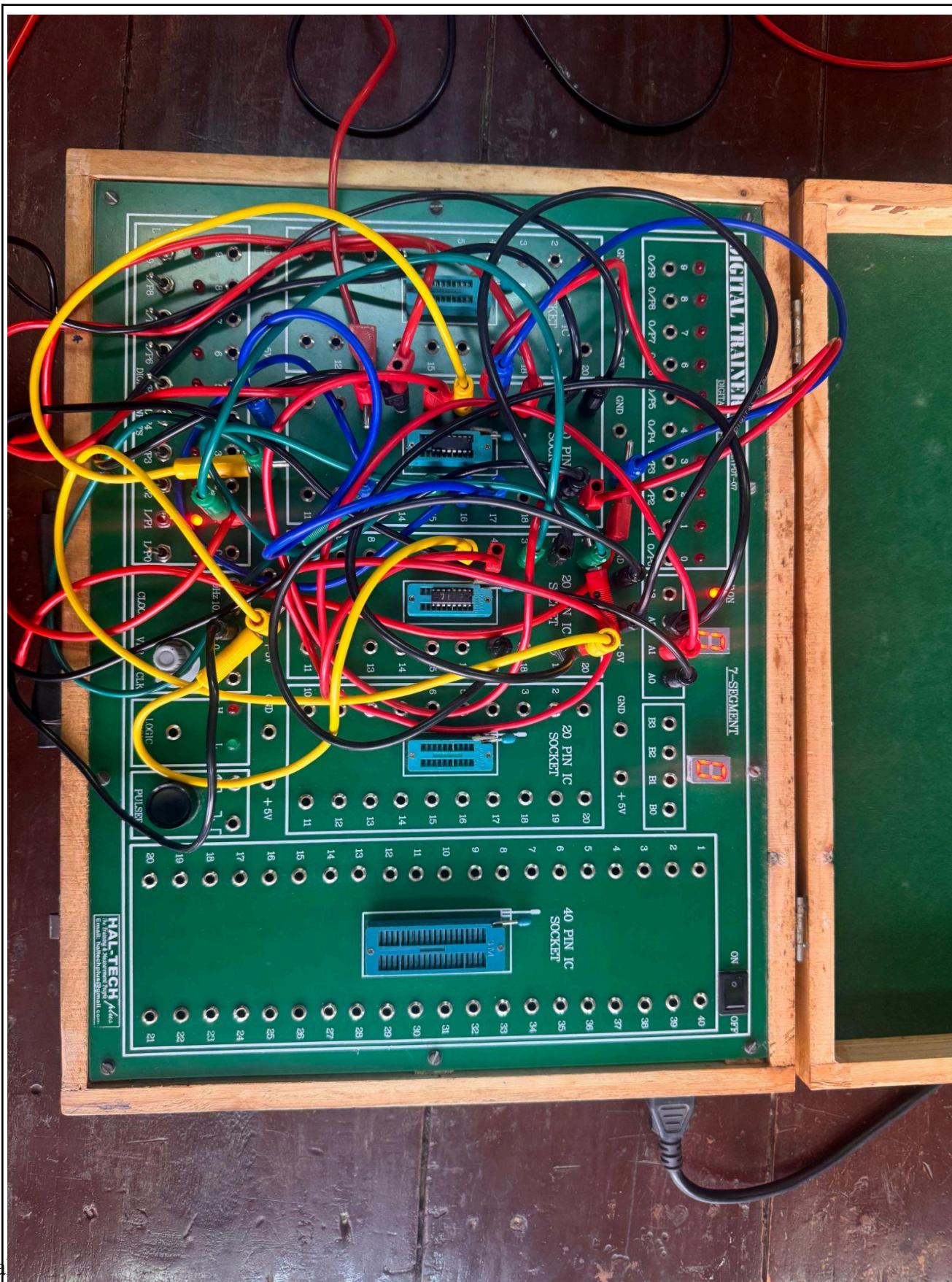


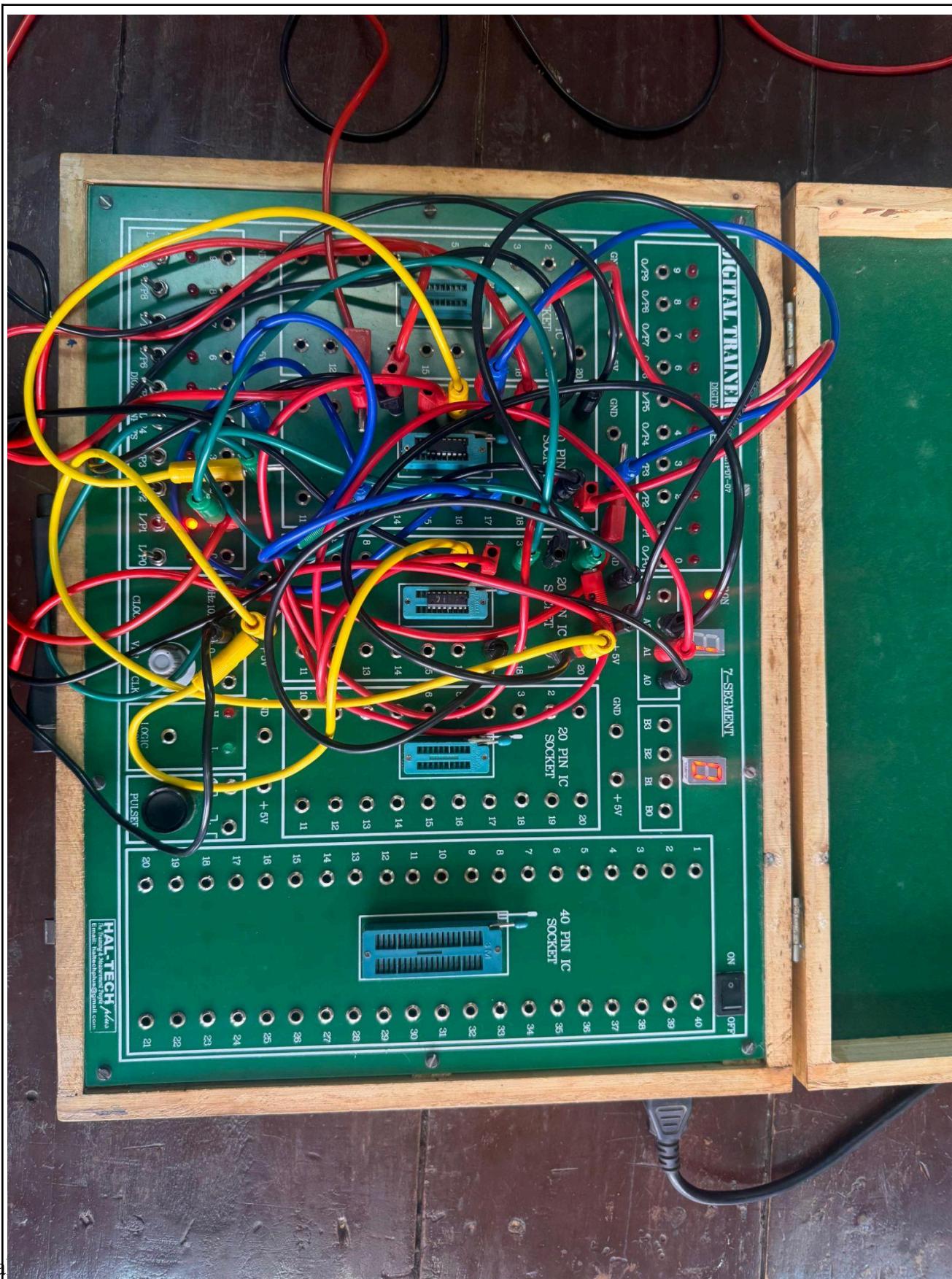


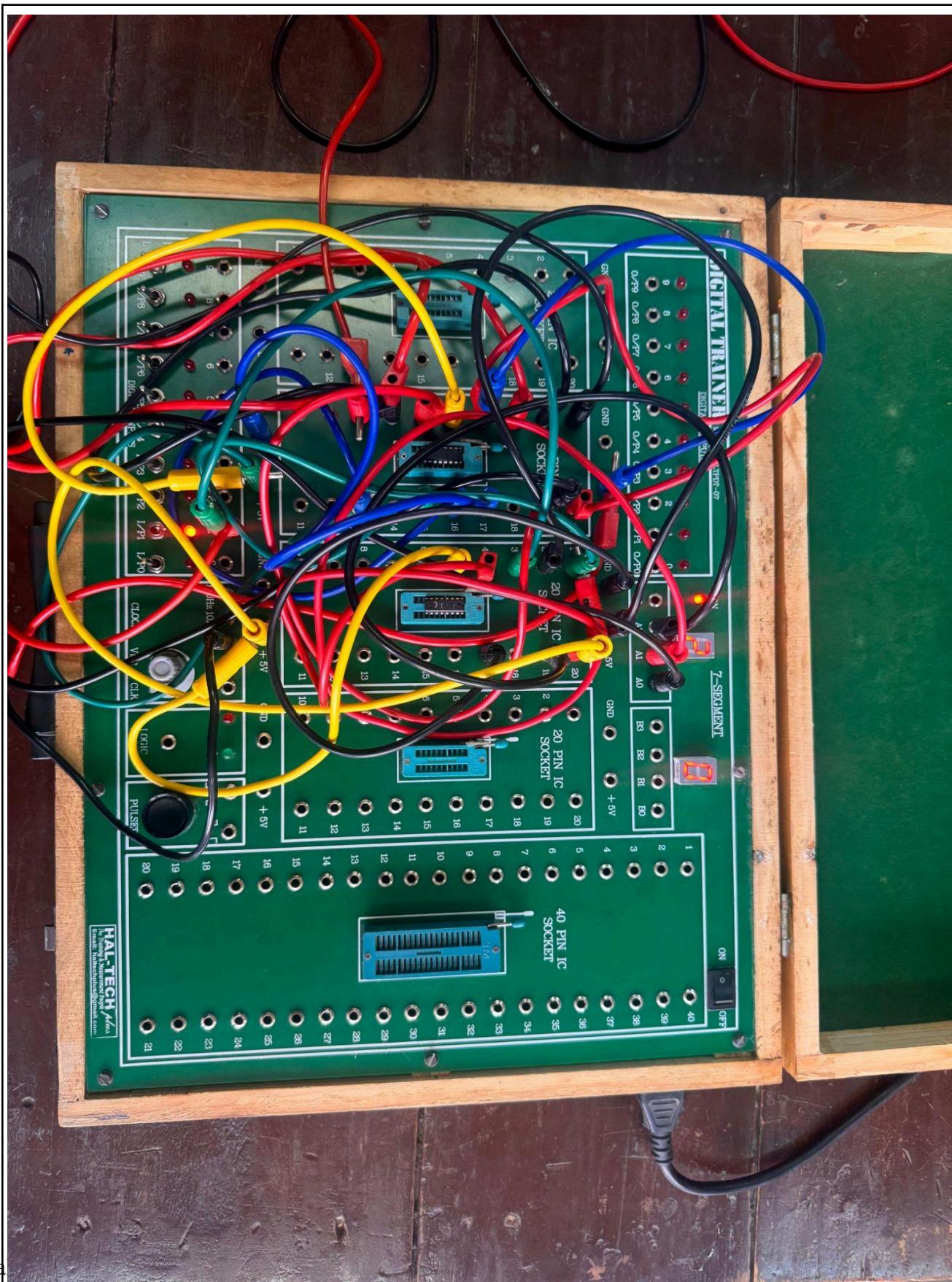












Post Lab Subjective/Objective type Questions:

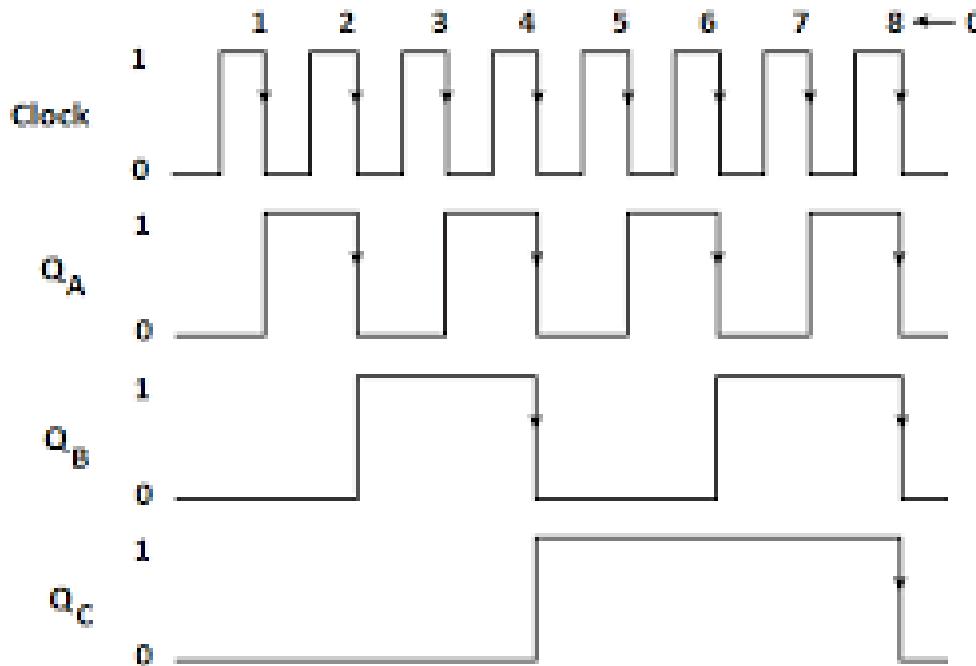
1. How JK FF need to be configured to use for counter operation?

To use JK flip-flops for a counter, you configure them in their "toggle" mode by connecting both the J and K inputs to a high logic level (logic 1). The flip-flops are then cascaded together, and a clock signal is used to control when they change state.

2. What changes are required to use the same counter as 3 bit asynchronous down counter?

To change an asynchronous up-counter into a down-counter, you must change the clocking of the flip-flops; instead of using the normal output of the previous flip-flop as the clock for the next, use the complemented output. The first flip-flop is still driven by the external clock, but the clock inputs for the subsequent flip-flops will be the inverted outputs of the flip-flops before them.

3. Draw the timing diagram of 3 bit Asynchronous up counter.



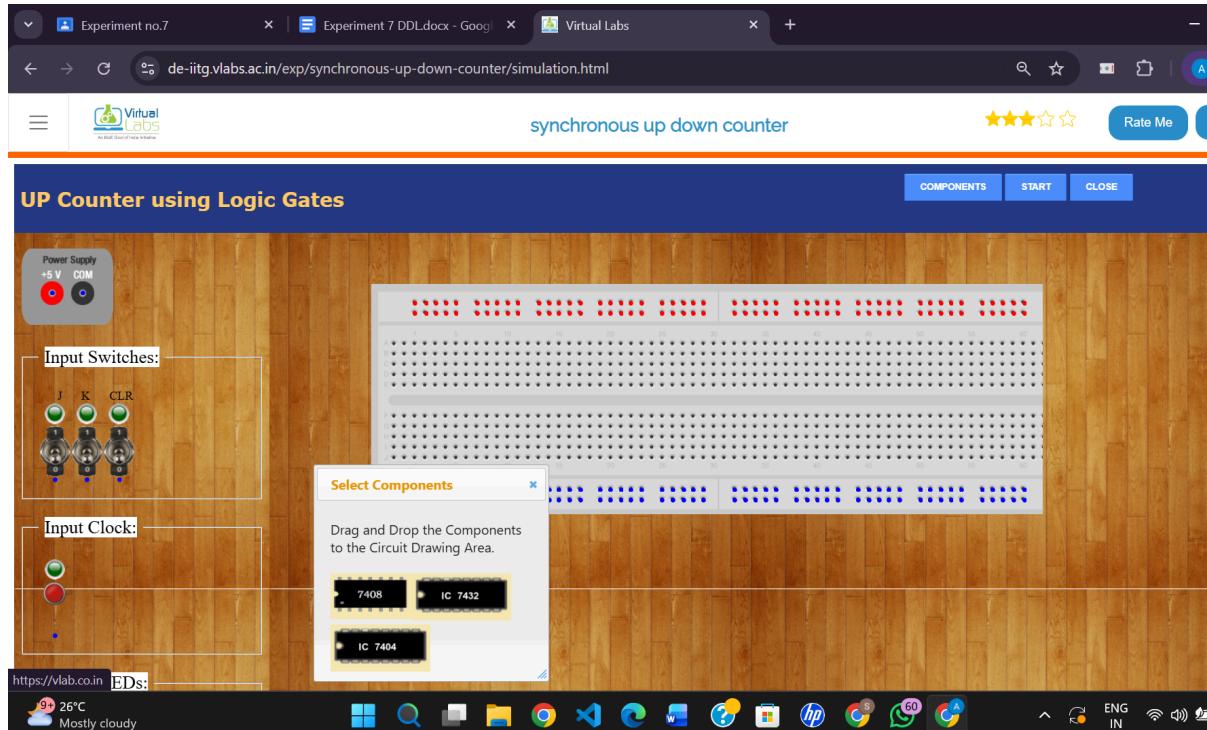
4. What is mod n concept used in counters?

The "mod n" concept in counters refers to a counter that has a specific number of states, or a modulus, before it cycles back to its starting state. A mod-n counter counts from 0 to $(n-1)$ and is also known as a "divide by n" counter because it divides the input frequency by n. For example, a mod-4 counter has four states and cycles through 00, 01, 10, and 11 before returning to 00, and a mod-10 counter counts from 0 to 9 and then resets.

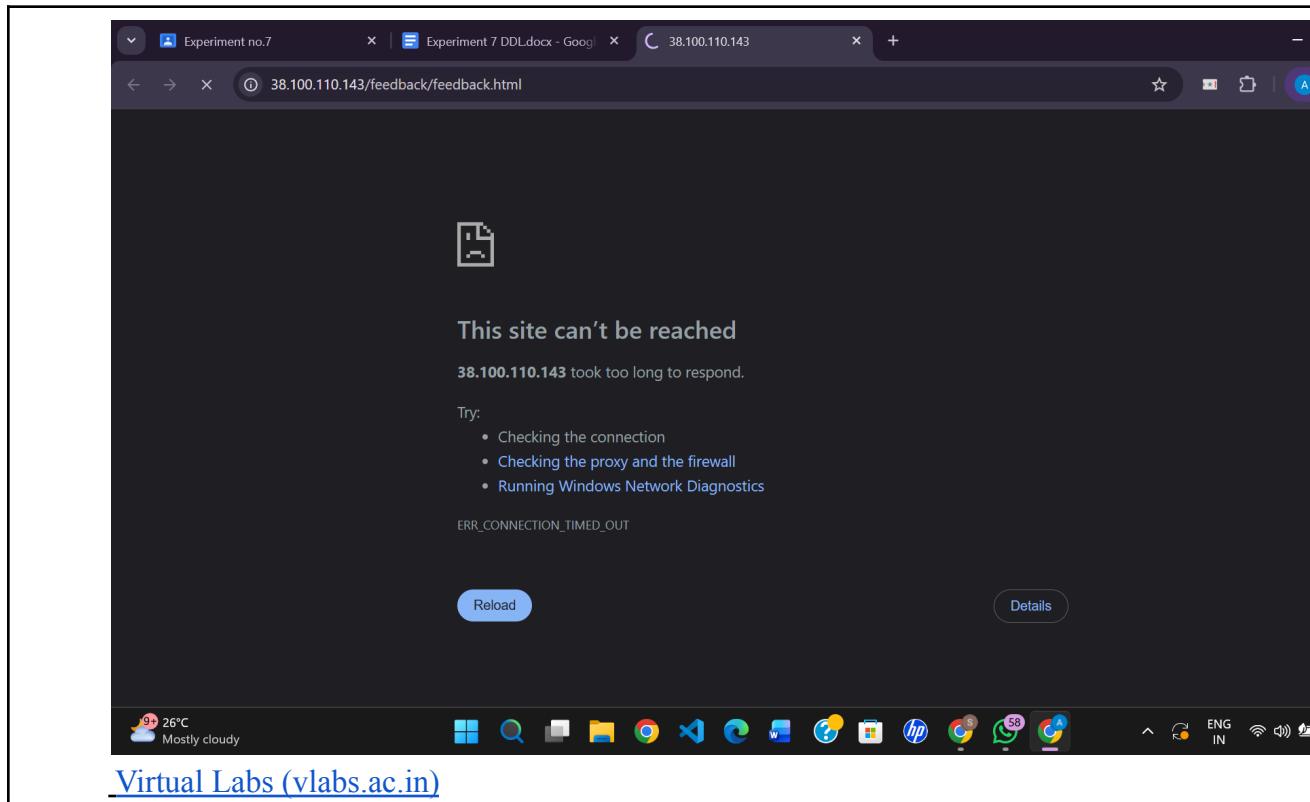
5. For Mod-5 counter how many JK FFs are required?

A Mod-5 counter requires 3 JK flip-flops because you need enough states to represent at least 5 different counts (0 through 4). The number of states available with n flip-flops is 2^n , so the smallest power of 2 that is greater than or equal to 5 is $2^3=8$, indicating that 3 flip-flops are necessary.

6. Virtual Lab for synchronous up down counter. Perform Simulation give feedback.
Feedback: Cannot use synchronous up or down counter as the screen does not have IC component



Required IC: 7473 is missing
Feedback form is also unavailable





1. UP-DOWN counter is a combination of:

- a: Latches
- b: Flip-flops
- c: UP counter
- d: Up counter & down counter

2. Binary counter that count incrementally and decremently is called

- a: Up-down counter
- b: LSI counters
- c: Down counter
- d: Up counter

3. UP-DOWN counter is also known as

- a: Dual counter
- b: Multi counter
- c: Multimode counter
- d: None of the mentioned

Submit Quiz

3 out of 3

Conclusion:

The experiment successfully demonstrated the design and operation of a 3-bit asynchronous up counter using JK flip-flops. The counter worked correctly in toggle mode, showing sequential binary counting. This helped understand flip-flop interconnections, clock propagation delays, and the mod-n counting concept in asynchronous sequential circuit design.

Signature of faculty in-charge with Date: