Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**30/10/2025**	**Batch No:**	**B2**
Faculty Name:		**Roll No:**	**16010124107**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 8
Title: 1-bit adder on VHDL

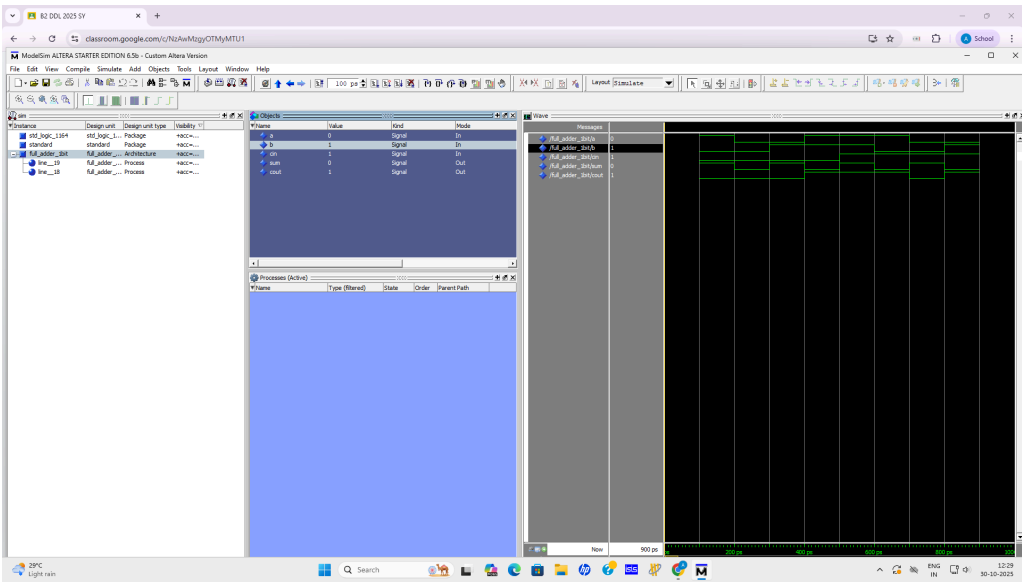
Aim and Objective of the Experiment:
To implement 1-bit adder on VHDL

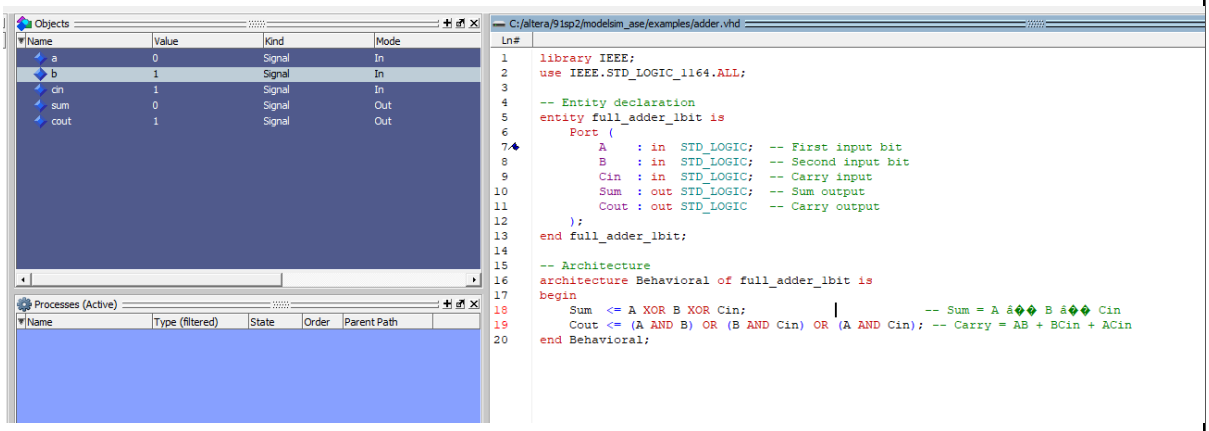
COs to be achieved:
CO4: Implement digital networks using VHDL

Tools used:
Quartus, ModelSim

Theory:
A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input. Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems.

Implementation Details





Post Lab Subjective/Objective type Questions:

1. How can 1-bit adder be used to implement a 4-bit adder?

A 1-bit adder is used to implement a 4-bit adder by connecting four 1-bit full adder circuits in a cascading or "ripple-carry" fashion. The carry-out from one full adder is connected to the carry-in of the next one, with the first stage using a half-adder or a full-adder with a carry-in of 0. This process adds the corresponding bits of two 4-bit binary numbers, plus the carry from the previous stage.

2. What is VHDL used for?

VHDL is used to describe the behavior and structure of digital circuits for design and simulation. It allows engineers to model complex digital systems, like microprocessors and memory devices, and then test the design before implementing it in hardware, saving energy, resources, and time.

Conclusion:
VHDL provides a robust and standardized framework for modern digital system design, bridging the gap between abstract concepts and physical hardware implementation through a structured process of modeling, simulation, and synthesis.

Signature of faculty in-charge with Date: