

# **K. J. Somaiya College of Engineering, Mumbai-77** (A Constituent College of Somaiya Vidyavihar University)



**Department of Computer Engineering** 

Batch: B2 Roll No.: 16010124107

Name: Ashwera Hasan Experiment No. 01

TITLE: Study of PCI and SCSI buses.

**AIM: To Study and learn PCI and SCSI** 

Expected OUTCOME of Experiment: Describe and define the structure of a computer with buses structure and detail working of the arithmetic logic unit and its sub modules

#### **Books/ Journals/ Websites referred:**

- 1. <u>https://www.techopedia.com/definition/8815/peripheral-component-interconnect-bus-pci-bus</u>
- 2. <a href="https://www.techopedia.com/definition/331/small-computer-system-interface-scsi">https://www.techopedia.com/definition/331/small-computer-system-interface-scsi</a>
- 3. <a href="http://www.csun.edu/~edaasic/roosta/BUS">http://www.csun.edu/~edaasic/roosta/BUS</a> Structures.pdf
- 4. W. Stallings William "Computer Organization and Architecture: Designing for Performance", Pearson Prentice Hall Publication, 7thEdition. C.

#### **Pre Lab/ Prior Concepts:**

Microcomputer buses which communicate with a peripheral devices or a memory location through communication lines called buses.

The major parts of microcomputers are central processing unit (CPU), memory, and input and output unit. To connect these parts together through three sets of parallel lines, called buses. These three buses are address bus, data bus, and control bus.

#### **Address Bus:**

The address bus consists of 16, 20, 24, or more parallel signal lines, through which the CPU sends out the address of the memory location. This memory location is used for to written to or read from. The number of memory location is depends on 2 to the power N address lines. Example, a CPU with 16 address lines can address 2^16 or 65,536 memory locations. When the CPU reads data from or writes data to a port, the port address is also sent out on the address bus. This is unidirectional. This means that the CPU can send data to a memory location or I/O ports.

#### **Data Bus:**

The data bus consists of 8, 16, 32 or more parallel signal lines. The data bus lines are bidirectional. This means that the CPU can read data from memory or from a I/O port as well as



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send data to a memory location or to a I/O port. In a system, many output devices are connected to the data bus, but only one device at a time will be enabled to the output.

#### **Control Bus:**

The control bus consists of 4-10 parallel signal lines. The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or port devices. Typically control bus signals are memory read, memory write, I/O read and I/O write. To read a data from a memory location, the CPU sends out the address of the desired data on the address bus and then sends out a memory read signal on the control bus. The memory read signal enables the addressed memory device to output the data onto the data bus where it is read by the CPU.

#### **PCI Bus**

PCI stands for Peripheral Component Interconnect Bus. It connects the CPU to the expansion boards like modem, network and sound cards, etc. The main functionality of a PCI bus is to add to the functionality of the computer system. It mainly operates on 64 bits and at a very high speed. However, it may not support older systems and costs more. Due to the growing demand of data transfer today, older PCI architecture is becoming outdated. In the future, a newer version called the PCI Express will replace to meet the need of technology for another ten years.

Ref: https://webstor.srmist.edu.in/web assets/srm mainsite/files/files/PCI.pdf

## **SCSI bus:**

SCSI stands for small computer system interface. Its main purpose is to connect peripheral devices to the computer system. Generally, it can support up to 16 peripheral devices including the host adapter on a single bus. SCSI increases performance and speed in achieving larger expansion for devices like scanners, CD writers, etc. There are four main components of an SCSI.

The initiator issues requests for service and receives responses. The target is simply a physical storage device. A service delivery subsystem allows for communication between the target and initiator. An expander helps multiple SASs share a single initiator port.

#### Ref:

https://www.geeksforgeeks.org/computer-networks/what-is-small-computer-system-interface-e-scsi/

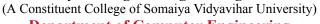
# **Post Lab Descriptive Questions:**

# Q1. Differentiate between PCI and SCSI Bus

PCI	SCSI
Connects CPU to expansion boards	Connects CPU to peripheral devices



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Operate on 64 bits	Operate on 8-16 bits
It is a parallel bus technology	It is faster on series bus technology (sas)
General purpose bus that accommodates many	Specialized bus mainly used for storage and
devices	peripheral devices

# Q2. List two applications each of PCI and SCSI Bus

# PCI Bus Applications:

- Connect hardware devices to CPU's motherboard
- Works as a plug and play system, allowing for easier adding and removing of expansion cards

### SCSI Bus Applications:

- In RAID configurations to provide data redundancy, improved performance and increased speed.
- Connect peripheral devices to the computer's motherboard. Allows for a faster data transfer with reduced latency.

#### **CONCLUSION:**

Buses are used to connect the three parts of the CPU together. The address bus is responsible for sending out the address of a memory location. The data bus is responsible for taking input and issuing output to a memory location. The control bus sends signals that initiate these actions. A PCI bus helps to attach several extension boards to the motherboard for added functionality. Via this bus, sound cards and graphic cards are connected in the computer. An SCSI bus connects the peripheral devices to the computer system and essentially boosts the speed of data transfer.

Date:	18/07/2025	
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