

(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering** 



Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	21/ 08/ 2025	Batch No:	B2
Faculty Name:		Roll No:	16010124107
Faculty Sign & Date:		Grade/Marks:	/25

# **Experiment No: 4**

Title: 4-bit magnitude comparator

Aim and Objective of the Experiment:
To design and implement 1-bit comparator using logic gates and verify 4-bit magnitude comp

To design and implement 1-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

#### COs to be achieved:

CO2: Use different minimization techniques and solve combinational circuits.

Tools used:	
Trainer kits	

#### Theory:

**Comparator:** The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.

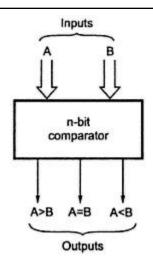
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## 1-bit Comparator Implementation Details: Truth Table

A	В	A <b< th=""><th>A=B</th><th>A&gt;B</th></b<>	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

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From the Truth Table:

(A < B) =

(A=B)=

(A>B)= ...refer the table above

Logic Diagram of 1-bit Comparator

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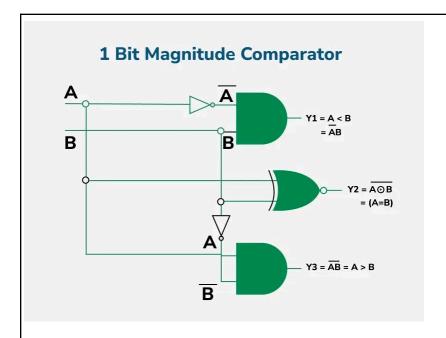
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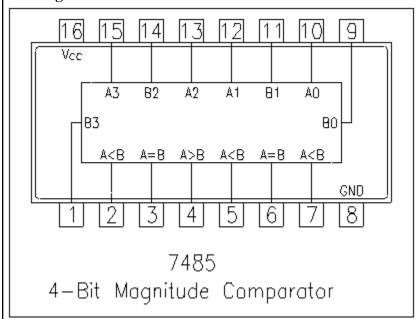
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## Four Bit Magnitude Comparator Implementation Details

# Pin Diagram of IC 7485



Logic Diagram of IC 7485

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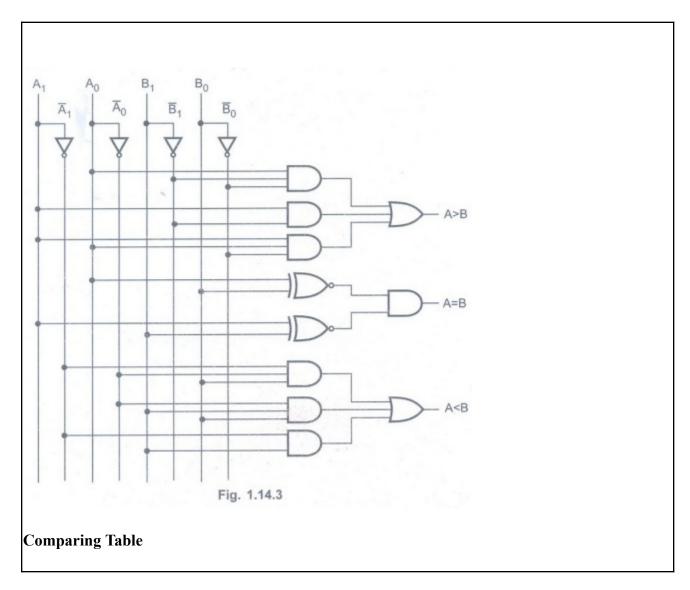
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	Entrées des nombres			Entrées cascadables			Sorties			
	A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
Ī	A3 > B3	Х	Х	Х	Х	Х	Х	1	0	0
	A3 < B3	Х	X	ΧÏ	Х	Х	X	0	1	0
	A3 = B3	A2 > B2	Х	Х	Х	Х	Х	1	0	0
Ī	A3 = B3	A2 < B2	{ <b>X</b> €.	<u>X</u> X4.,	ξ <b>X</b> < .	X	<u> </u>	(0)	<u>(18)</u>	/.03
	A3 = B3	A2 = B2	A1 > B1	X	Х	X	X	§18	0	00
ſ	A3 = B3	A2 = B2	A1 < B1	X	( x )	X	§ x>	0	110	0
Į	A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	110	0	0
,	A3 = B3	A2 = B2	A1 = B1	A0 < B0	Х	Х	Х	0	1	0
Ī	A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	0	1	0	0
Ī	A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1,	0	0	1	0
,	A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	1	0	0	1
	A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	1	0	0	1
	A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	0	0	0	0
-	A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	0	1:	1	0

#### **Implementation Details**

#### **Procedure:**

- 1) Locate the IC 7485 on the trainer kit.
- 2) Connect 1<sup>st</sup> input no. to A3-A0 input slot and 2<sup>nd</sup> to B3-B0.
- 3) Connect the output  $Y_{\text{A}>\text{B}}$  ,  $Y_{\text{A}<\text{B}}$  and  $Y_{\text{A}=\text{B}}$  to the output indicators.
- 4) Switch ON the power supply and monitor the output for various input combinations.

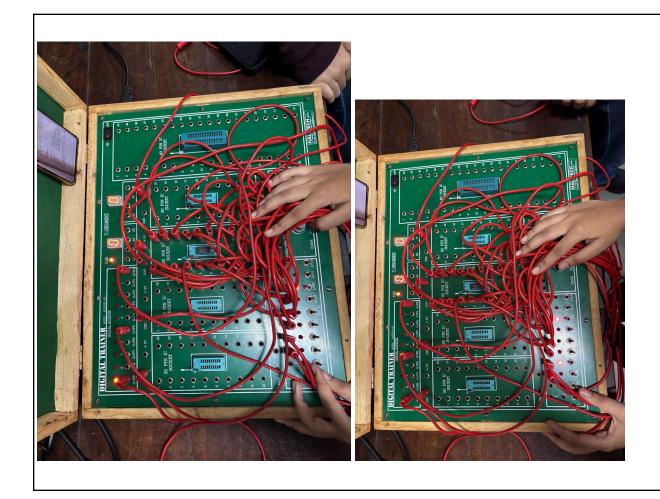
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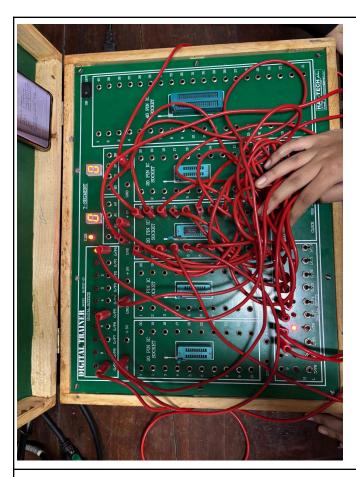
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Post Lab Subjective/Objective type Questions:

1. Design 2-bit magnitude comparator.

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A = B

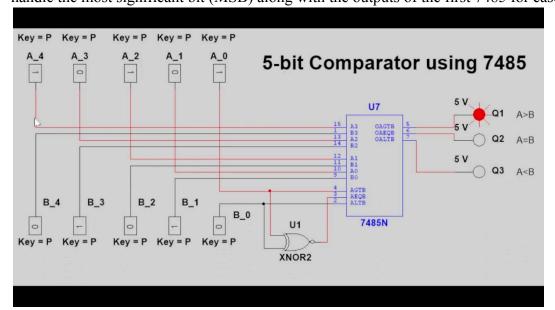
A < B



# 2 Bit Magnitude Comparator A1 A0 B1 B0 B A>B

2. How can we implement 5-bit magnitude comparator using IC 7485.

To create a 5-bit magnitude comparator using the 7485 IC, which is a 4-bit comparator, you need to cascade two 7485s. One 7485 will handle the lower four bits, and the other will handle the most significant bit (MSB) along with the outputs of the first 7485 for cascading.



3. Virtual Lab for 8 bit digital comparator using Virtual Lab (<u>Digital Logic Design</u>) Perform simulation.

Virtual Labs (vlabs.ac.in)

Give feedback for the experiments of virtual lab using somaiya email id.

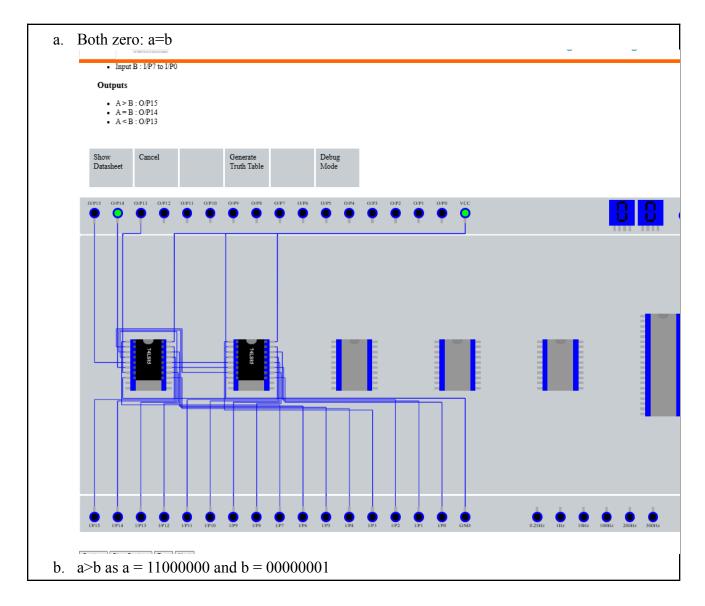
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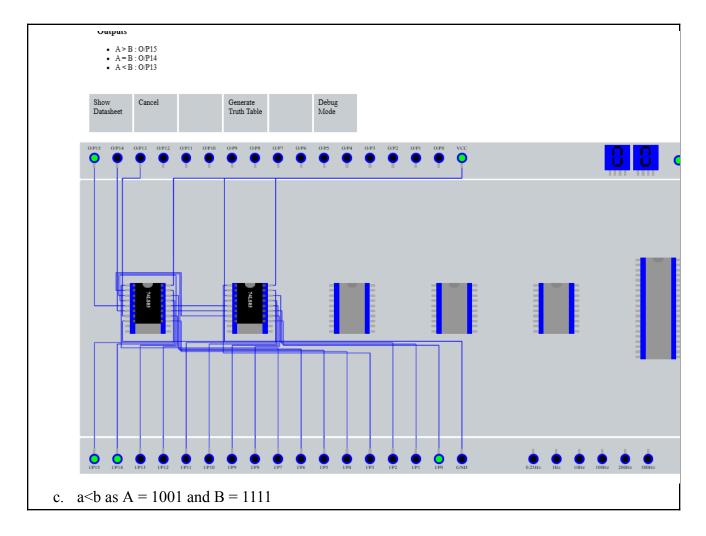
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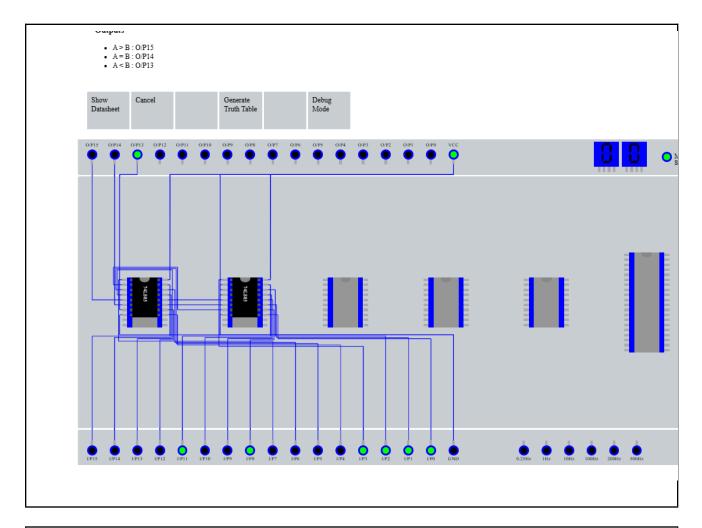


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#### **Conclusion:**

The experiment successfully demonstrated the design and working of a 1-bit comparator using logic gates and verification of a 4-bit magnitude comparator using IC 7485. It helped understand number comparison logic, cascading technique, and practical implementation on trainer kits, reinforcing concepts of combinational circuits and digital system design effectively.

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Signature of faculty in-charge with Date:

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