# COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE 14:332:331

## Rutgers University Maria Striki Spring 2021

Homework 2A: 55 pts = 7 + 9 + 12 + 11 + 12 + 4 pts

Issued on: Wed 02-17-2021 Due on: Fri 02-26-2021 at 22.00

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#### Problem 1 (7 pts):

**Part 1 (4 pts):** Translate the following C code to RISC-V assembly code, using the minimum number of instructions you can think of. The values of: w, y, i, j are in registers: x4, x5, x6, x7. Register x8 holds the based address of array A.

```
for (i=0; i<=w; i++)
for (j=0; j<y; j+=2)
A[3*i + j] = 2*i +3*j;
```

Code in RISC V Assembly Code:

```
x4 = w
x5 = y
x6 = i
x7 = j
add x6, x0, 0 // i = 0
```

Loop 1:

```
bne x6, x4, Exit // loop goes to exit if i != to w addi x6, x6, 1 // i = i + 1 add x7, x0, 0 // j = 0
```

Loop 2:

```
beq x7, x5, LOOP 1 // loop goes to exit if i != to w
addi x7, x7, 2 // i = i + 2
slli x30, x6, 3 // x30 = 3*i
addi x30, x30, x7 // x30 = 3*i +j
add x30, x30, x8 // x30 = A[3*i+j]
slli x28, x6, 2 // x28 = i*2
slli x29, x7, 3 // x28 = j*3
add x31, x28, x29 //x31 = x28 + x29
sd x31, 0(x30) // A[3*i +j] = 2*i + 3*j
```

```
beq x0, x0, LOOP 2
```

**EXIT** 

**Part 2 (3 pts\_:** How many RISC-V instructions are needed to implement the above code? If w and y are initialized to 3 and 6 and elements of A are initially 0, what is the total number of RISC-V instructions executed to complete the loop?

Total Instructions: 85 is including the initialization of values and the exits

# Problem 2: (9 pts)

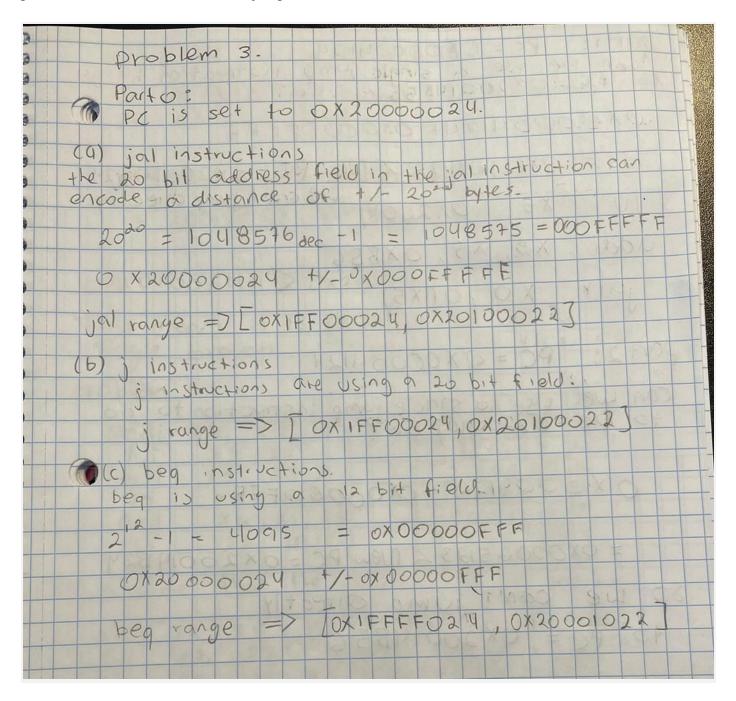
Find the shortest sequence of RISC-V instructions that extracts bits 19 down to 8 from register x7 and uses the value of this field to replace bits 26 down to 15 in register x4 without changing the other bits of registers x7 or x4. (Be sure to test your code using x7 = 0 and x4 = 0xffffffffffffff. Doing so may reveal a common oversight.)

#### **Solution:**

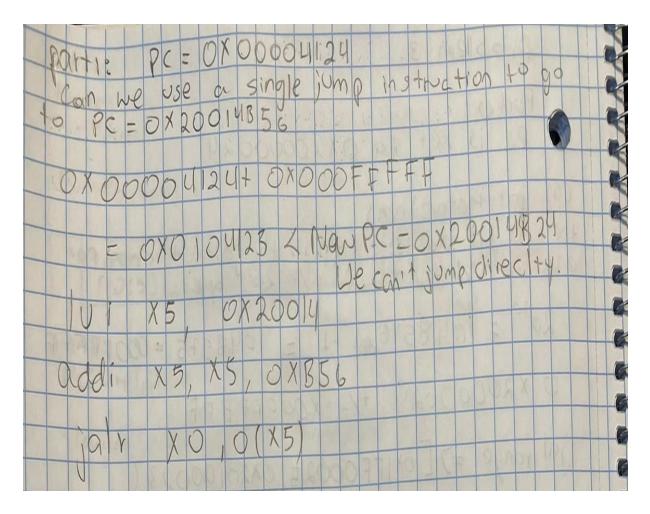
```
addi x5, x0, 0xFF // create a bit mask for 19 to 8
slli x5, x5, 8 // shifting masked bits
and x28, x7, x5 // apply mask to x7
slli x5, x4, 7 // shift the mark to cover bits 26 to 15
xori x5,x5,-1 // not an operation
and x4, x4, x5 // "zero out" positions 26 to 15 of x4
slli x28, x28,7 // move selection from x7 into positions 26 to 15
or x4, x4, x28 // load bits 26 to 15 from x28
```

## Problem 3: (12 pts, 3 pts each subpart)

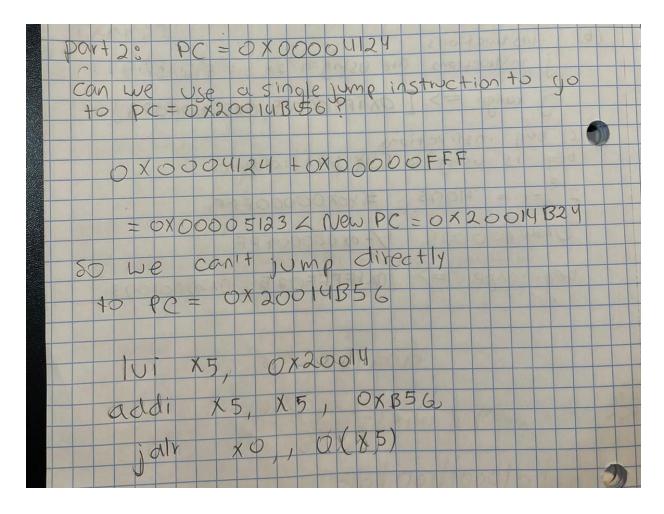
**Part 0:** Suppose the PC is set to 0x20000024. What range of addresses can be reached using the RISC V a) jal instruction, b) j instruction, c) beq instruction? In other words, what is the set of possible values for the PC after the jump instruction executes?



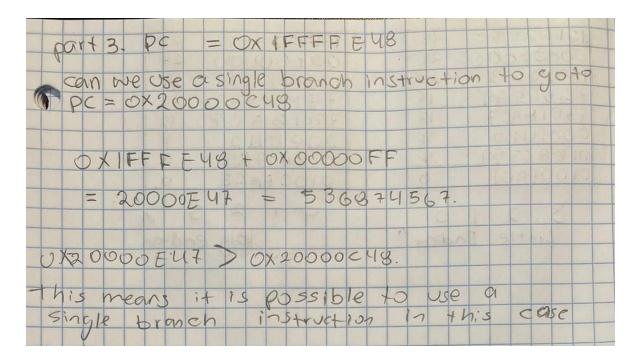
**Part 1:** Suppose that the current value of PC is 0x00004124. Can we use a single jump instruction to go to PC=0x20014B56? (if yes, write the jump instruction and show the value of the immediate field in Hex. If not, use a combinations of instructions to do so and show the immediate values in Hex)



**Part 2:** Suppose that the current value of PC is 0x00004124. Can we use a single branch instruction to go to PC=0x20014B56? (if yes, write the branch instruction and show the value of the immediate field in Hex. If not, use a combinations of instructions to do so and show the immediate values in Hex)



**Part 3:** Suppose that the current value of PC is 0x1FFFFE48. Can we use a single branch instruction to go to PC=0x20000C48? (if yes, write the branch instruction and show the value of the immediate field in Hex. If not, use a combinations of instructions to do so and show the immediate values in Hex)



# **Problem 4: (10 pts)**

**Part 1:** (3 pts) Consider the following code:

1b x5, 0(x10) sd x5, 8(x10)

Assume that register x10 contains address  $0\times10000000$  and the data at address is  $0\times7$ FEEDDCCCDBC2365.

**Q 1:** What value is stored in 0×10000008 on a big-endian machine?

Q 2: What value is stored in 0×10000008 on a little-endian machine?

**Part 2:** (**5 pts**) Write the RISC-V assembly code that creates the above 64-bit constant (0×7FEEDDCCCDBC2365) and stores that value to register x10.

**Part 3:** (2 pts) Provide the instruction type, assembly language instruction, and binary representation of instruction described by the following RISC-V fields: opcode=0x3, funct3=0x3, rs1=27, rd=3, imm=0x4

#### Solution:

Part 1 Q1) The value stored in 0×10000008 on a big-endian machine is 0x65

Part 1 Q2) The value stored in 0×10000008 on a little-endian machine is 0x7F

Part 2: RISC-V Code to Generate 64-bit constant and store in register 10.

lui x10, 0x7FEEE

addi x10, x10, 0xDCC

lui x10, 0xCDBC2

addi x10, x10, 0x365

Part 3: The instruction type is I-Type or I-Format, instruction is ld and the binary representation is as follows

000000000100<mark>11011</mark>011000110000011

Imm

Rs1

Funct3

Rd

Opcode

### **Problem 5: (12 pts)**

Consider the following code sequence and memory state (memory contents are given in hexadecimal. Other values are in decimal).

- a) Assume that the machine is **Big Endian**.
- b) Assume that the machine is Little Endian.

Show the **contents of memory** as well as the value stored in **x5** and **x6** after running this code for both cases. Show the value in **HEX**.

17FD25EC	28
223101BA	24
18926163	20
7E1565A9	16
7701BAC7	12
00011110	8
01BAC789	4
0100FACE	0

#### Memory Address Decimal:

- \*\*\* Assume that byte addressing starts from left to right, i.e., memory byte address 0 corresponds to 01, memory byte address 3 corresponds to CE, memory byte address 4 corresponds to 01, memory byte address 5 corresponds to BA.
- \*\*\* If you have already solved the problem assuming the opposite direction, I will take your solution as correct if it is correct in all other analysis.

## Solution:

addi x2, x0, 14 // x  [Ui x5, 27 // x3:  Sxli x5 x3, 2 // x5:  [b x1 0(x2) // x1=  and x6 x1, x5 // x6:  and x6 x1, x5 // x6:	17 FD 25 EC 28  223101BA 24  1892616320  731565 A9 16  7701BAC712  000111108  01BAC7894  0100 FACE 0  e 5 Big Endian.  2=X0+14=0+14  =(27)2<12=110592  =x3>>2=0x0000006C00  mem [0+14]=0xFFFFFBA  0x0000000000000000000000000000000000
17 FD 25 EC 28  0000 6 C 0 0 24  1892 6 1 6 3 20  7 E1 5 6 5 A 9 16  7 7 0 1 B A C 7 12  00 0 1 1 1 0 8  01 B A C 7 8 9 4  01 0 0 F A C E 0  Little Endian	17FD 25EC 28 00006c00 18926163 20 18926163 20 18926163 20 18926163 20 1001110 8 0100FACE 0

Big Endian
value in register x5 = 006C00000
value in register x6 = 006C00000

Little Endian value in register x5 = 000006C00 value in register x6 = 000006C00

**Problem 6:** (4 pts) Let's explore the value of labels as we discussed in class. You can work on this problem either through your lab or do some deep digging in the resources available and figure this out. For this experiment provide to beq and/or bne labels nearby the instructions executed.

- 1. Implement instruction: you are to implement the program of our slides presentation in slide: 100 and verify the value of the labels. What number do they show? You may load registers with the same value using li pseudo-instruction, which loads a 64-bit binary number directly to the register.
- 2. Explore what is the impact on your compiler's behavior if you type: beq x10, x11 4000. This is larger number supplied by the range of beq.
- 3. Explore what is the impact on your compiler's behavior if you type: beq x10, x11 1001. This is an odd address we feed to beq instruction. What will happen now?

#### Solution:

- 1) The numbers that the labels Exit and Loop show are 12 and -20 respectively.
- 2) A traditional compiler would get an error if the line beq x10, x11 4000 because 4000 is out of range for addressing.
- 3) When typing beq x10, x11 1001 the compiler will once again give an error because beq and its format is only compatible with even numbers. However 1001 could be doubled and then the new address would be 2002 in order to properly work.