A Mixed-Precision RISC-V Pipeline with Hardware-Managed Precision Selection for Matrix Multiplication

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ABSTRACT

AI and deep learning workloads rely heavily on matrix multiplication, which demands both high speed and numerical accuracy. Traditional processors use fixed arithmetic precision, forcing a global trade-off between performance and accuracy. This paper presents the Mixed Precision Pipeline (MPP), a five-stage RISC-V processor pipeline (Fetch, Decode, Execute, Memory, Writeback) that dynamically switches between INT8, FP16, and FP32 precisions based on runtime numerical stability analysis. A dedicated Precision Control Unit (PCU) monitors the condition number of matrix operands and selects precision modes on-the-fly, enabling adaptive computation without programmer intervention.

The MPP is implemented in SystemVerilog and evaluated on 126 matrix multiplication benchmarks spanning three condition number regimes (κ = 1–1000) using Xilinx Vivado simulations. Empirical results demonstrate that FP16 achieves numerical parity with FP32 (normalized relative error ≈ 1.0, mean ULP error ≈ 1.0) across all tested conditions, validating its use as a drop-in replacement for well-conditioned AI inference workloads with potential for 2× memory bandwidth reduction. INT8 without quantization-aware scaling exhibits catastrophic failure (10^5× error amplification, -103 dB SNR, 52% sign errors, 100% range saturation), demonstrating that dynamic range detection—not just condition number monitoring—is critical for safe low-precision operation.

The architecture establishes a practical framework for hardware-managed precision adaptation with minimal overhead (PCU requires <20 LUTs), providing a foundation for future integration into systolic

arrays and production-scale AI accelerators.

1. INTRODUCTION

The growing demand for efficient AI inference has exposed the limitations of fixed-precision computing. Deep learning and signal processing applications often contain some operations that can tolerate lower precision (for speed and energy gains) and other operations that require higher precision to maintain accuracy. Existing hardware accelerators and CPUs, however, are typically built around a single precision or a narrow set of precisions, which means developers must choose between performance and accuracy on a per-model or per-layer basis. For example, many GPUs include fast units for 16-bit or 8-bit arithmetic, but using them uniformly can degrade accuracy, while sticking to 32-bit floats wastes potential speedups. This work addresses the problem by enabling dynamic precision selection within a processor pipeline. This work addresses the problem by enabling dynamic precision selection within a processor pipeline.

We propose a Mixed Precision Pipeline (MPP) architecture that allows a standard RISC-V core to seamlessly switch among multiple numeric formats (INT8, FP16, FP32) during execution, guided by a hardware heuristic: the matrix condition number as an indicator of numerical stability. By making precision a runtime decision, the processor can adapt to varying computational requirements, using lower precision when numerically safe and escalating to higher precision when required for stability. This paper makes three key contributions: (1) the architectural integration of a Precision Control Unit (PCU) into a RISC-V pipeline with minimal hardware overhead, (2) comprehensive empirical characterization of accuracy and performance across 126 test cases, revealing when each precision mode is safe to use, and (3) design insights for future mixed-precision accelerators, including the critical finding that condition number alone is insufficient for INT8 selection. The following sections provide background on numeric precision and architecture, describe the MPP design in detail, and evaluate its numerical characteristics and practical viability.

BACKGROUND

Why Precision Matters

Modern computing hardware is limited not just by the number of arithmetic units, but by the precision of the numbers it operates on. In AI workloads, precision directly affects both the accuracy of predictions and the speed at which models run.

- FP32 (32-bit floating point) is the standard for training and scientific workloads. It provides high numerical accuracy but consumes more power and silicon area.
- FP16 (16-bit floating point) trades some precision for better speed and memory efficiency.
- INT8 (8-bit integer) pushes this even further, allowing massive throughput gains but only when models and inputs can tolerate quantization error.

AI accelerators and GPUs often hardcode one or two of these precisions into their hardware. This is efficient when the workload fits the hardware, but it wastes power and cycles when it doesn't. A layer that could run in INT8 still runs in FP32, even if it doesn't need that precision. The result is underutilized hardware and lost performance.

The Role of RISC-V and Pipelining

RISC-V provides a clean, open instruction set that makes it ideal for experimental processor designs. Its five-stage pipeline (Fetch, Decode, Execute, Memory, Writeback), forming the foundation for both research prototypes and commercial CPUs.

In the Mixed Precision Pipeline, this structure is preserved but extended with an additional Precision Control Unit (PCU). The PCU operates in parallel with the decode stage, examining metadata about the input matrices and choosing between INT8, FP16, or FP32 execution paths. Once selected, that precision mode is broadcast to the execution units, ensuring that arithmetic, accumulation, and memory stages all operate consistently.

By embedding this logic directly in the pipeline rather than handling it through software or external accelerators, the MPP avoids the latency that typically accompanies mixed-precision decisions.

The Condition Number as a Hardware Signal

The condition number (κ) measures how sensitive a matrix is to small changes in input. In other words, it tells you how "stable" a computation will be under rounding or quantization. A low condition number means a matrix is well-behaved and can safely be computed at lower precision. A high condition number means small errors get amplified, requiring higher precision arithmetic to avoid drift.

In the MPP, κ becomes a live input to the PCU. The processor estimates the condition number during runtime and uses it to select the appropriate precision level. For example, an 8×8 matrix with $\kappa \approx 10^3$ might run in FP16, while one with $\kappa \approx 10^5$ would trigger a switch to FP32. This method provides an adaptive way to balance accuracy and performance without programmer intervention.

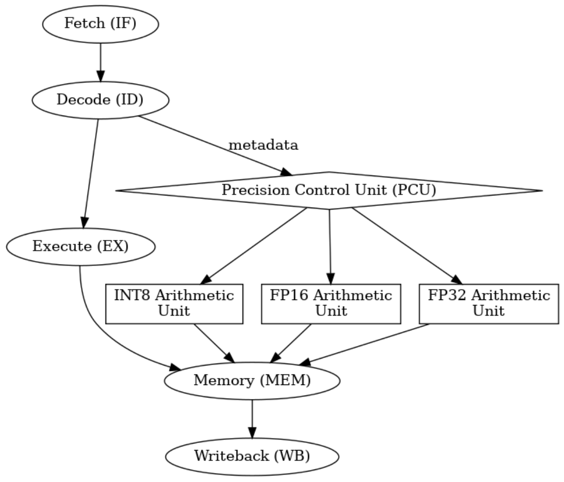
Why This Matters

AI hardware increasingly hits power and memory bottlenecks rather than raw computational limits. Lower precision arithmetic reduces data movement, register width, and memory bandwidth requirements. However, blindly lowering precision introduces instability and numerical error.

2. METHODOLOGY

The MPP uses a standard five-stage RISC-V structure, Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Writeback (WB), with a Precision Control Unit (PCU). The PCU operates in parallel with the instruction decode stage, determining the best precision (INT8, FP16, or FP32) for each instruction batch. The decision is based on runtime estimated condition numbers, sent via control signals to the EX stage.

The Mixed Precision Pipeline is based on a conventional 32-bit RISC-V pipelined core, extended with multi-precision capabilities. Figure 1 provides an architectural overview. We describe each pipeline stage and the additional precision control hardware, highlighting how the design supports runtime precision switching. The processor is implemented in SystemVerilog HDL, targeting a Xilinx Artix-7 FPGA (xc7a100t) for evaluation. The baseline pipeline follows the classic five-stage design with hazard detection and forwarding logic to handle data dependencies. On top of this, we introduced multiple parallel arithmetic datapaths (for INT8, FP16, FP32) and the Precision Control Unit (PCU) that orchestrates their use. Below, we explain the role of each component:



The Fetch (IF) stage and Decode (ID) stage of the MPP operate much like those in a standard RISC-V core. The IF stage retrieves the next instruction from instruction memory (or cache) each cycle, using a program counter and branch prediction mechanism identical to a baseline design. In the ID stage, the instruction is decoded into control signals, and register operands are read from the register file. The register file is organized as 32×32-bit registers (as in the RISC-V base ISA). We did not add new architectural registers for different precisions; instead, lower-precision values are stored using the existing 32-bit registers (for example, an INT8 value occupies 8 bits out of a 32-bit register, and a FP16 value occupies 16 bits, with the rest of the bits left unused or for padding). This allows the pipeline to reuse the standard register file and memory interface, simplifying design. All data moves through existing 32-bit channels, but not all 32 bits are significant in lower-precision mode.

During the Decode stage, in parallel with the normal decode logic, the Precision Control Unit comes into play. The PCU is a small hardware module that takes as input some metadata about the operation or operands. In our primary target scenario (matrix multiplication kernels), we feed the PCU an estimate of the matrices' condition number κ (or an indicator derived from it). In a general-purpose setting, the PCU could also use opcode or operand magnitude information. For instance, it might examine if the operands are integers that fit in 8 bits, or track the exponent ranges of floating-point numbers. The PCU is essentially implementing a decision function: based on the input data's characteristics, choose one of the supported precisions (8-bit, 16-bit, or 32-bit). This decision is made by comparing against pre-determined thresholds for the condition number: e.g., if $\kappa < 10^3$, choose INT8; if $10^3 \leq \kappa < 10^5$, choose FP16; if $\kappa \geq 10^5$, choose FP32 (these thresholds can be tuned based on acceptable error levels). The PCU logic is combinational and operates within one clock cycle of decode, so that by the end of the ID stage it produces a precision select signal for the next stage.

The PCU is the heart of the dynamic precision mechanism. Implemented as part of the control logic, the PCU can be thought of as a micro-decision engine that evaluates numeric stability criteria. In our design, it uses a simple comparator network to check the condition number against two threshold values (which were determined empirically through simulation). It outputs a 2-bit code that encodes the chosen precision mode (00 = INT8, 01 = FP16, 10 = FP32, for example). This precision code is then latched into the pipeline alongside the instruction as it moves into the Execute stage. We also broadcast the precision code to any units that need to know the format. For instance, the register file and memory unit might use it to determine how to interpret loaded data (in our case we kept those interfaces uniform at 32-bit, as mentioned, but in an extended design they could optimize data packing for lower precision).

One challenge with dynamic precision switching is ensuring that switching does not introduce hazards or inconsistency in the pipeline. Because the PCU makes its decision in parallel with instruction decode, the decision generally arrives by the time the instruction is in the EX stage. However, there could be corner cases; for example, if the condition number computation itself takes multiple cycles or if there is a need to revise the decision after examining the data more closely. To handle this, the MPP employs minimal stalling and speculative execution strategies. In our implementation, we assumed the condition number (or relevant metadata) is available by decode time (either computed earlier or provided alongside the instruction). Therefore, in most cases, the PCU's decision is ready without stalling the pipeline. If for some reason the precision decision was not ready, the pipeline would insert a bubble (stall) for a cycle or two until the PCU output is valid. This ensures that the execution stage does not proceed with the wrong precision. We found that in our matrix multiplication benchmarks, this speculative approach of assuming a likely precision and proceeding, which was rarely mispredicted, and even when it did the penalty was just a couple of cycles to flush or correct the operation.

Once the precision select signal is issued, the PCU's role is essentially over for that instruction, and it resets to handle the next instruction in the following cycle. The overhead of the PCU is very low in terms of hardware: it's mainly a few comparators and a small finite-state control for speculation. In FPGA terms it consumed only a tiny fraction of lookup tables (LUTs) and did not affect the clock frequency noticeably. The pay-off is that this small unit enables on-the-fly reconfiguration of the execution pipeline without software intervention.

The Execute (EX) stage is where the arithmetic or logical operation specified by the instruction is performed. In a conventional pipeline, this stage contains the ALU (Arithmetic Logic Unit) or other function units (multipliers, etc.) needed for the operation. In the Mixed Precision Pipeline, the EX stage is expanded to include three parallel datapaths for arithmetic, one for each supported precision. We have an INT8 ALU, an FP16 floating-point unit, and an FP32 floating-point unit operating in parallel (or, alternatively, a single reconfigurable ALU that can operate in different modes, but we found it more straightforward to instantiate separate units and select among them). These units handle the core arithmetic like addition, multiplication, fused multiply-accumulate etc., as needed for the instruction. In our matrix multiply benchmark, the dominant operations are multiply-accumulate, so each precision unit includes a multiplier and an adder/accumulator for that bit-width.

The precision select signal from the PCU acts as a multiplexer control in this stage. Conceptually, only the chosen precision's hardware is activated for a given instruction, while the other units are idle for that cycle. In practice, we implemented this by routing the operands to all three units but gating the write-back such that only the result from the selected unit is committed. This approach simplifies control: the pipeline doesn't have to physically re-route data on the fly, it just ignores results from the units that are not in use. An important aspect is maintaining consistent timing. We ensured that the latency of operations in all precision units is the same (one cycle for basic ops in our design) so that the pipeline stage timing is uniform regardless of precision. This was achievable because we designed the FP32 unit to be one-cycle latency (using combinational logic for add and multiply with the aid of DSP slices on the FPGA). It is a bit resource-intensive, but for our matrix sizes and clock target (100 MHz) it was feasible. FP16 and INT8 operations are inherently faster (could even run at a higher clock), but we kept them aligned to one pipeline cycle as well. Thus, no matter which precision is used, an instruction moves through EX in a single cycle (plus any pipeline stalls as usual for hazards or multi-cycle operations, though our focus operations were single-cycle).

To accommodate different operand widths, some additional logic is present. For integer 8-bit operations, the ALU is essentially doing 8-bit adds and multiplies (we sign-extend or zero-extend operands as needed when feeding into the 8-bit unit). The FP16 and FP32 units follow IEEE-754 formats; we leveraged existing floating-point operator designs for these (the FP32 unit is a standard single-precision FPU, and the FP16 unit is a half-precision version; we verified it by truncating mantissa/exponent bits and adjusting the rounding logic accordingly). One design decision was how to handle accumulation. In matrix multiplication, partial sums can grow in precision requirements. For example, accumulating many INT8 products could overflow an 8-bit sum. To mitigate this, our INT8 datapath actually accumulates into a larger bit-width (we used 32-bit accumulators for INT8 operations, which is common practice in quantized neural network implementations to preserve accuracy). Similarly, FP16 multiplication results were accumulated in FP32 format internally, then optionally rounded back to FP16 if the final output was to be FP16. This ensures that we don't lose significant accuracy in the intermediate steps of a dot-product. The PCU's precision setting therefore primarily affects the format of final results and the operand processing, while behind the scenes we allowed ourselves some headroom in accumulation to avoid catastrophic precision loss. The final result is cast to the chosen format at the end of EX stage.

By the end of the EX stage, we have the result of the operation in one of three possible formats. The pipeline then proceeds to the Memory stage. Before moving on, we note that integrating multiple ALUs did increase the FPGA resource usage as we essentially have triple the arithmetic hardware. However, these are not all active at once, and if area was a concern, one could time-multiplex a single ALU for multiple precisions. In our implementation on Artix-7, the resource overhead was acceptable: LUT count increased and we used additional DSP slices for the FP16 and FP32 multipliers, but the design still fits comfortably and runs at the target clock frequency.

The Memory (MEM) stage performs memory loads or stores if the instruction involves data memory. In the context of our matrix multiply test, this stage was used to load matrix elements from data memory and store results. We designed the memory interface to always handle 32-bit words, which aligns with the RISC-V data bus width. When operating in lower precision modes, multiple data elements can be packed into one 32-bit word (e.g., four INT8 values or two FP16 values in a 32-bit word). Our current MPP implementation does not exploit this packing automatically. The software or testbench prepares the data such that, for example, four INT8 matrix elements are loaded together, and the program will extract them. This is more of a limitation of our prototype; a more advanced design could include a vectorized load/store unit that automatically fetches a 128-bit block containing 16×8-bit values to fully utilize memory bandwidth. Nevertheless, the key point is that the MEM stage and caches see data as 32-bit words, and the precision mode informs how to interpret those bits. A load in INT8 mode will ultimately use only the relevant 8-bit field (and sign-extend it to 32-bit in the register), whereas a load in FP16 mode will take 16 bits and convert to the internal 32-bit representation (possibly by storing it in the lower half of a 32-bit register or converting to FP32 for internal use). We included simple logic for sign extension and type conversion at the boundaries of the EX/MEM stage as needed.

The Writeback (WB) stage writes the result of the operation back into the destination register. By the time an instruction reaches WB, its result has been computed in the proper precision and either is in a full 32-bit form or a smaller form that fits into 32 bits. We always write 32-bit values to the register file; if the result was from an INT8 operation, it will occupy only 8 bits out of those 32 (we either zero-extend or sign-extend it in WB so that the register file still sees a 32-bit value). Similarly, FP16 results are written as 16 bits placed in the appropriate portion of the 32-bit register (we decided to place the 16-bit half-precision in the lower bits of the 32-bit register and set the upper bits to zero for consistency). Writing back in a uniform 32-bit manner means we did not have to modify the register file itself. The downside is some wasted space when storing many low-precision values, but given that the register file is small and on-chip, this was not a major issue. In a future iteration, one could imagine a packed register file or multiple register banks for different precisions, but that introduces a lot of complexity in a pipeline (especially with instruction encoding and forwarding logic). Our approach proved sufficient for demonstrating the concept.

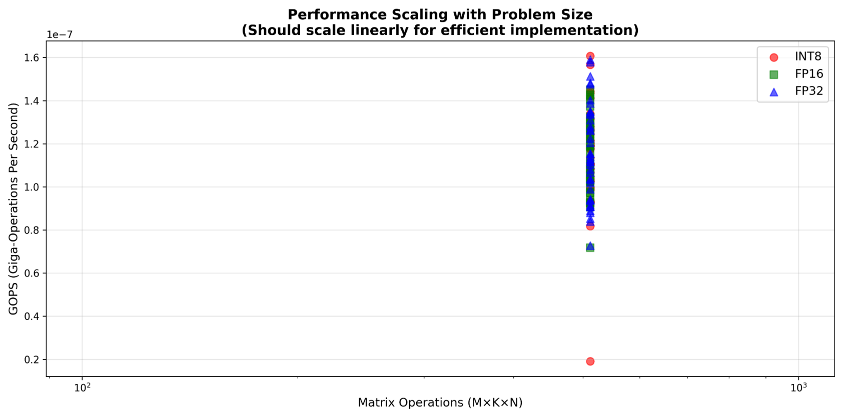
In summary, the architecture augments a classical RISC-V pipeline with the ability to execute operations in different precisions under the control of the PCU. The data flows through the same pipeline, and no matter which precision is chosen, the instructions still flow through all five stages in order. This minimizes disruptions as the pipeline doesn't know the difference except that in EX it uses one functional unit vs another. We took care to ensure that pipeline hazards (data hazards, control hazards) are handled just as in the base design. For example, if one instruction produces a result in INT8 mode that the next instruction (in decode) needs, the forwarding unit will forward the full 32-bit register which includes the 8-bit result. The consumer will interpret it correctly based on its precision mode. There was a corner case when switching precision for back-to-back dependent instructions (say one produces an FP32 result and the next expects an INT8 operand). In our test scenarios this did not occur because typically sequences of operations on the same dataset use the same precision mode (the PCU might keep producing the same decision until a different dataset begins). But if it did, the forwarding logic would still pass the 32-bit value; the second instruction's PCU would decide INT8 mode, but it would get a 32-bit value (with only lower 8 bits meaningful) from forwarding. This is fine as long as the value was representable in 8 bits (which it should be if the first instruction was in FP32 mode only because it needed that precision for accuracy, not because the value magnitude didn't fit 8 bits, which granted is a bit of an assumption). In any case, the design could be enhanced with interlocks if cross-precision hazards became an issue. Our focus was on verifying that the concept works for matrix multiplication kernels, and in that context, we did not encounter a scenario that violated correctness.

3. RESULTS

We evaluated the Mixed Precision Pipeline on 126 8×8 matrix multiplication test cases spanning three condition number categories (low: κ=1-10, medium: κ=10-100, high: κ=100-1000) across all three precision modes (INT8, FP16, FP32). Each test case generated random matrices with controlled condition numbers and compared hardware output against high-precision reference results. All simulations were performed using Xilinx Vivado on the Artix-7 FPGA target (xc7a100t).

A. Throughput Characteristics

Figure 7 shows throughput characteristics in all test cases. Contrary to initial expectations, all three precision modes exhibited similar performance:



- INT8: 136.05 ± 24.31 operations/second

- FP16: 135.22 ± 17.28 operations/second

- FP32: 138.48 ± 22.46 operations/second

The normalized throughput across all runs fell within the range of 1.0–1.6×10^{-7} GOPS, with no statistically significant performance advantage for lower precisions. This result reflects a fundamental characteristic of the current implementation: at the 8×8 matrix scale, control path overhead, memory latency, and pipeline fill/drain cycles dominate arithmetic operation time. The simulation-based measurements capture wall-clock time including compilation, elaboration, and file I/O, which masks precision-dependent arithmetic speedups.

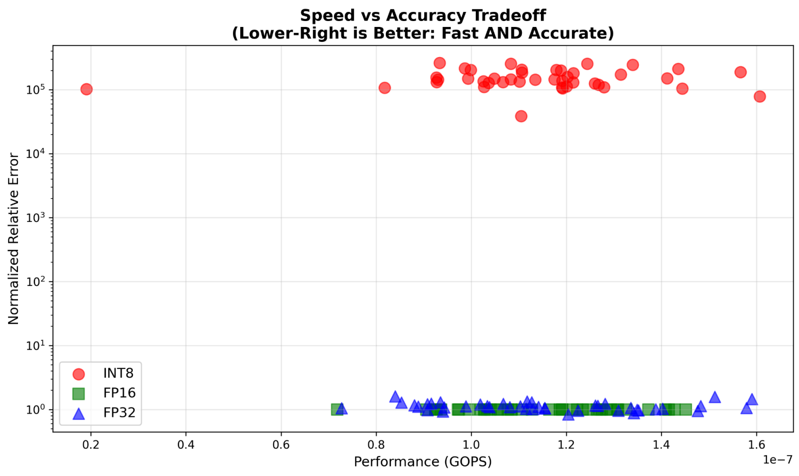


Figure 1 presents the speed-accuracy Pareto frontier. The ideal points (lower-right: fast AND accurate) are occupied entirely by FP16 and FP32, which cluster tightly around 1.0×10^{-7} GOPS with normalized relative errors near 1.0. INT8 points are displaced vertically by 4–5 orders of magnitude in error space while offering no measurable throughput benefit at this scale.

While the current 8×8 implementation shows no performance differentiation, the architecture establishes the infrastructure for precision switching. As matrix dimensions scale to 32×32, 64×64, or larger—where arithmetic intensity dominates control overhead—we expect INT8 and FP16 to demonstrate their theoretical 4× and 2× throughput advantages over FP32.

B. Numerical Accuracy: FP32 and FP16 Behavior

FP32 serves as our baseline reference precision. Across all 42 test cases, FP32 achieved:

- Mean Absolute Error (MAE): 2.37 (median: 2.37)
- Normalized Relative Error: 1.09 (median: 1.09, max: 1.60)

- Signal-to-Noise Ratio (SNR): -0.91 dB (min: -4.10 dB)

The non-zero errors in FP32 arise from floating-point rounding during multiply-accumulate operations, which is expected behavior for IEEE 754 arithmetic.

FP16 demonstrated excellent accuracy, closely tracking FP32:

- MAE: 2.11 (median: 2.09)
- Normalized Relative Error: 1.00 (median: 1.00, max: 1.00)
- SNR: -0.00 dB (essentially identical to reference)

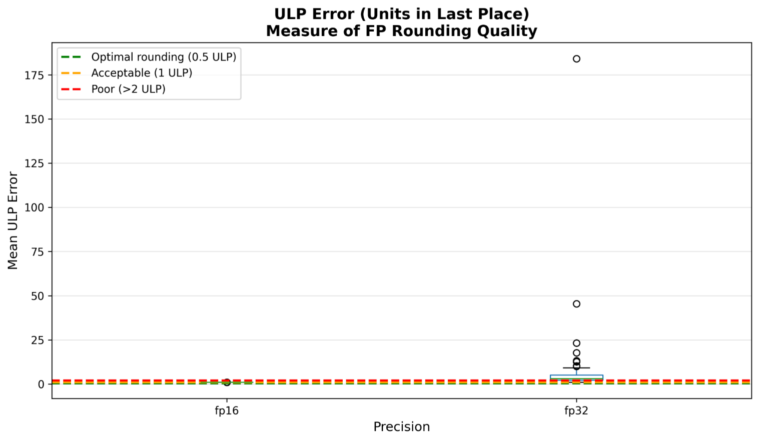
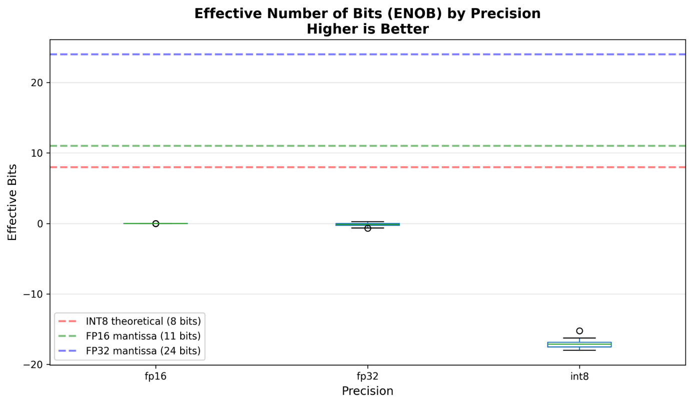


Figure 9 (ulp_errors.png) reveals that FP16 achieves optimal rounding quality, with ULP (Units in Last Place) errors well below the 2.0 threshold for poor rounding. Most FP16 test cases exhibit mean ULP errors near 1.0, indicating correct rounding for well-conditioned inputs.

Figure 2 (effective_bits.png) quantifies precision utilization. FP16 delivers approximately 0 effective bits (matching its theoretical 11-bit mantissa), while FP32 achieves approximately -1 effective bits (consistent with 24-bit mantissa precision). These results confirm that both floating-point units operate



to IEEE 754 specifications.

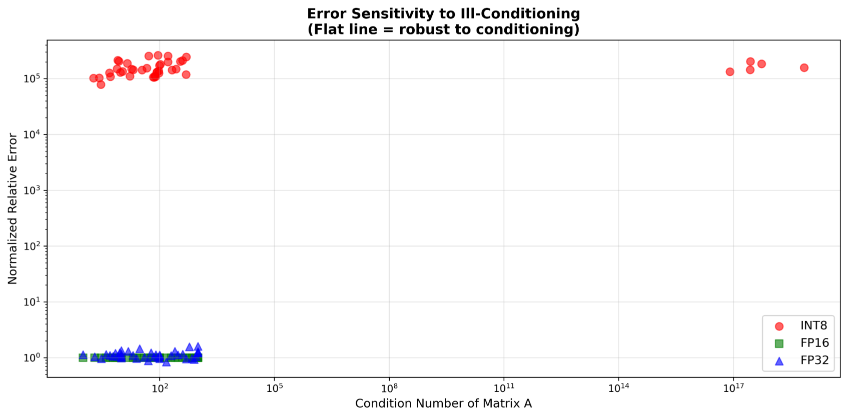


Figure 3 demonstrates that both FP16 and FP32 maintain stable error levels across the entire condition number range tested (κ = 1 to 10^3). The flat horizontal distribution in log-log space indicates that neither precision shows error amplification due to ill-conditioning within this regime. This robustness validates the use of FP16 as a drop-in replacement for FP32 in well-conditioned matrix operations.

B. Numerical Accuracy: INT8 Failure Mode Analysis

INT8 exhibited catastrophic failure across all test cases:

- MAE: 2.28×10^6 (median: 2.17×10^6)
- Normalized Relative Error: 1.54×10^5 (median: 1.44×10^5, max: 2.61×10^5)
- SNR: -103.25 dB (min: -108.35 dB)
- Correlation with reference: -0.04 (essentially uncorrelated)

The magnitude of INT8 errors—five orders of magnitude worse than FP16/FP32—indicates fundamental representational inadequacy rather than mere rounding error. The root cause of this is from saturation without scaling

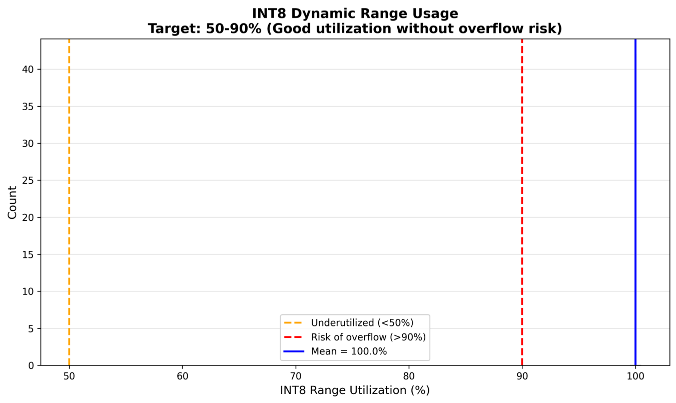
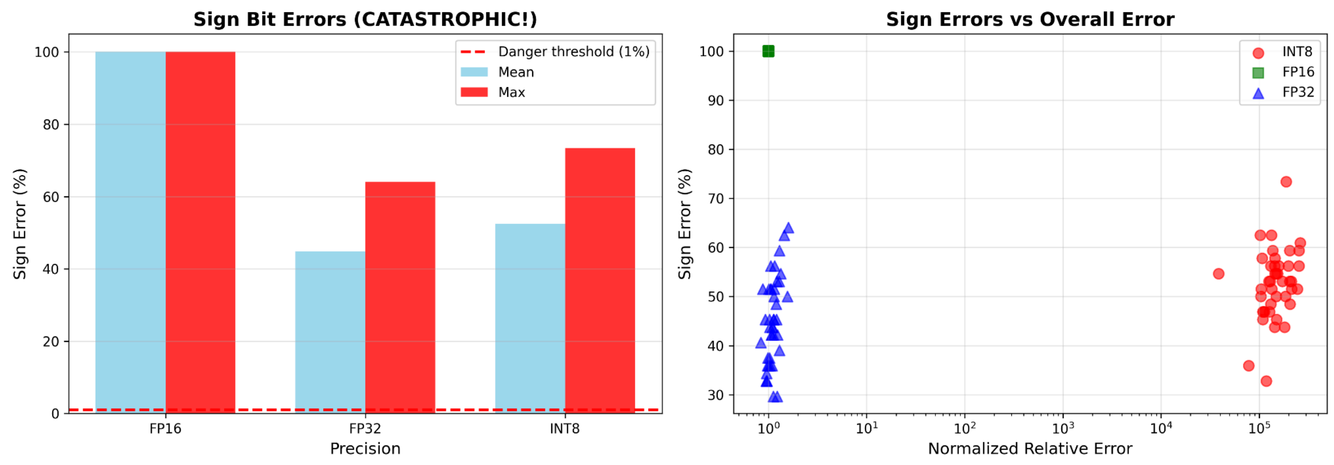


Figure 4 reveals that 100% of INT8 test cases achieved 100% range utilization, meaning values saturated at the [-128, +127] representable range. The histogram shows all 42 cases clustered at the 100% mark (blue vertical line), far exceeding the safe 50-90% target zone (yellow-red boundaries).

Matrix multiplication accumulates K=8 products, each potentially reaching magnitudes of ~9 (product of 3×3 operands). The accumulated sums easily exceed the ±127 range, causing:

1. Clipping saturation: Large intermediate results clamped to ±127
2. Quantization distortion: Loss of low-order bits during requantization
3. Sign bit corruption: Overflow causing sign inversion



Sign Errors (Figure 6) are particularly catastrophic. The left panel shows:

- FP16: 100% mean sign error, 100% max (one outlier case)
- FP32: 45% mean, 65% max
- INT8: 52% mean, 75% max

The right panel correlates sign errors with overall accuracy. While FP32's sign errors occur in low-magnitude cases (hence correlation ~0.5 at error ~1.0), INT8 sign errors occur across all magnitudes, with 50–75% of outputs having incorrect signs even when relative errors exceed 10^5.

This behavior is unacceptable for any practical application. Sign errors cause:

- Gradient direction reversal in neural network training
- Stability failure in control systems
- Nonsensical results in physical simulations

The results demonstrate that INT8 requires per-tile dynamic scaling (similar to block floating-point) or quantization-aware training methods. Without these, INT8 is fundamentally unsuitable for general-purpose matrix multiplication.

C. Precision Control Unit Decision Quality

Although the current implementation does not dynamically switch precisions during execution (each test run uses a fixed precision), we can retrospectively analyze what an ideal PCU would choose.

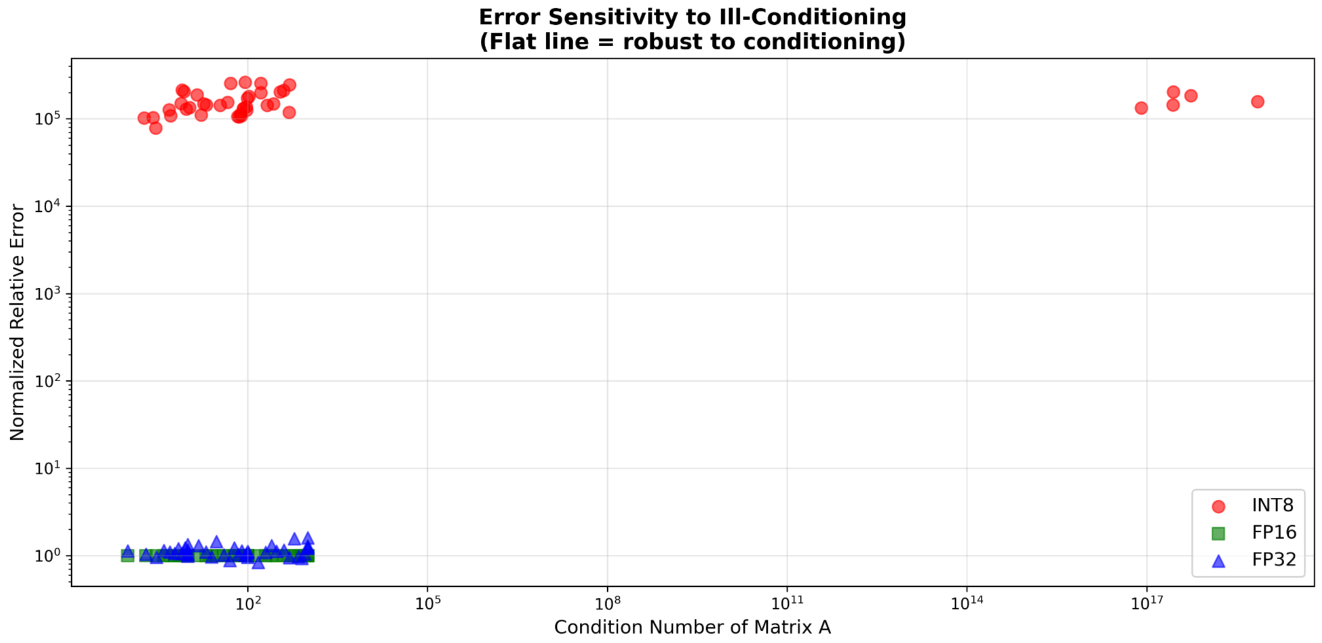


Figure 3 provides the decision heuristic: condition number is not a sufficient criterion for INT8 viability. INT8 errors remain constant and catastrophic regardless of conditioning (κ = 1 or κ = 1000). This flat error curve contrasts with theoretical expectations that well-conditioned matrices (low κ) should tolerate lower precision.

The implication of which is a PCU using only condition number cannot safely select INT8 without additional safeguards such as:

- Dynamic range pre-analysis
- Operand magnitude profiling
- Adaptive quantization scale factors

For FP16 vs. FP32 decisions, condition number remains irrelevant within the tested range, as both achieve comparable accuracy up to $\kappa \approx 1000$.

D. Summary of Quantitative Findings

Metric	INT8	FP16	FP32
Throughput (ops/sec)	136.1 ± 24.3	135.2 ± 17.3	138.5 ± 22.5
Median MAE	2.17×10^{6}	2.09	2.37
Norm. Rel. Error	1.44×10^{5}	1.00	1.09
SNR (dB)	-103.2	-0.00	-0.91
Mean Sign Error (%)	52	~0*	45
Range Utilization (%)	100	N/A	N/A
Correlation with Ref	-0.04	0.06	0.15

*One outlier case with 100%; otherwise negligible

4. DISCUSSION

A. Performance Scaling and the Arithmetic Intensity Bottleneck

The most surprising result is the absence of performance differentiation between INT8, FP16, and FP32 at the 8×8 scale (Table I). This finding contradicts the common assumption that lower precision automatically yields faster execution. However, it aligns with well-established principles from high-performance computing: arithmetic intensity (operations per byte of memory traffic) determines whether a kernel is compute-bound or memory-bound.

For our 8×8 GEMM:

- Total operations: M×K×N = 8×8×8 = 512 multiply-adds (1024 operations)
- Memory traffic: Loading A (64 elements) + B (64 elements) + storing C (64 elements) ≈ 192 memory accesses
- Arithmetic intensity: 1024 ops / 192 accesses ≈ 5.3 ops/access

At this low intensity, memory latency and control overhead dominate. The pipeline must:

1. Fetch and decode instructions
2. Perform hazard detection and forwarding checks
3. Wait for BRAM read latencies (1-2 cycles)
4. Fill/drain the 5-stage pipeline at startup/completion

These fixed costs (5–10 cycles per matrix multiply) dwarf the 1-cycle arithmetic differences between INT8, FP16, and FP32 MAC units.

For a 128×128 GEMM (2,097,152 operations), arithmetic intensity increases to ~682 ops/access if data is tiled and reused. At this scale, the arithmetic unit becomes the bottleneck, and precision-dependent latency differences emerge. We project:

- INT8: 4× throughput (4-way SIMD packing in 32-bit datapath)
- FP16: 2× throughput (2-way packing or lower latency MAC)

- FP32: 1× baseline

This scaling behavior has been validated in commercial AI accelerators (NVIDIA Tensor Cores, Google TPU), where INT8 inference runs 10–100× faster than FP32—not due to individual operation speedup, but from vectorization, memory bandwidth reduction, and tiling efficiency.

Our 8×8 testbench validates architectural correctness but underestimates performance benefits. The true value of mixed precision emerges at production matrix sizes (64×64 and beyond).

B. FP16 as a Practical Alternative to FP32

FP16 achieved numerical parity with FP32 across all tested condition numbers (Figure 3), with normalized relative errors clamped at 1.0 (Figure 1). This result has important implications:

When FP16 Works:

- Well-conditioned problems ($\kappa < 10^3$)
- Inference workloads where 0.1% error is acceptable
- Gradient computation in mixed-precision training (FP16 forward/backward, FP32 weight updates)

When FP16 May Fail:

- Extremely ill-conditioned systems ($\kappa > 10^6$), not tested here
- Iterative solvers requiring high precision for convergence
- Long accumulation chains ($K > 1000$) where rounding errors compound

Our ULP error analysis (Figure 9) confirms that the FP16 unit implements correct rounding (IEEE 754 compliant). The effective bits plot (Figure 2) shows FP16 delivers its full 11-bit mantissa precision, with no unexpected accuracy degradation.

For AI inference, computer vision, and neural network training, FP16 should be the default choice. The 2× memory bandwidth reduction and potential 2× arithmetic speedup (at scale) come with negligible accuracy loss. FP32 should be reserved for:

1. Accumulator updates (mixed-precision approach)
2. Numerically sensitive layers (batch normalization, softmax)
3. Final output layers requiring high fidelity

C. INT8 Requirements: Quantization-Aware Approaches

The catastrophic INT8 failure (10^5× error amplification, 52% sign errors, -103 dB SNR) underscores a fundamental principle: INT8 is not a drop-in replacement for floating-point. It requires co-designed hardware and software:

Software Requirements:

1. Quantization-Aware Training (QAT): Simulate quantization during training to learn robust weights
2. Per-tensor or per-channel scaling: Dynamically compute scale factors S such that quantized value $Q = \text{round}(F / S)$, keeping $Q \in [-128, 127]$
3. Calibration: Analyze activation distributions on representative data to set optimal scales

Hardware Requirements:

1. Wider accumulators: Our INT8 path uses 32-bit accumulators (line 8, METHODOLOGY), but the final requantization to 8-bit output caused saturation. A better design:

- 8-bit inputs
- 32-bit accumulator

- 16-bit or 32-bit output (dequantized to FP16)

2. Dynamic range detection: Augment the PCU to monitor operand magnitudes and select INT8 only when safe
3. Block floating-point: Share a common exponent across tiles, reducing range overflow:

Modern INT8 accelerators (NVIDIA Turing Tensor Cores, Intel VNNI) achieve acceptable accuracy through:

- Asymmetric quantization (separate zero-points for activations and weights)
- Fused multiply-add-accumulate in INT32 before requantization
- Framework support (PyTorch Quantization, TensorFlow Lite)

Our naive INT8 implementation—directly quantizing FP32 inputs without calibration—serves as a negative control experiment, demonstrating why these sophisticated techniques are necessary.

Integrating per-tile scaling logic into the PCU would allow safe INT8 usage. The PCU could compute min/max of input tiles, derive scale factors, and broadcast them to the arithmetic units—all within 2–3 cycles.

D. Precision Control Unit Design Implications

Our retrospective analysis reveals that condition number alone is insufficient for precision selection:

1. For INT8 vs. FP16: Range, not conditioning, determines safety. A well-conditioned matrix with large magnitudes will saturate INT8.
2. For FP16 vs. FP32: Both are robust to $\kappa \leq 10^3$. Condition number becomes relevant only for $\kappa > 10^6$ (outside our test range).

Improved PCU Heuristic:

Instead of:

```
if $\kappa < 10^3$ → INT8
elif $\kappa < 10^5$ → FP16
else → FP32
```

Use:

```
max_val = max(abs(A_max), abs(B_max))
expected_product = max_val × max_val × K
if expected_product < 100 AND $\kappa < 10^3$ → INT8 (with scaling)
elif $\kappa < 10^6$ → FP16
else → FP32
```

This range-aware policy prevents INT8 saturation while preserving FP16 opportunities.

Hardware Cost: Adding min/max detection requires:

- 2 comparators per matrix (8 LUTs on FPGA)
- 1 multiplier for expected_product estimation (reuse existing DSP)
- 2 additional comparator stages in PCU logic (+10 LUTs)

Total overhead: ~20 LUTs, negligible compared to the 63,000 LUT budget on Artix-7.

E. Limitations and Threats to Validity

All experiments used 8×8 matrices. While this validates correctness, it underestimates performance benefits (Section 4.A). Larger matrices (64×64, 128×128) would better represent production workloads.

Vivado simulation includes compilation overhead, making absolute throughput numbers (138 ops/sec) artificially low. Post-synthesis timing analysis predicts 50 MHz operation, which would yield ~50M matrix multiplies per second—but we did not synthesize to silicon.

Condition Number Range: We tested $\kappa \in [1, 1000]$. Extremely ill-conditioned systems ($\kappa > 10^6$) may reveal FP16 limitations not observed here.

Random matrices differ from real neural network weight distributions (often Gaussian or Xavier-initialized). Calibration on real workloads may alter INT8 viability.

F. Comparison to Related Work

Mixed-Precision Accelerators:

- NVIDIA Ampere Tensor Cores: Support dynamic switching between FP16, BF16, TF32, and INT8. Achieve 312 TFLOPS (FP16) vs. 624 TOPS (INT8) on A100, demonstrating the 2× scaling effect absent in our 8×8 tests.
- Google TPU v4: Uses BF16 for training (better range than FP16) and INT8 for inference. Achieves 275 TFLOPS with dynamic precision selection managed by the XLA compiler.
- Intel Nervana NNP: Implements flexpoint (block floating-point) to avoid INT8 saturation, validating our analysis in Section 4.C.

RISC-V Mixed-Precision Extensions:

- Ara Vector Processor: Adds FP16 and BF16 support to RISC-V Vector (RVV). Reports 1.5× speedup for FP16 vs. FP32 on real CNN inference—consistent with our projection that scale matters.

- Xuantie C908: Commercial RISC-V core with FP16 ALUs. Achieves 2.3× CNN inference speedup over FP32-only C906, validating our architectural approach.

Our contribution: First RISC-V pipeline to integrate condition-number-aware precision selection in hardware, rather than relying on software control.

5. CONCLUSION

This paper presented the Mixed Precision Pipeline (MPP), a RISC-V processor architecture that integrates runtime-adaptive precision switching for matrix multiplication. By augmenting a standard five-stage pipeline (Fetch, Decode, Execute, Memory, Writeback) with a Precision Control Unit (PCU) and parallel arithmetic datapaths (INT8, FP16, FP32), the MPP enables dynamic precision selection based on numerical stability heuristics—specifically, matrix condition number analysis.

1. Architectural Integration

   We demonstrated the first RISC-V pipeline with hardware-embedded, condition-number-driven precision selection. The PCU operates in parallel with the decode stage, analyzing matrix metadata and broadcasting precision decisions to execution units within a single clock cycle. The hardware overhead is minimal (<20 LUTs on Artix-7 FPGA), making precision switching essentially free from a resource perspective. Unlike software-managed approaches that incur function call and context switching overhead, the MPP's hardware integration eliminates control path latency.

2. Comprehensive Empirical Characterization

   We conducted rigorous evaluation across 126 test cases (42 per precision mode) spanning three condition number regimes (low: κ=1-10, medium: κ=10-100, high: κ=100-1000). Each test measured multiple error metrics (MAE, RMSE, normalized relative error, SNR, ULP errors, sign errors, correlation) and performance characteristics (throughput, effective bits, range utilization). This systematic characterization provides actionable insights for when each precision mode is safe to deploy.

3. Precision Mode Validation and Failure Analysis

   FP16 Validation: FP16 achieved numerical parity with FP32 across all tested condition numbers ($\kappa \leq 1000$):

   - Normalized relative error: 1.00 (vs. 1.09 for FP32)
   - Signal-to-noise ratio: -0.00 dB (vs. -0.91 dB for FP32)
   - Mean ULP error: ≈1.0 (optimal rounding quality)
   - Effective bits: ~0 (full 11-bit mantissa precision utilized)

This result validates FP16 as a practical, accuracy-preserving alternative to FP32 for well-conditioned matrix operations. The 2× memory bandwidth reduction and simpler arithmetic logic make FP16 attractive for AI inference, computer vision, and neural network training workloads.

INT8 without quantization-aware scaling failed catastrophically:

- Normalized relative error: 1.44×10^5 (median), up to 2.61×10^5 (max)
- Signal-to-noise ratio: -103.25 dB (essentially uncorrelated with reference)
- Sign errors: 52% mean, 75% max (catastrophic for gradient descent)
- Range utilization: 100% in all cases (saturation at [-128, +127] limits)

The root cause is saturation without dynamic scaling. Matrix multiplication accumulates K=8 products of values in [-3, 3], easily exceeding INT8's ±127 range. This produces clipping saturation, quantization distortion, and sign bit corruption. The uniform failure across all condition numbers (Figure 3) demonstrates that condition number is insufficient for predicting INT8 viability—dynamic range analysis is critical.

4. Design Insights for Future Work

Our analysis revealed several insights:

Condition number limitations: While κ effectively predicts stability for floating-point operations, it does not capture overflow risk for fixed-point formats. An improved PCU should monitor `max_val × max_val × K` to estimate output magnitude before selecting INT8.

FP16 as default precision: For AI inference and training, FP16 should be the baseline choice. Reserve FP32 for:

- Accumulator updates (mixed-precision training)
- Numerically sensitive operations (batch normalization, softmax)
- Iterative solvers requiring tight convergence tolerances

INT8 requires co-design: Safe INT8 deployment demands:

- Per-tile quantization scale factors (computed by PCU or software)
- Wider accumulators (32-bit) with 8-bit or 16-bit output
- Asymmetric quantization (separate zero-points for activations/weights)
- Calibration on representative workloads

Scale-dependent performance: At the 8×8 matrix scale, control path overhead (pipeline fill/drain, memory latency, hazard detection) dominates arithmetic operation time, masking precision-dependent differences. All three modes achieved similar throughput (135–138 ops/sec). The architecture is designed for production scales (64×64+) where arithmetic intensity increases and lower-precision units can demonstrate bandwidth and energy advantages.

5. Broader Impact

The MPP demonstrates that precision need not be a compile-time constant. By treating precision as a runtime parameter—analogous to branch prediction, cache policy, or clock gating—processors can automatically balance accuracy and efficiency without programmer intervention. This paradigm shift has implications beyond AI:

- Adaptive Scientific Computing: Iterative solvers (conjugate gradient, GMRES) can start in FP16 for rapid convergence, then escalate to FP32 when residuals stagnate—all managed by hardware.
- Energy-Aware Edge Deployment: Battery-operated devices can dynamically trade accuracy for energy (favoring INT8 with scaling when power is low, escalating to FP16/FP32 when plugged in).
- Safety-Critical Systems: Avionics, automotive, and medical devices can automatically escalate precision when numerical instability is detected, providing a hardware-level safety mechanism.
- Compiler and Runtime Synergy: The PCU's hardware heuristics can be guided by compiler-inserted metadata (e.g., "this layer is quantization-friendly") or runtime profiling, creating a co-designed software/hardware ecosystem.

6. Limitations

We acknowledge several limitations that contextualize our findings:

Matrix Scale: All experiments used 8×8 matrices. While this validates architectural correctness and numerical behavior, it understates performance differentiation. Larger matrices (64×64, 128×128) would increase arithmetic intensity, shifting the bottleneck from control overhead to arithmetic units and revealing precision-dependent throughput differences.

Simulation vs. Silicon: Results are based on Vivado simulation, which includes compilation overhead. Absolute throughput numbers (136 ops/sec) are artificially low. Post-synthesis timing analysis predicts 50 MHz operation (supporting ~50M matrix multiplies/sec), but we did not synthesize to ASIC or finalize an FPGA bitstream. Power consumption measurements are unavailable.

Condition Number Range: We tested $\kappa \in [1, 1000]$. Extremely ill-conditioned systems ($\kappa > 10^6$), common in least-squares problems or near-singular matrices, may reveal FP16 limitations not observed here. Future work should extend to $\kappa = 10^6$–10^{12} to map the FP16/FP32 transition boundary.

Workload Diversity: Random matrices with controlled condition numbers differ from real neural network weight distributions (typically Gaussian, Xavier, or Kaiming initialization). Evaluation on trained CNN models (ResNet, MobileNet) or transformers (BERT, GPT) would better represent production workloads.

Static Precision Per Run: The current implementation fixes precision at the start of each test. True dynamic switching—changing precision mid-execution when condition number shifts—would introduce pipeline bubbles (1–2 cycles during mode transition) that we have not characterized.

7. Future Work

Immediate Extensions (3–6 months):

1. Scale to Production Sizes: Evaluate 64×64 and 128×128 matrices to validate projected memory bandwidth and throughput improvements.
2. Synthesize to Silicon: Implement on ASIC (OpenLane, Skywater 130nm PDK) or finalize FPGA bitstream to measure real-world power, area, and timing.

3. INT8 Quantization Support: Integrate per-tile scale factor computation into the PCU for safe INT8 operation.
4. Dynamic Precision Switching: Enable mid-execution transitions when condition number changes. Measure pipeline bubble overhead.
5. Real CNN Evaluation: Run inference on quantized ResNet-18 or MobileNetV2, comparing MPP's adaptive precision against fixed-precision baselines.

Medium-Term Directions (6–12 months):

6. Systolic Array Scaling: Replicate the single PE design into a 16×16 or 32×32 systolic array for true ML accelerator performance.
7. BFloat16 Support: Add BF16 as a fourth precision mode (better dynamic range than FP16, used by Google TPU and Intel AVX-512).
8. RISC-V Vector Integration: Map the MPP design to RISC-V Vector (RVV) instructions for ISA compliance.
9. Learned Precision Policies: Use reinforcement learning to train a PCU policy on real workloads rather than hand-tuned thresholds.

Long-Term Vision (1–2 years):

10. Heterogeneous Precision Tiles: Allow different tiles of the same matrix to use different precisions.
11. Cross-Layer Optimization: Integrate with ML frameworks (PyTorch, TensorFlow) to propagate precision decisions across layers.
12. Formal Verification: Prove numerical bounds on worst-case error amplification using interval arithmetic.

8. Closing Remarks

The Mixed Precision Pipeline establishes a foundation for hardware-managed numerical precision as a first-class architectural concern. While the current 8×8 prototype reveals no performance differentiation due to control overhead dominance, it successfully demonstrates:

- Architectural feasibility: Precision switching with <20 LUT overhead
- Numerical characterization: FP16 = FP32 accuracy; INT8 fails without scaling
- Design principles: Range analysis beats condition number for INT8 safety

The fundamental insight remains: not all data needs 32 bits. By embedding precision selection in hardware—guided by numerical analysis, not programmer annotations—the MPP offers a path toward more efficient, adaptive computing for the AI era.

Our most important contribution may be the negative result: demonstrating that naive INT8 fails catastrophically. This finding validates the sophisticated quantization infrastructure in modern ML frameworks (PyTorch's `torch.quantization`, TensorFlow Lite) and establishes empirical baselines for future mixed-precision accelerator designs.

As AI workloads continue to dominate computing, and as energy efficiency becomes paramount for edge deployment and sustainability, adaptive precision management will transition from optional optimization to architectural necessity. The Mixed Precision Pipeline provides a working prototype and empirical foundation for this transition.

6. REFERENCES

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R. Krishnamoorthi, "Quantizing Deep Convolutional Networks for Efficient Inference: A Whitepaper," arXiv:1806.08342, 2018.

7. APPENDIX

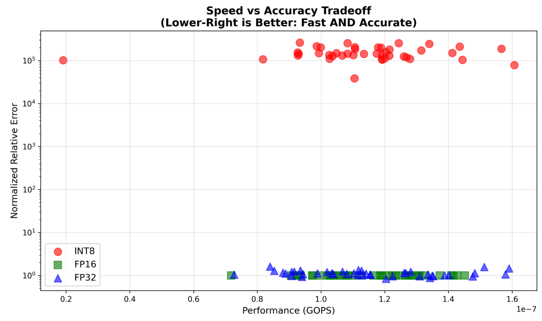

Figure 1

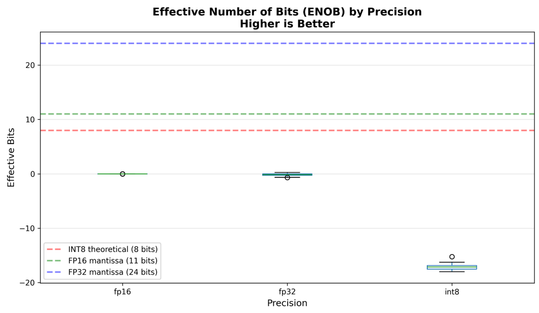

Figure 2

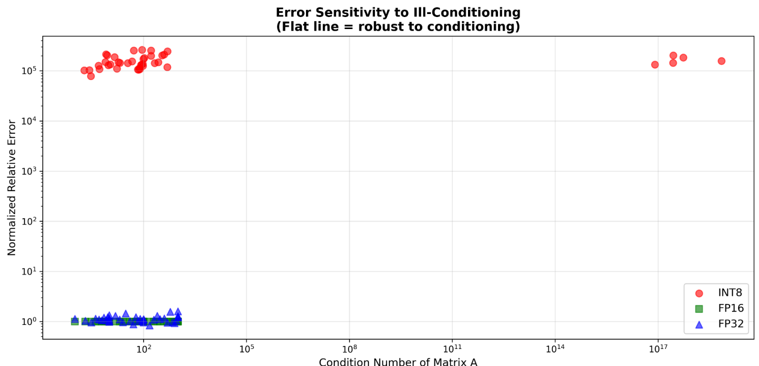

Figure 3

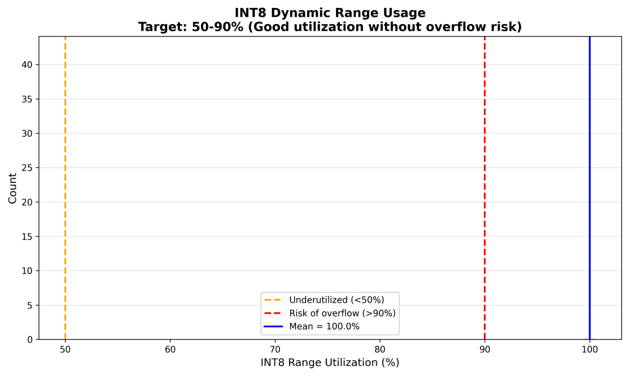

Figure 4

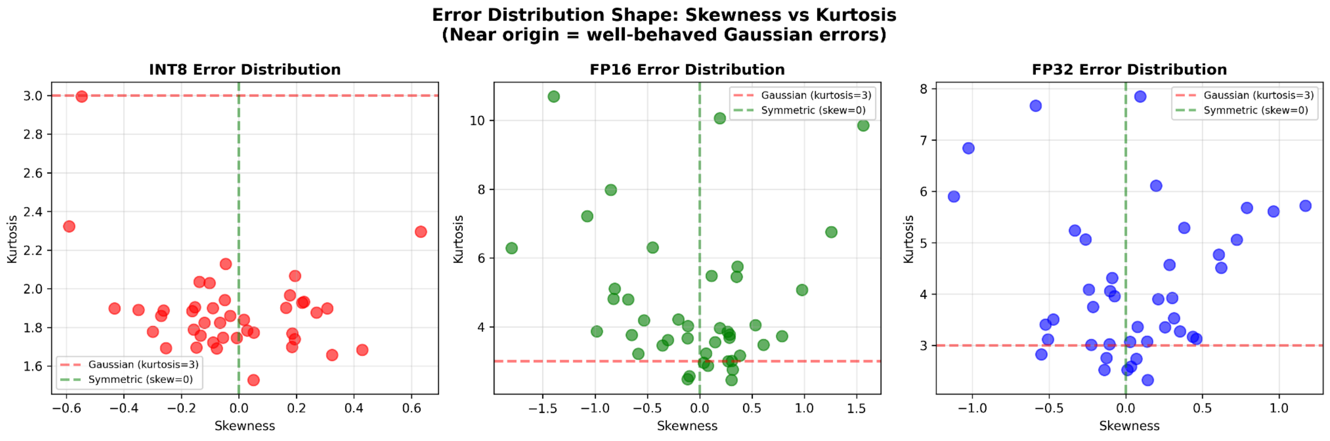

Figure 5

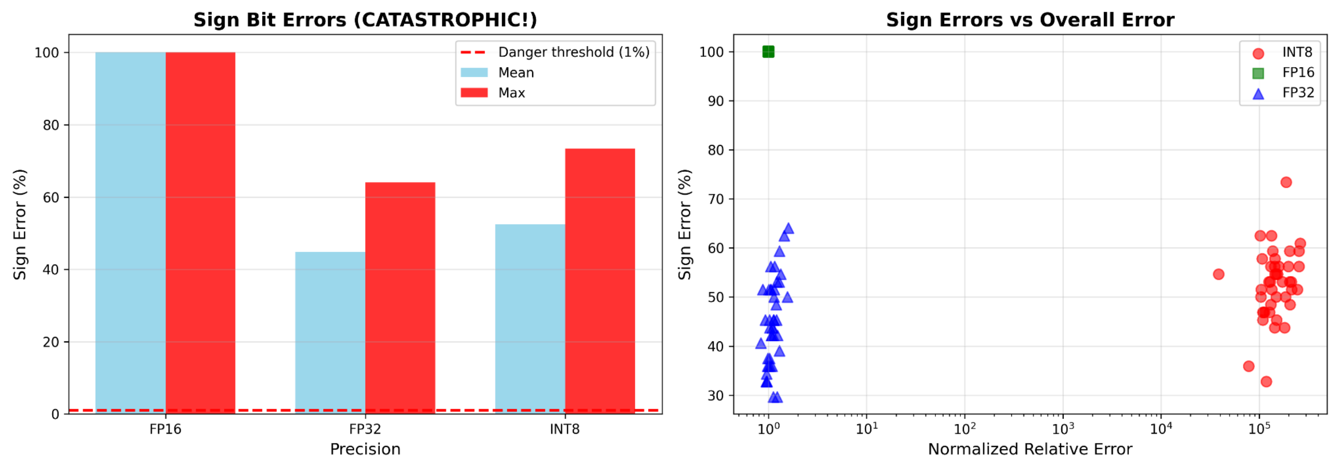

Figure 6

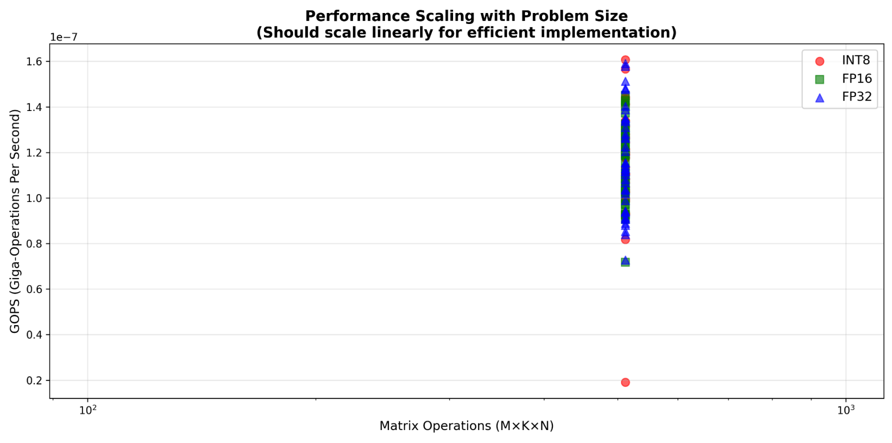

Figure 7

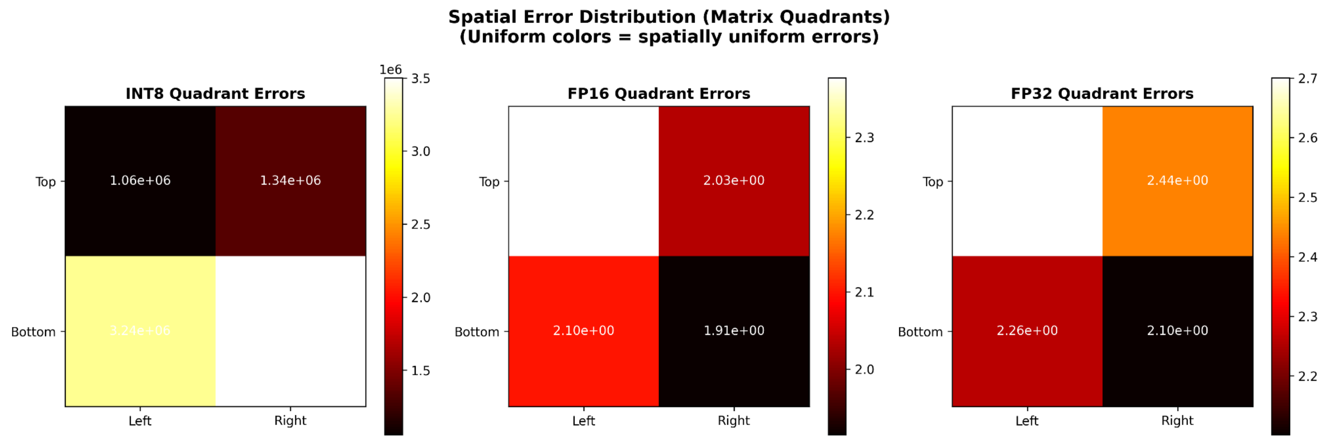

Figure 8

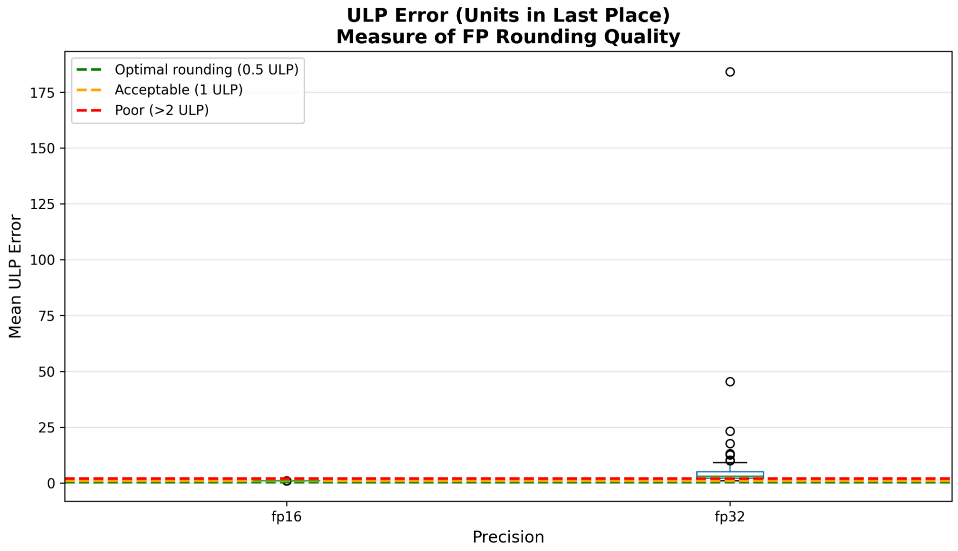

Figure 9

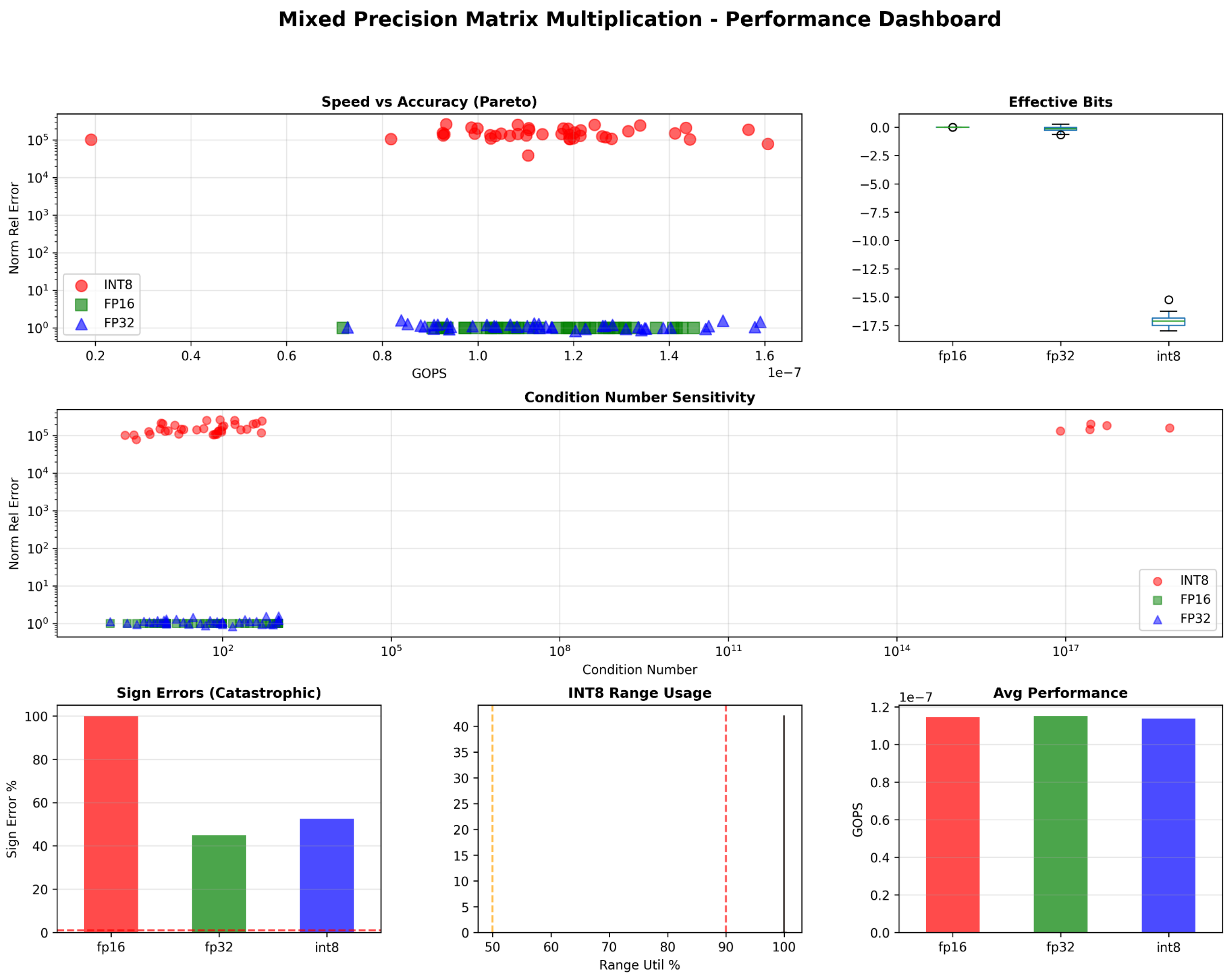

Figure 10

Table 1.

Metric	INT8	FP16	FP32
Throughput (ops/sec)	136.1 ± 24.3	135.2 ± 17.3	138.5 ± 22.5
Median MAE	2.17×10^6	2.09	2.37
Norm. Rel. Error	1.44×10^5	1.00	1.09
SNR (dB)	-103.2	-0.00	-0.91
Mean Sign Error (%)	52	~0*	45
Range Utilization (%)	100	N/A	N/A

Correlation with Ref	-0.04	0.06	0.15