

CMOS Circuit Design Workshop - Spice Simulation using Sky130nm Technology

Lab Documentation

Day 01 day1_nfet_idvds_L2_W5.spice

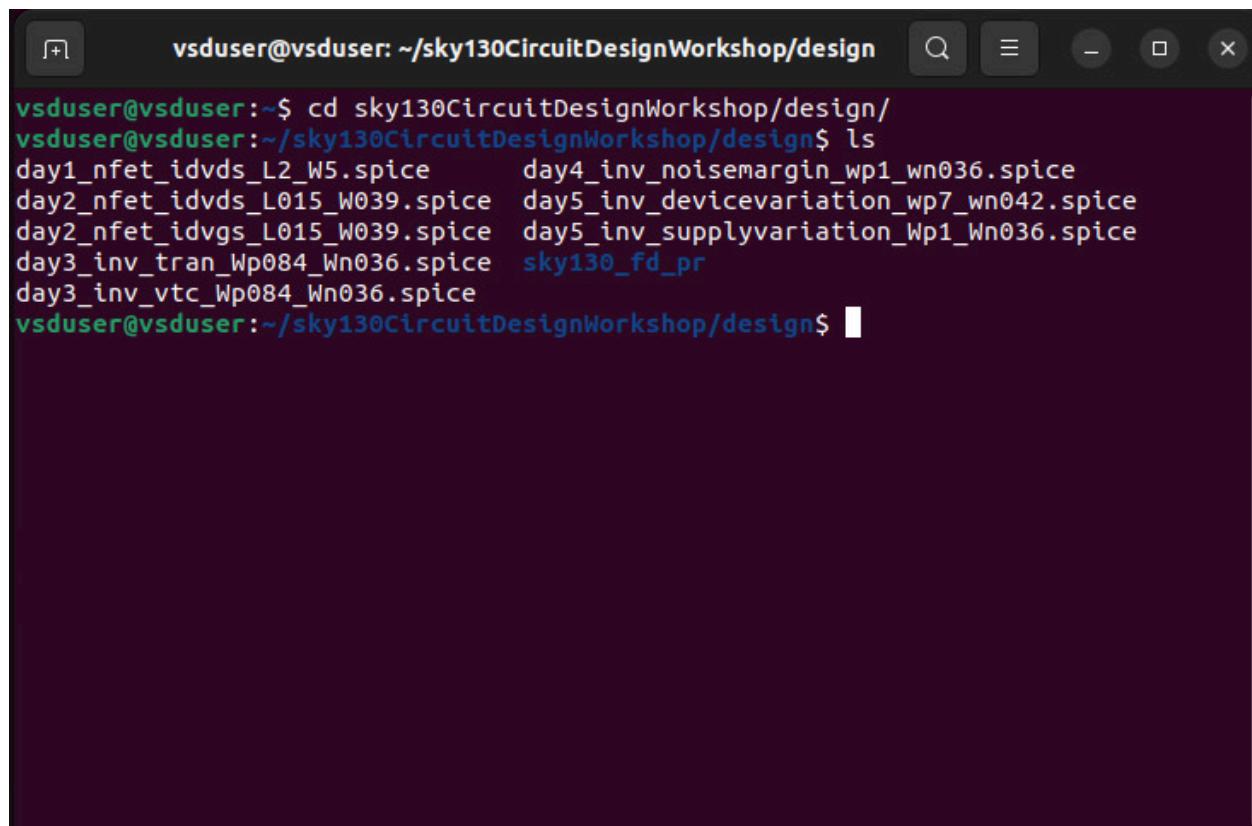
Open virtual Box

In the Terminal Emulator, Open the folder of design files by the following command :

```
cd sky130CircuitDesignWorkshop/design/
```

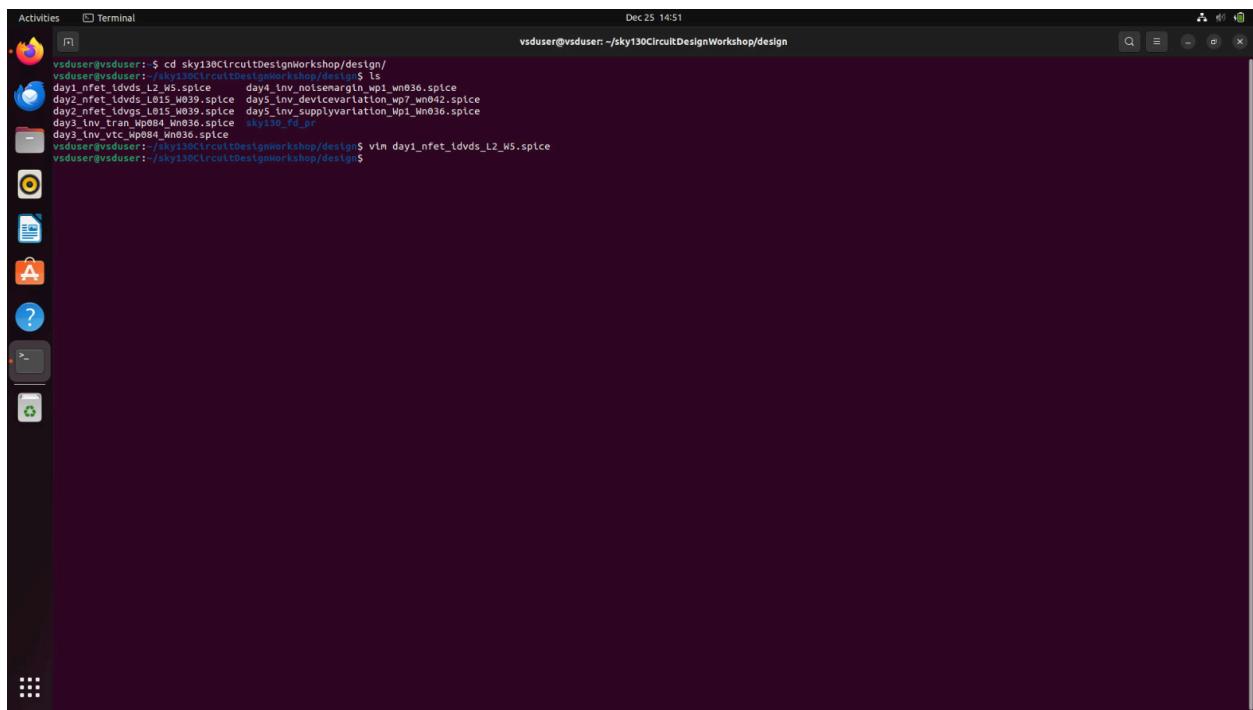
Now type **ls** and enter to see the list of the list of design files

In that,



```
vsduser@vsduser:~/sky130CircuitDesignWorkshop/design$ cd sky130CircuitDesignWorkshop/design/
vsduser@vsduser:~/sky130CircuitDesignWorkshop/design$ ls
day1_nfet_idvds_L2_W5.spice      day4_inv_noisemargin_wp1_wn036.spice
day2_nfet_idvds_L015_W039.spice   day5_inv_devicevariation_wp7_wn042.spice
day2_nfet_idvgs_L015_W039.spice   day5_inv_supplyvariation_Wp1_Wn036.spice
day3_inv_tran_Wp084_Wn036.spice   sky130_fd_pr
day3_inv_vtc_Wp084_Wn036.spice
vsduser@vsduser:~/sky130CircuitDesignWorkshop/design$
```

code for lab1 is seen using vim editor as follows,



A screenshot of a Linux desktop environment showing a terminal window. The terminal window has a dark background and contains the following text:

```
Activities Terminal Dec 25 14:51
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design/
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$ ls
day1_nfet_ldvds_L2_W5.spice  day4_inv_nosemargin_wp1_wn036.spice
day2_nfet_ldvds_L015_W039.spice  day5_inv_devicevariation_wp7_wn042.spice
day2_nfet_ldvgs_L015_W039.spice  day5_inv_supplyvariation_Wp1_Wn036.spice
day3_lrn_trn_wp084_Wn036.spice  sky130_fd_pr
day3_lnv_vtc_Wp084_Wn036.spice
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$ vim day1_nfet_ldvds_L2_W5.spice
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$
```

The terminal window is titled "Terminal" and shows the date and time as "Dec 25 14:51". The command "ls" lists several SPICE files. The command "vim day1_nfet_ldvds_L2_W5.spice" is shown being entered. The window title bar also displays the path "vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design". On the left side of the terminal window, there is a vertical dock with icons for various applications like a browser, file manager, terminal, and help.

```

Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description

XM1 Vdd n1 0 0 sky130_fd_pr_nfet_01v8 w=5 l=2

R1 n1 in 55

Vdd vdd 0 1.8V
Vin in 0 1.8V

*simulation commands

.op
.dc Vdd 0 1.8 0.1 Vin 0 1.8 0.2

.control

run
display
setplot dc1
.endc

.end

```

Above we see Vdd varying from 0 to 1.8 volts with step size of 0.1V and Vgs sweeping from 0 to 1.8V and with step size of 0.2V

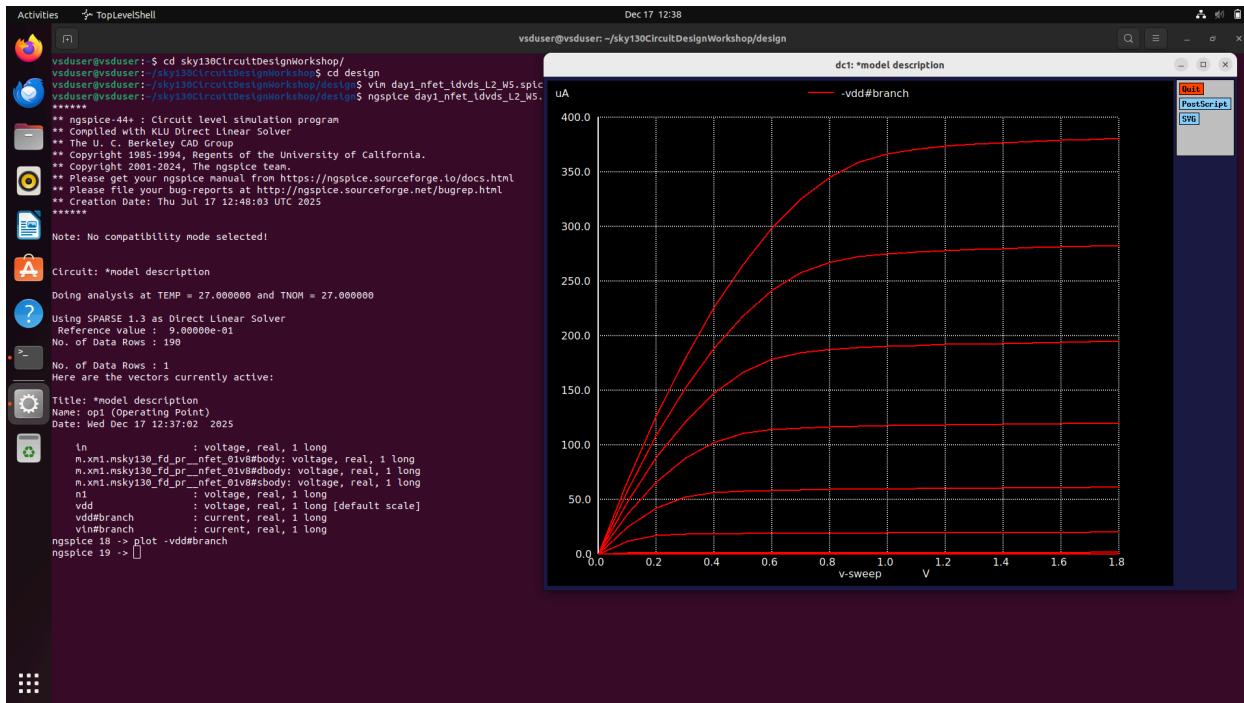
Now let's do spice simulation by the following command :

```
ngspice day1_nfet_idvds_L2_W5.spice
```

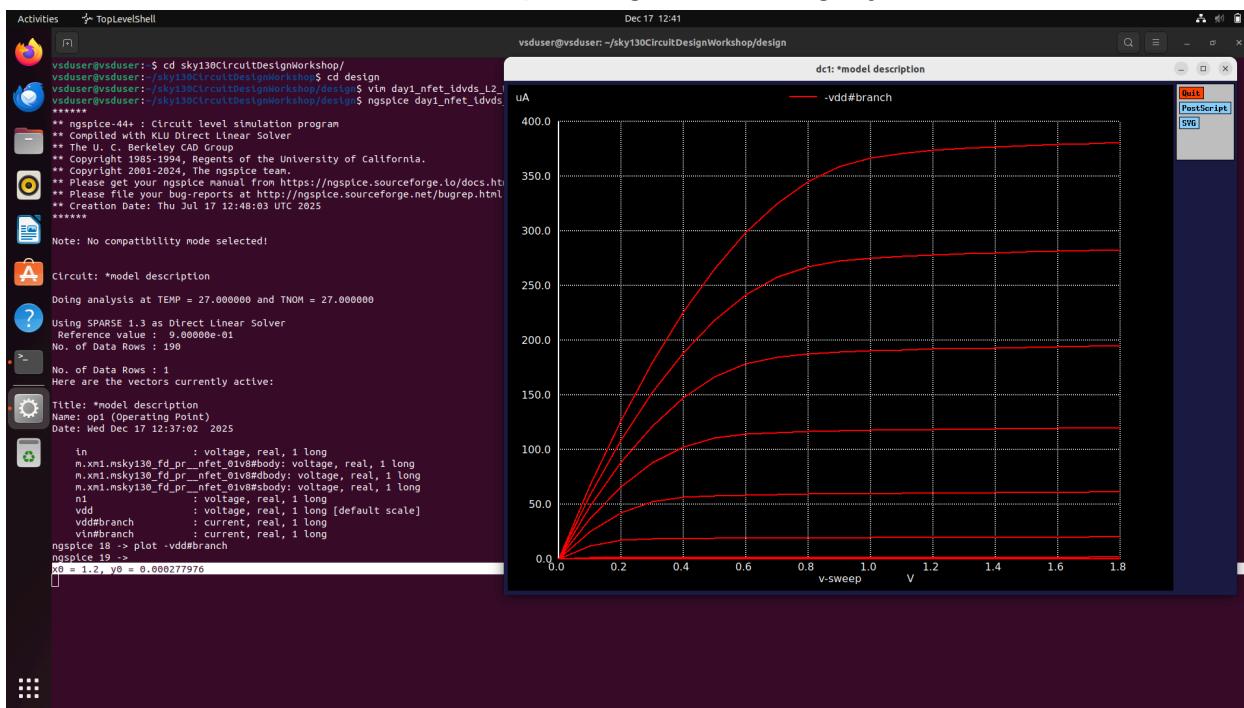
Then,

Plot -vdd#branch

The result is a plot of the above spice code in another tab as pop-up

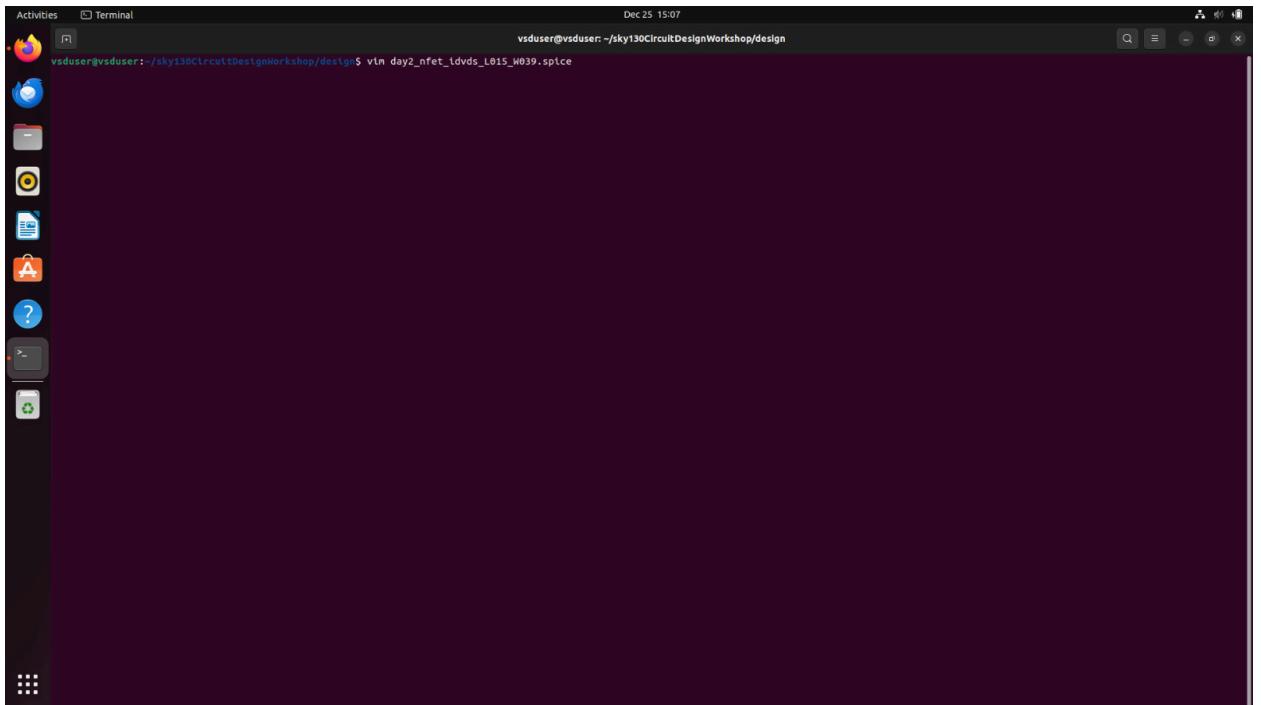


To check the value of Id for corresponding Vds and Vgs, just left click and see,



Day 02:

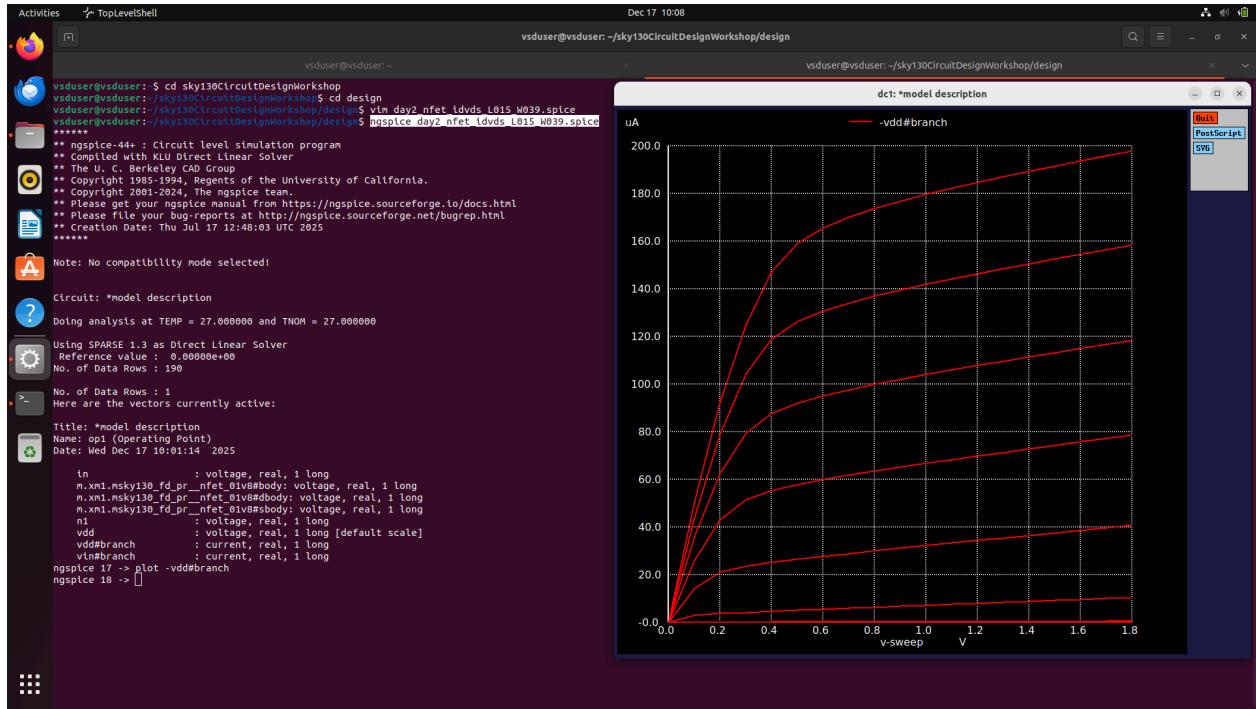
Lab 2.1 - day2_nfet_idvds_L015_W039.spice



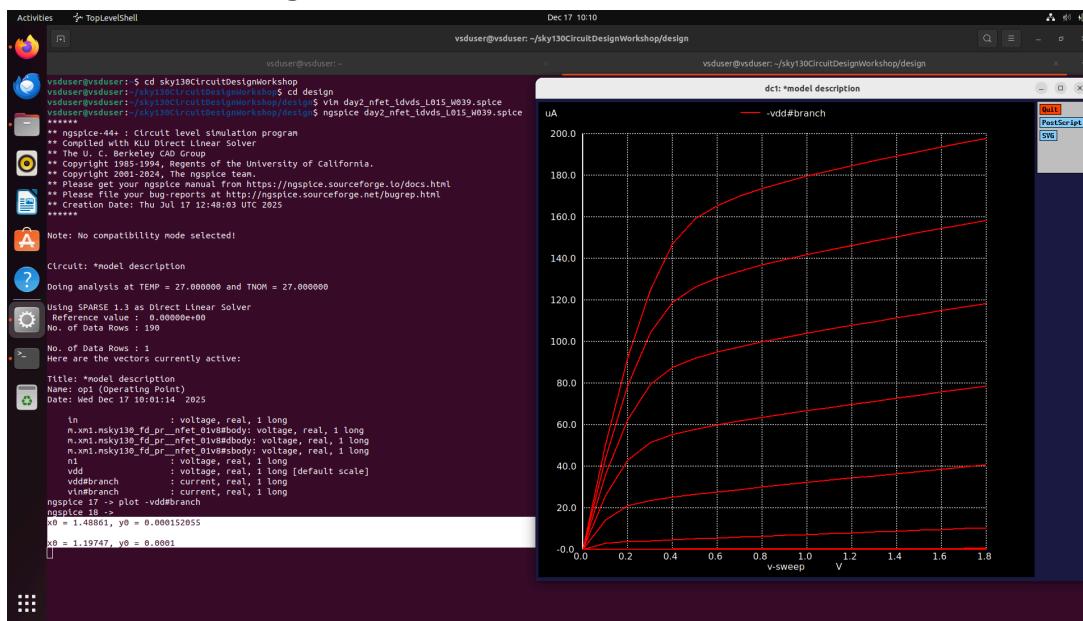
The spice code for the day 2 Id vs Vgs is given below,

```
/*including sky130 library files
.ltb "sky130_fd_pr/models/sky130.lib.spice" tt
*Netlist Description
XH1 Vdd n1 0 0 sky130_fd_pr_nfet_01v8 w=0.39 l=0.15
R1 n1 tn 55
Vdd vdd 0 1.8V
Vtn tn 0 1.8V
*A *simulation commands
.op
.dc Vdd 0 1.8 0.1 Vin 0 1.8 0.2
.control
run
display
setplot dc1
.endc
.end
*/
/*day2_nfet_idvds_L015_W039.spice" 33L, 344B
```

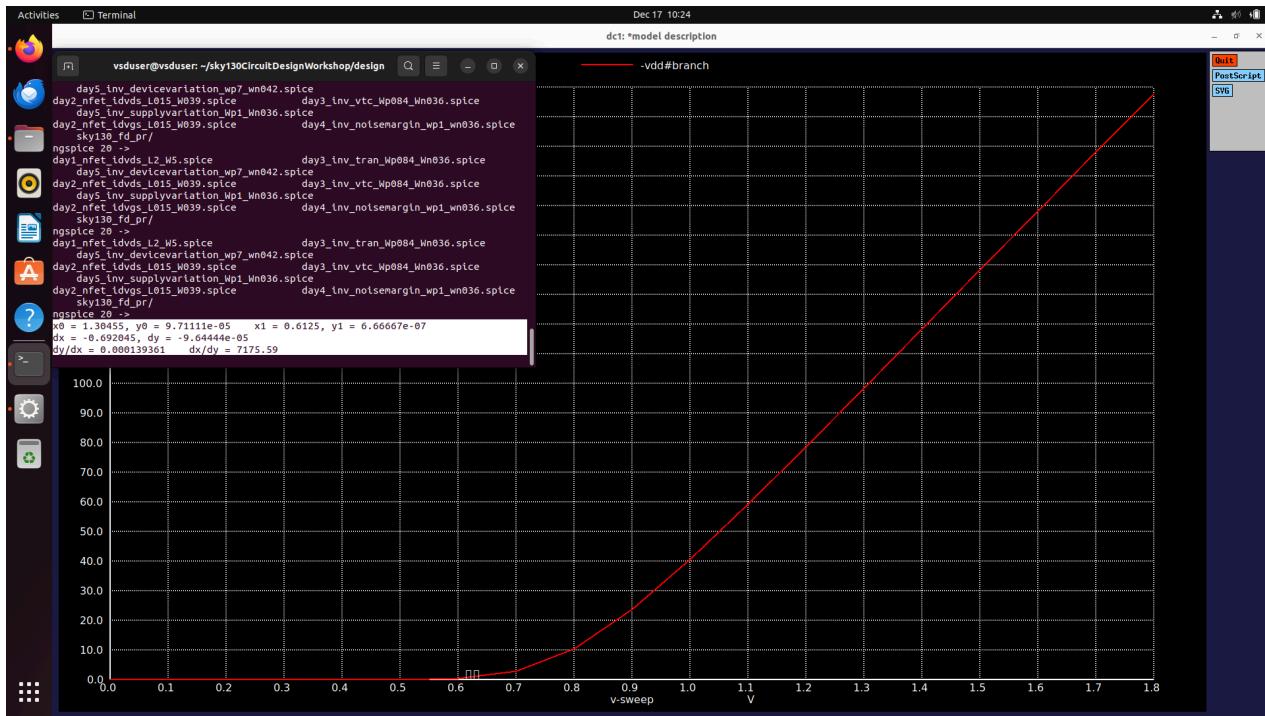
From the above code, we can see the values for L and W is 0.15u and W=0.39u.



The plot shows **I_d vs V_{ds}** for different **V_{gs}** values. For low values of V_{gs} , it is showing **quadratic type behaviour**, and for higher V_{gs} values it becomes **almost linear**. If we want to see the peak current for $V_{gs} = 1.8$ V, just **left click on the curve at $V_{gs} = 1.8$ V**.



Here also, we take $L = 0.15\mu$ and $W = 0.39\mu$. V_{ds} is maintained at 1.8 V and V_{gs} is swept from 0 to 1.8 V in steps of 0.1 V.



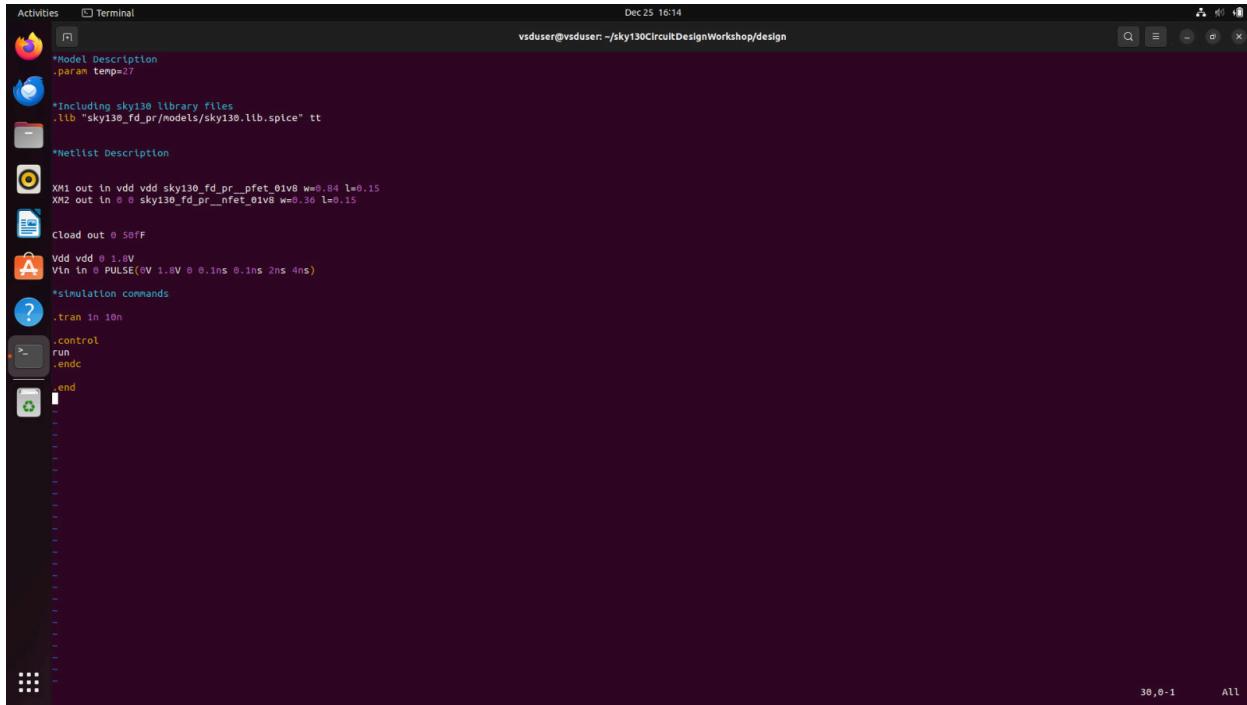
In the above graph we can see that, due to short channel effect we are seeing a linear behaviour for higher V_{gs} and V_{ds} being constant.

From the above curve we can find threshold voltage by seeing that V_t is the value when current increases drastically for small change in V_{gs} . To calculate we will draw tangent on the curve and see where it touches.

It comes around 0.72

Day 03 :

Lab 3.1 - day3_inv_tran_Wp084_Wn036.spice



```
Dec 25 16:14
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design

*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description

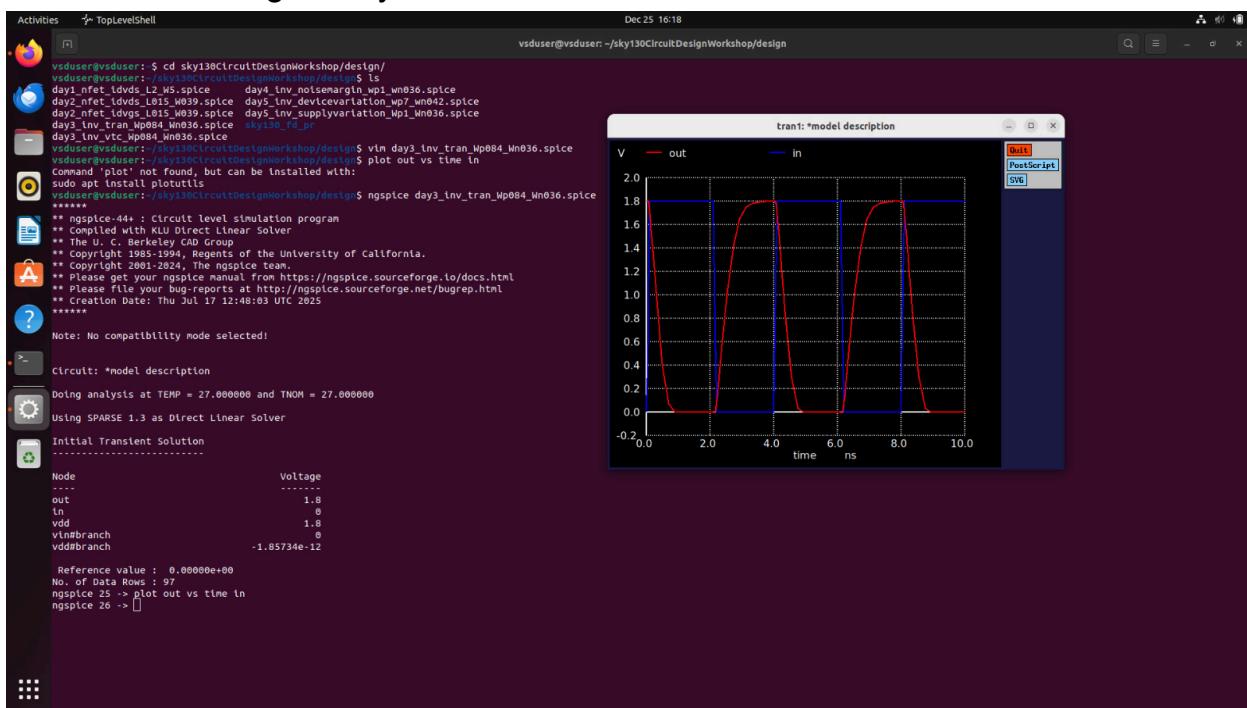
XM1 out in vdd vdd sky130_fd_pr_nfet_01v8 w=0.84 l=0.15
XM2 out in @ @ sky130_fd_pr_nfet_01v8 w=0.30 l=0.15

Cload out @ 50ff

Vdd vdd @ 1.8V
Vin in @ PULSE(0V 1.8V 0 0.ns 2ns 4ns)

*Simulation commands
.tran in 10n
.control
  run
  .endc
.end
```

The waveform is given by,



```
Dec 25 16:18
vsduser@vsduser: $ cd sky130CircuitDesignWorkshop/design/
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$ ./run.sh
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$ vim day3_inv_tran_Wp084_Wn036.spice
day2_nfet_ldvds_L015_W039.spice day4_inv_nosemargin_Wp1_Wn036.spice
day2_nfet_ldvds_L015_W039.spice day5_inv_devicevariation_Wp7_Wn036.spice
day3_inv_tran_Wp084_Wn036.spice sky130_fd_pr
day3_inv_vtc_Wp084_Wn036.spice
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design$ ngsim day3_inv_tran_Wp084_Wn036.spice
***ngspice-4.4 : Circuit Level simulation program
** compiled with KLU Direct Linear Solver
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2024, The ngspice team.
** Please get your ngspice manual from https://ngspice.sourceforge.io/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Thu Jul 17 12:48:03 UTC 2025
*****
Note: No compatibility mode selected!

Circuit: *model description

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
Using SPARSE 1.3 as Direct Linear Solver

Initial Transient Solution
-----
Node          Voltage
---- -----
out           1.8
in            0
vdd           1.8
vinbranch     0
vddbranch    -1.85734e-12

Reference value : 0.00000e+00
No of Data Rows : 97
ngspice 25 -> plot out vs time in
ngspice 26 -> [ ]
```

tran1: *model description

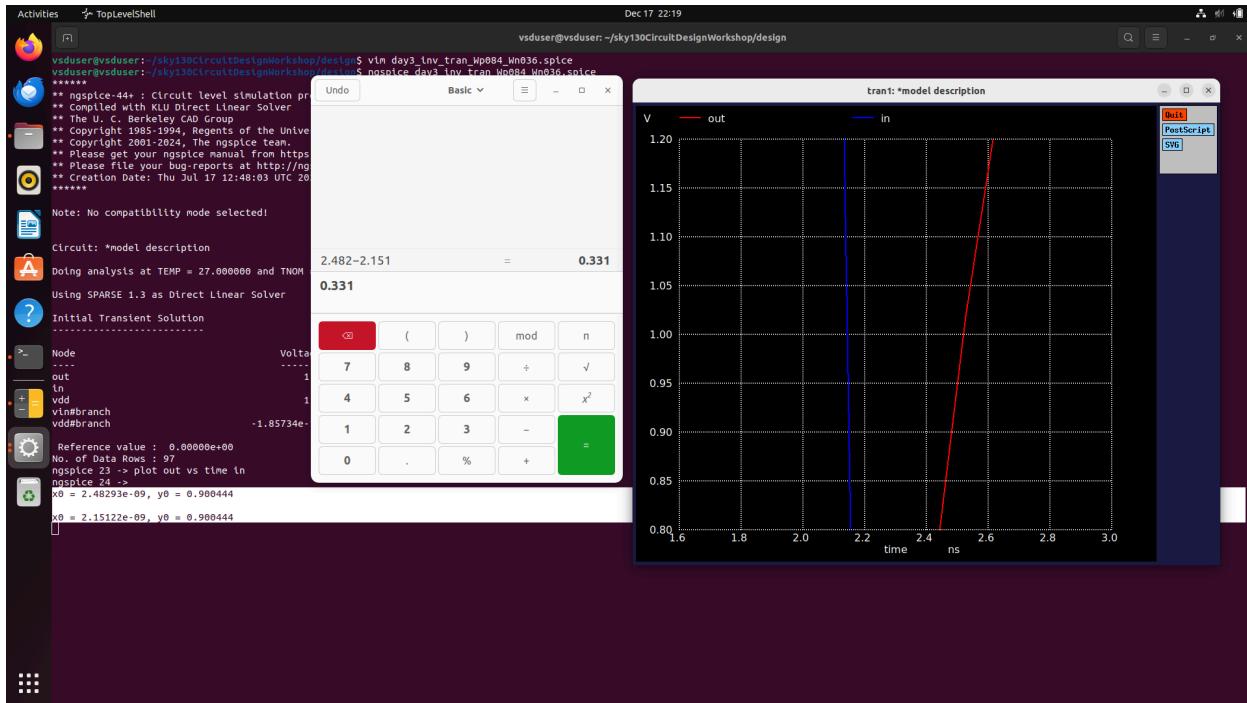
V — out — in

time 0.0000000000000000 ns

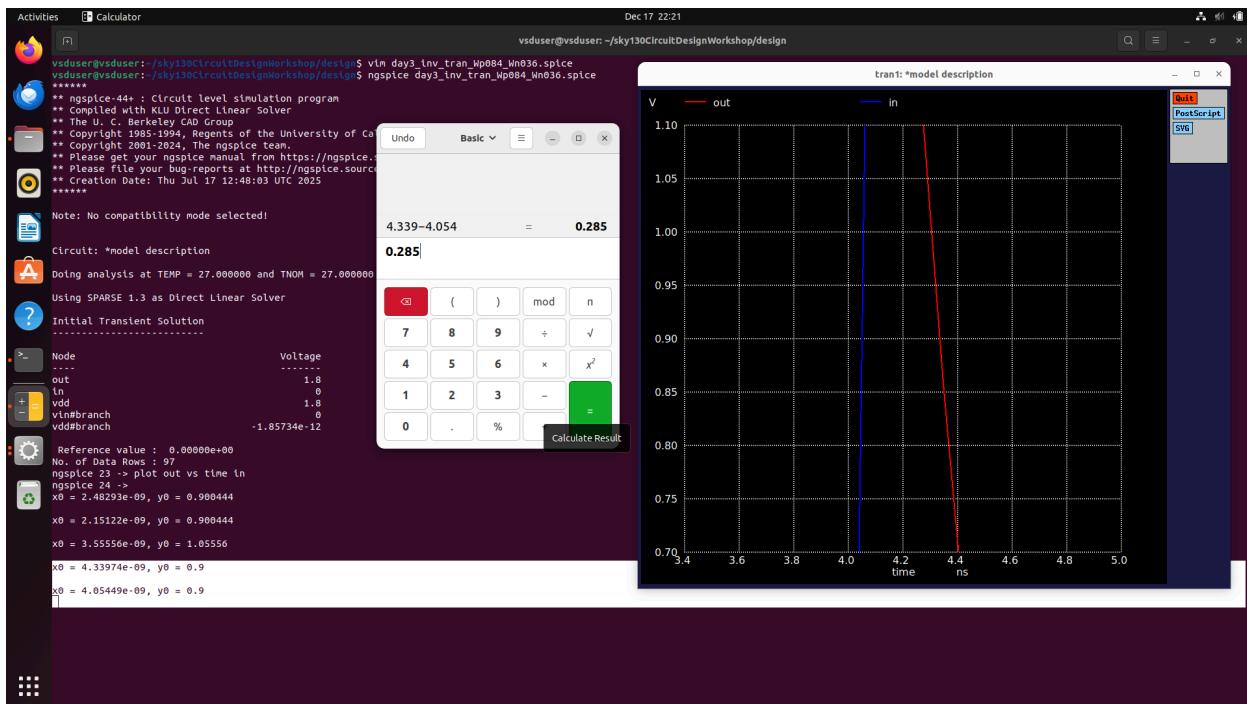
Time (ns)	out (V)	in (V)
0.0000000000000000	1.8000000000000000	0.0000000000000000
1.5000000000000000	0.0000000000000000	1.8000000000000000
3.0000000000000000	1.8000000000000000	0.0000000000000000
4.5000000000000000	0.0000000000000000	1.8000000000000000
6.0000000000000000	1.8000000000000000	0.0000000000000000
7.5000000000000000	0.0000000000000000	1.8000000000000000
9.0000000000000000	1.8000000000000000	0.0000000000000000
10.0000000000000000	1.8000000000000000	0.0000000000000000

From the above waveform we can find the Rise and Fall Delay

Rise Delay :



Fall Delay :



Lab 3.2 - day3_inv_vtc_Wp084_Wn036.spice

Spice code for the VTC Characteristics can be given by,

```
Activities Terminal Dec 25 16:24
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design
*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

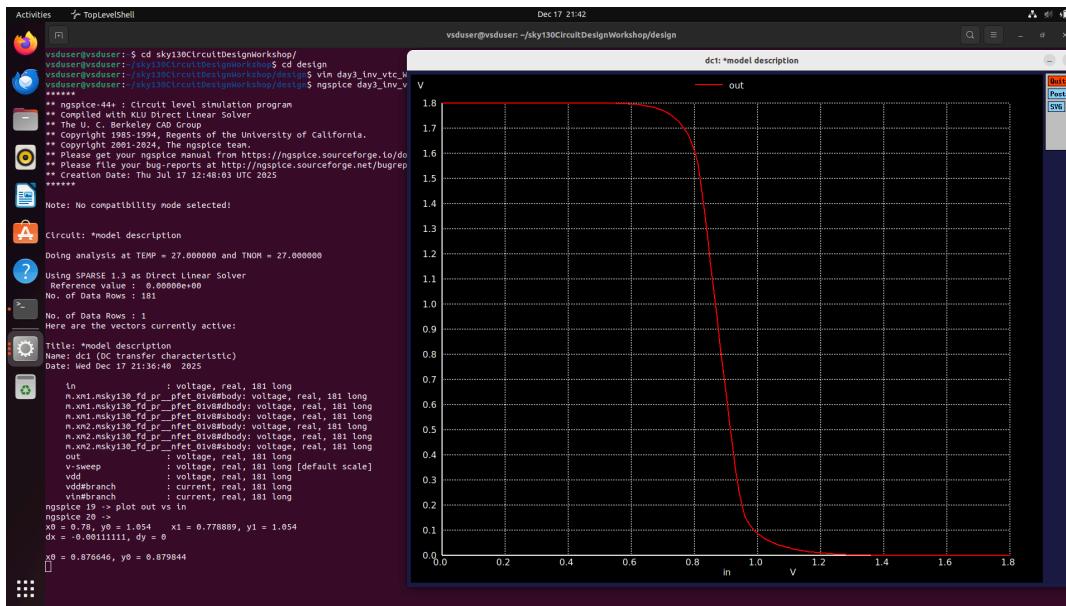
*Netlist Description
XH1 out in vdd vdd sky130_fd_pr_pfet_01v8 w=0.84 l=0.15
XH2 out in s 0 sky130_fd_pr_nfet_01v8 w=0.36 l=0.15

Cload out 0 50FF
Vdd vdd 0 1.8V
Vtn in 0 1.8V

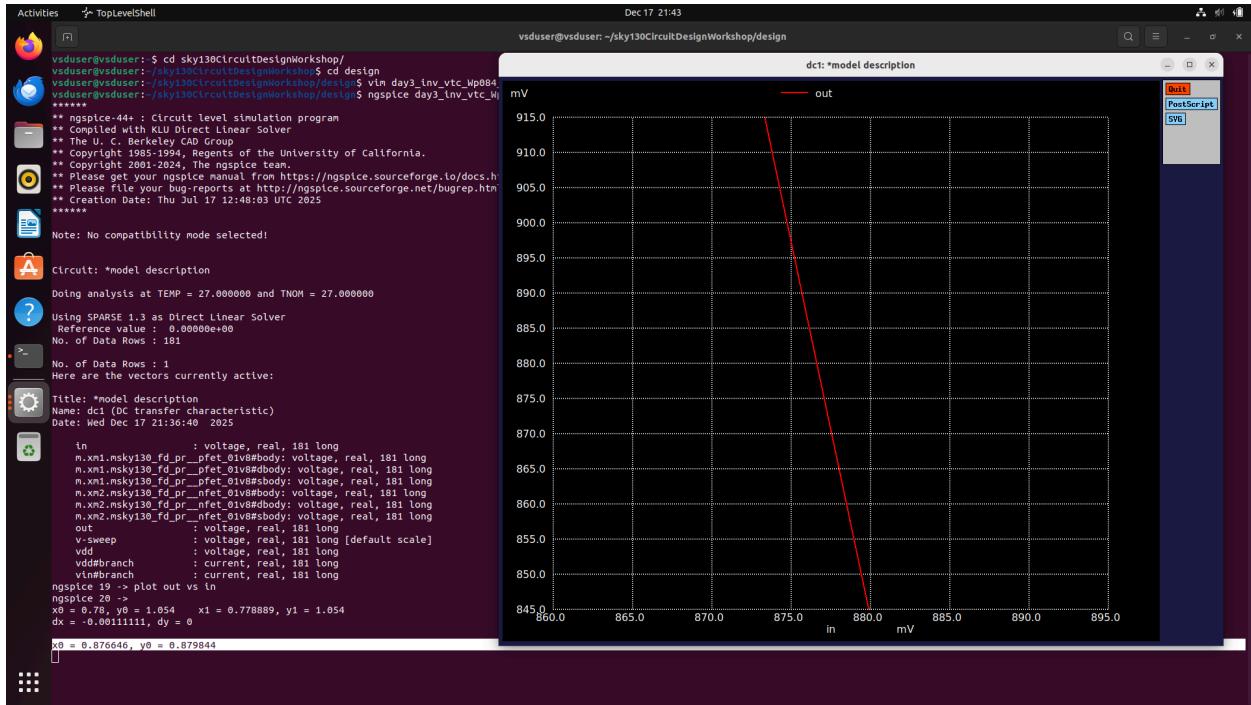
*simulation commands
.op
.dc Vtn 0 1.8 0.01
.control
run
setplot dci
display
.endc
.end

day3_inv_vtc_Wp084_Wn036.spice" 34L, 393B 34,0-1 All
```

Here we are using pfet and nfet for the CMOS inverter. The W/L ratio of pmos is taken as 2.33 times compared to nmos. Vin is swept from 0 to 1.8 V with step size 0.01 V and Vout is plotted,



Now we need to find the switching threshold from this graph. It is the point where Vin is equal to Vout. To zoom into the curve, press the right mouse button and hold it.



Day 04 :

Lab 4.1 - Day4_inv_noisemargin_wp1_wn036.spice

Here is the spice code for day4

```

Activities Terminal Dec 25 10:35
vsduser@vsduser: ~/sky130CircuitDesignWorkshop/design

*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description
XM1 out in vdd vdd sky130_fd_pr_pfet_01v8 w=1 l=0.15
XM2 out in 0 0 sky130_fd_pr_nfet_01v8 w=0.36 l=0.15

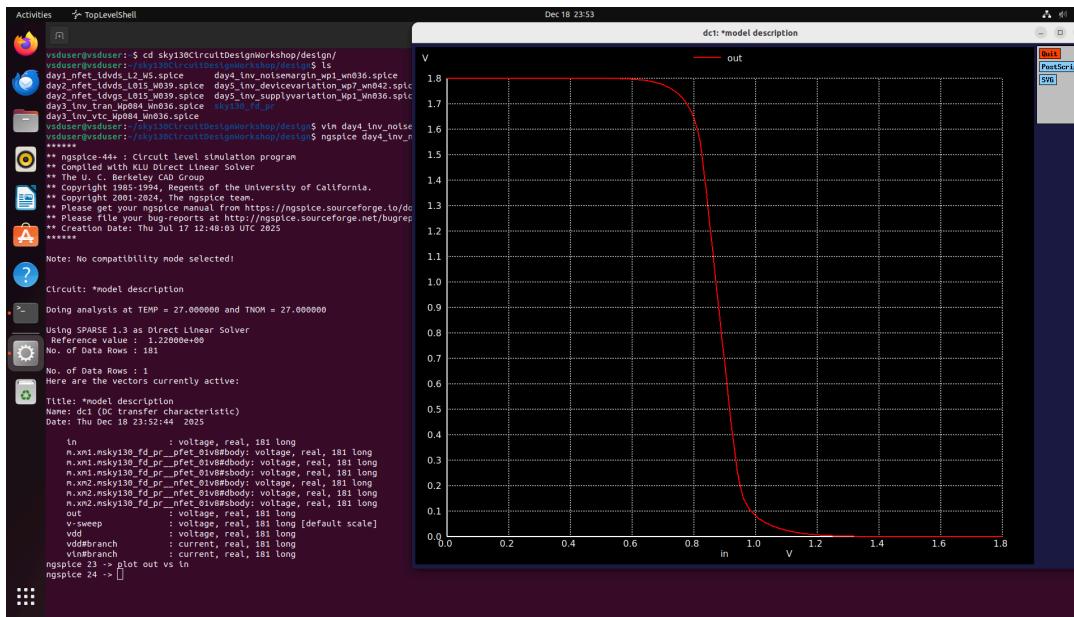
Cload out 0 50fF
Vdd vdd 0 1.8V
Vth th 0 1.8V

*simulation commands
.op
.dc Vln 0 1.8 0.01
.control
run
setplot dc1
display
.endc

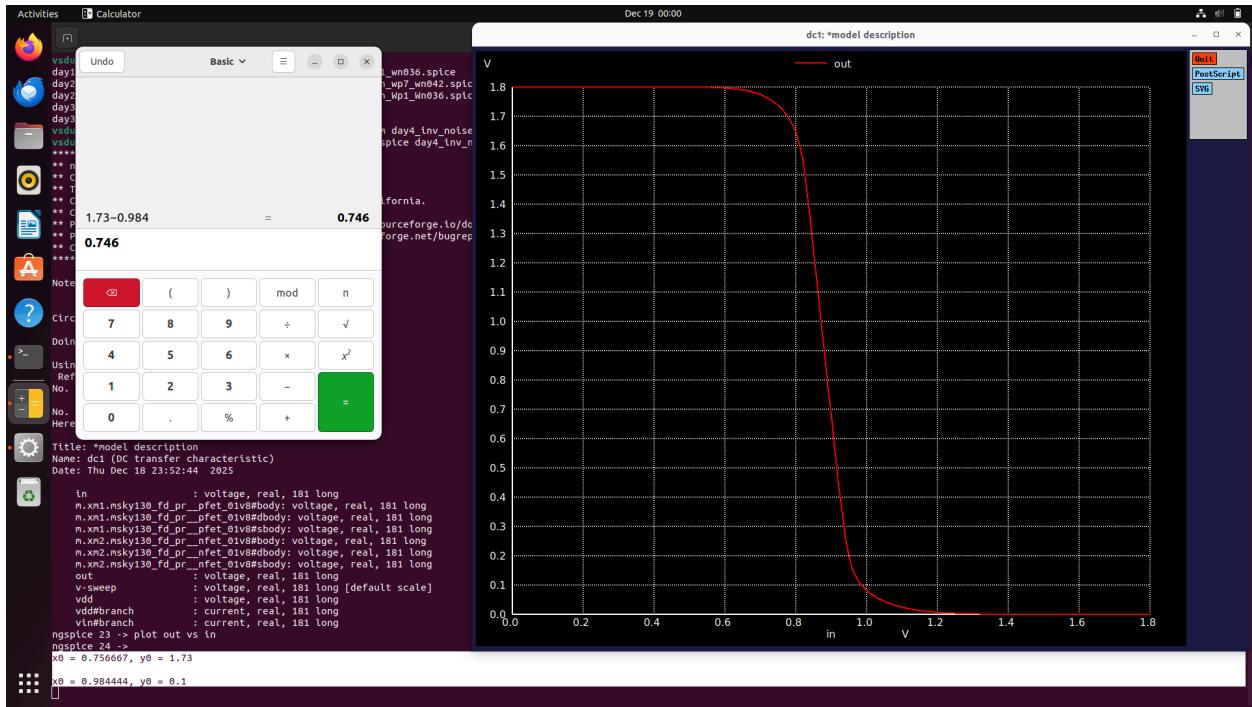
.end

```

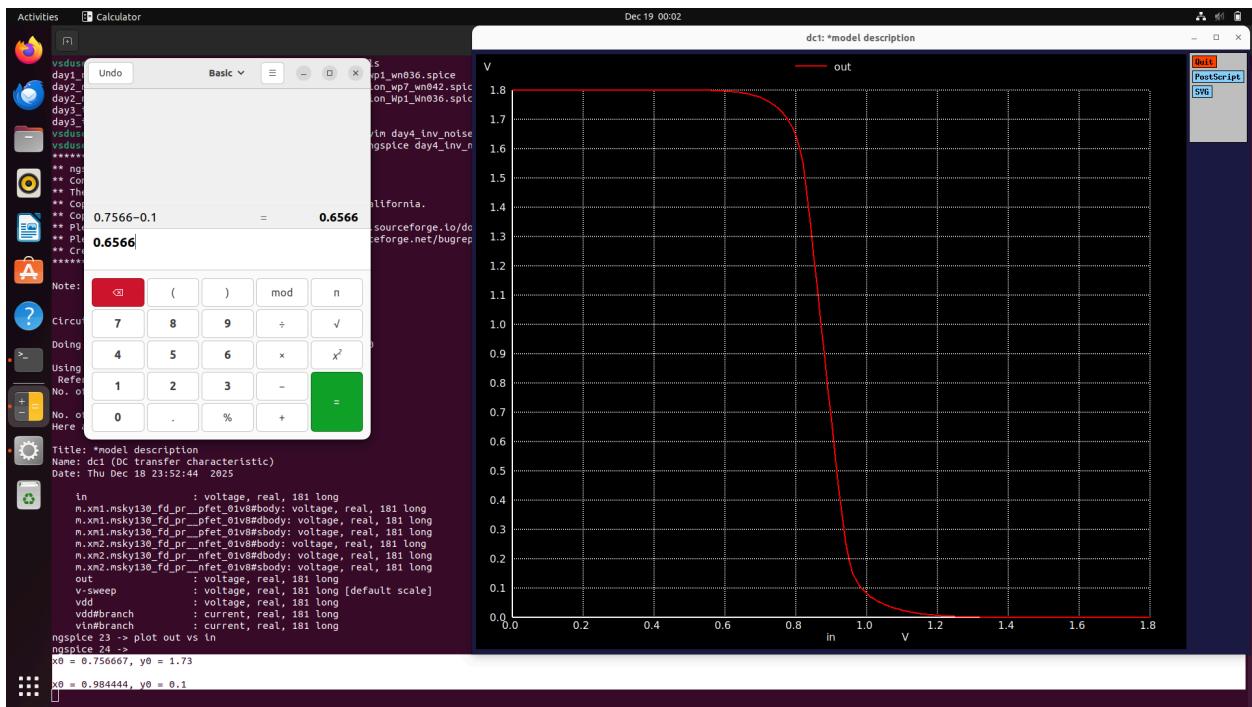
Here we take the W/L ratio of PMOS and NMOS as 2.77 and Vin is sweeped from 0 to 1.8 V with stepsize 0.01 V,



Noise Margin High :



Noise Margin Low:



We take the point where slope becomes -1 . The x axis gives V_{IL} and V_{IH}, while the y axis gives V_{OH} and V_{OL}.

$$\text{Noise Margin High} = V_{OH} - V_{IH} = 1.73 - 0.984 = 0.746$$

$$\text{Noise Margin Low} = V_{IL} - V_{OL} = 0.7566 - 0.1 = 0.6566$$

Day 05 :

Lab 5.1 - Supply Variation

day5_inv_supplyvariation_Wp1_Wn036.spice

Spice Code is given below,

```
*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist Description
XH1 out in vdd vdd sky130_fd_pr_nfet_01v8 w=0.15 l=0.15
XM2 out in @ @ sky130_fd_pr_nfet_01v8 w=0.30 l=0.15

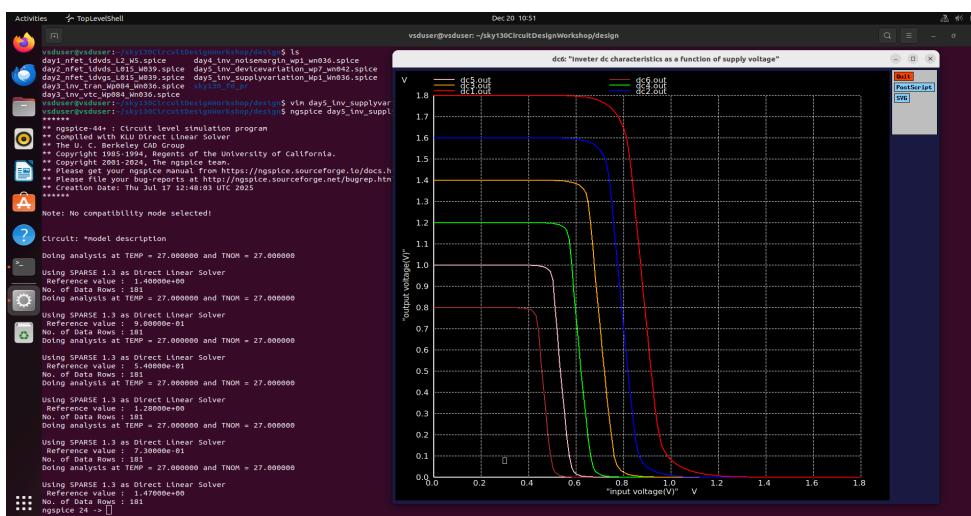
Cload out @ .5OFF
Vdd vdd @ 1.8V
Vin in @ 1.8V

.control
let powersupply = 3.8
alter Vdd = powersupply
    let voltagesupplyvariation = 0
        doWhile voltagesupplyvariation < 6
        dc Vin @ 1.8 0.01
        let powersupply = powersupply - 0.2
        alter Vdd = powersupply
            let voltagesupplyvariation = voltagesupplyvariation + 1
end

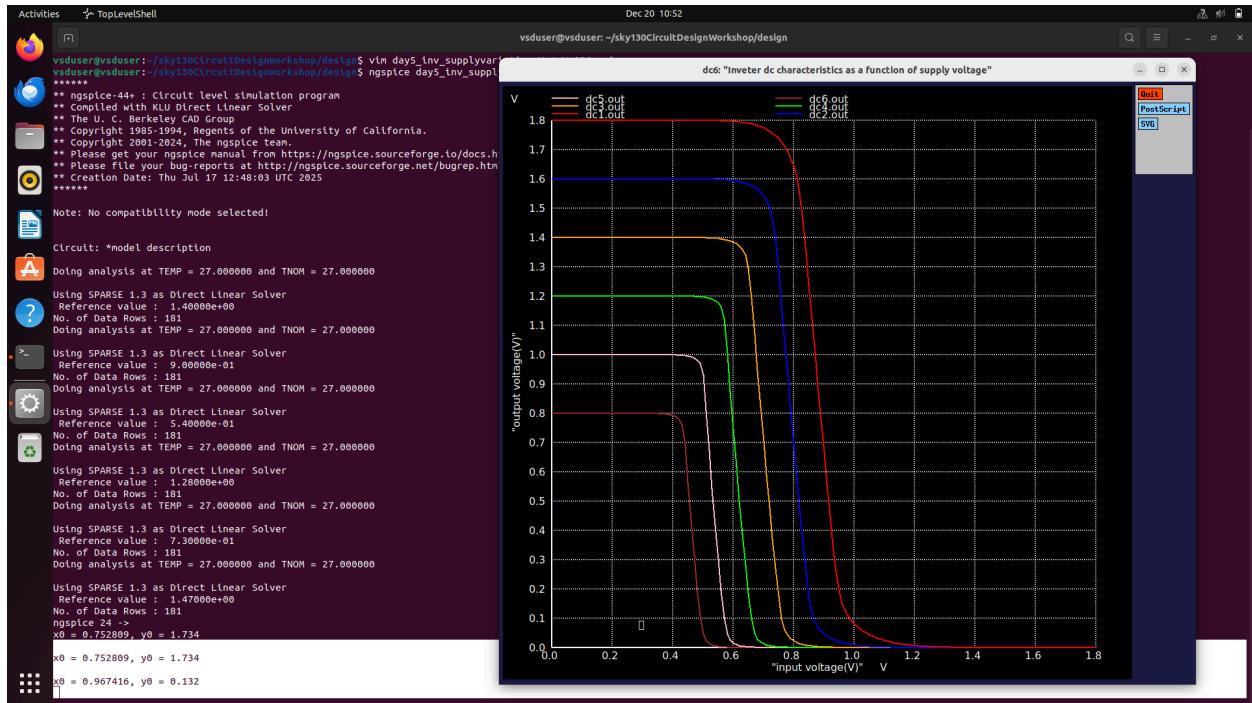
plot dc1.out vs in dc2.out vs in dc3.out vs in dc4.out vs in dc5.out vs in dc6.out vs in xlabel "Input voltage(V)" ylabel "Output voltage(V)" title "Inverter dc characteristics as a function of supply voltage"
.endc
.end

-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
```

First the supply voltage is taken as 1.8 V, then it is decreased by 0.2 V each time. So overall, it gives around 6 iterations.



From the above waveform, we can calculate the gain and supply variation



Lab 5.2 - Device Variation

Day5_inv_devicevariation_wp7_wn042.spice

Spice code can be given by,

```

Activities Terminal
vsduser@vsduser:~/sky130CircuitDesignWorkshop/design$ Dec 25 17:35
*Model Description
.param temp=27

*Including sky130 library files
.lib "sky130_fd_pr/models/sky130.lib.spice" tt

*Netlist description
XM1 out in vdd vdd sky130_fd_pr_pfet_b1v8 w=.07 l=.015
XM2 out in 0 vdd sky130_fd_pr_nfet_b1v8 w=.02 l=.015

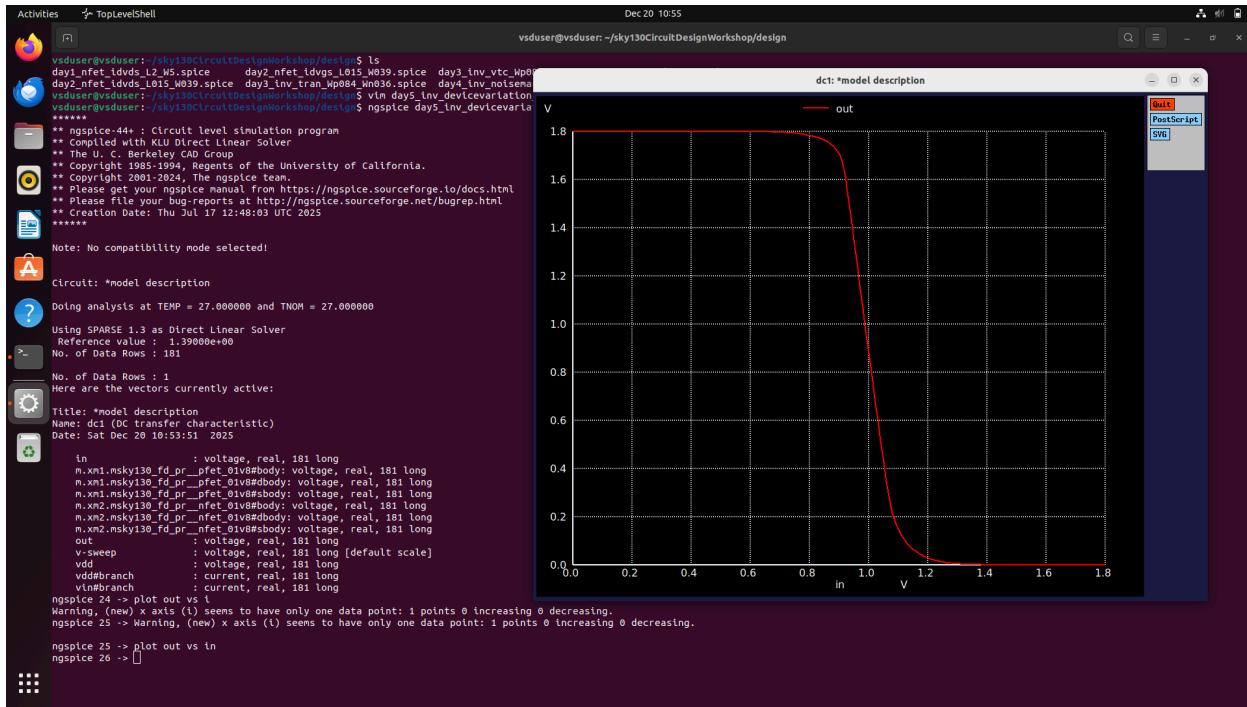
Cload out 0 0.8F
Vdd vdd 0 1.8V
Vin in 0 1.8V

*simulation commands
.op
.vdc Vtn 0 1.8 0.01
.control
run
list dci
display
.endc
.end

"day5_inv_devicevariation_wp7_wn042.spice" 35L, 391B

```

The simulation,



From the code, we can see that PMOS width is higher than NMOS, so it is strong PMOS and weak NMOS case. Hence the V_m will shift to the right.

