Verification Report

Bug Info:

1. Bug Report: Premature Assertion of rinc - Resolved by Changing wdata Transfer to Non-blocking

Bug Details:

- Bug Identification: Premature Assertion of rinc
- Issue Type: Timing Violation
- Severity: Moderate Bug Description:

1. **Symptoms:**
   - Premature assertion of rinc observed in certain simulation scenarios.
   - Violation of the expected timing relationship between rinc and the availability of rdata.
2. **Root Cause:**
   - Identified Cause: Sending wdata in Blocking Format during assignment.
   - Nature of the Issue**:** Blocking wdata assignment leading to premature assertion of rinc.

Technical Analysis:

1. **Blocking wdata Assignment:**
   - The use of blocking wdata assignment introduces delays in the completion of the write operation.
   - Premature assertion of rinc occurs before rdata is available, violating the expected timing.
2. **Verification Adjustment:**
   - Change the wdata assignment mechanism to a non-blocking format for faster completion.

Resolution:

1. **Solution:**
   - Modify the wdata assignment mechanism from blocking to non-blocking.

- This adjustment ensures that rinc is asserted only after the availability of rdata, aligning with the expected timing.

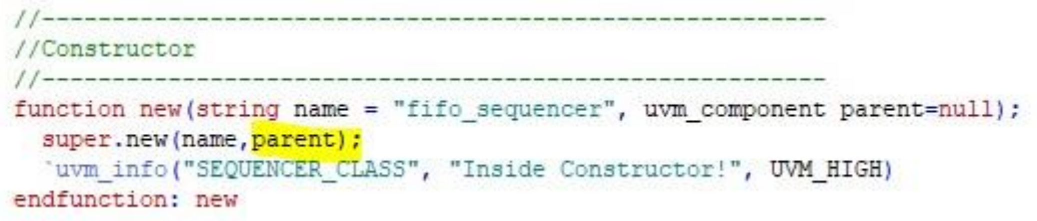
2. Bug Report: Incorrect UVM Hierarchy Due to Missing Parent Assignment in Sequencer Class

Bug Details:

- Bug Identification: Incorrect UVM Hierarchy
- Issue Type: Hierarchy Assignment
- Severity: Low

Bug Description:

1. **Symptoms:**
    - Incorrect UVM hierarchy observed in the simulation environment.
    - Components not organized as expected in the UVM hierarchy.
2. **Root Cause:**
    - Identified Cause: Missing parent assignment during component creation.
    - Nature of the Issue**:** The absence of the parent assignment resulted in an incorrect UVM hierarchy.
3. **Solution:**



```
//-------------------------------------------------------
//Constructor
//-------------------------------------------------------
function new(string name = "fifo_sequencer", uvm_component parent=null);
  super.new(name,parent);
  `uvm_info("SEQUENCER_CLASS", "Inside Constructor!", UVM_HIGH)
endfunction: new
```

3. Bug Report: Early Simulation Completion Before Full Reception of rdata

Bug Details:

- Bug Identification: Simulation Completing Prematurely.
- Issue Type**:** UVM Phase Mismanagement
- **Severity:** Medium Bug Description:

1. **Symptoms:**

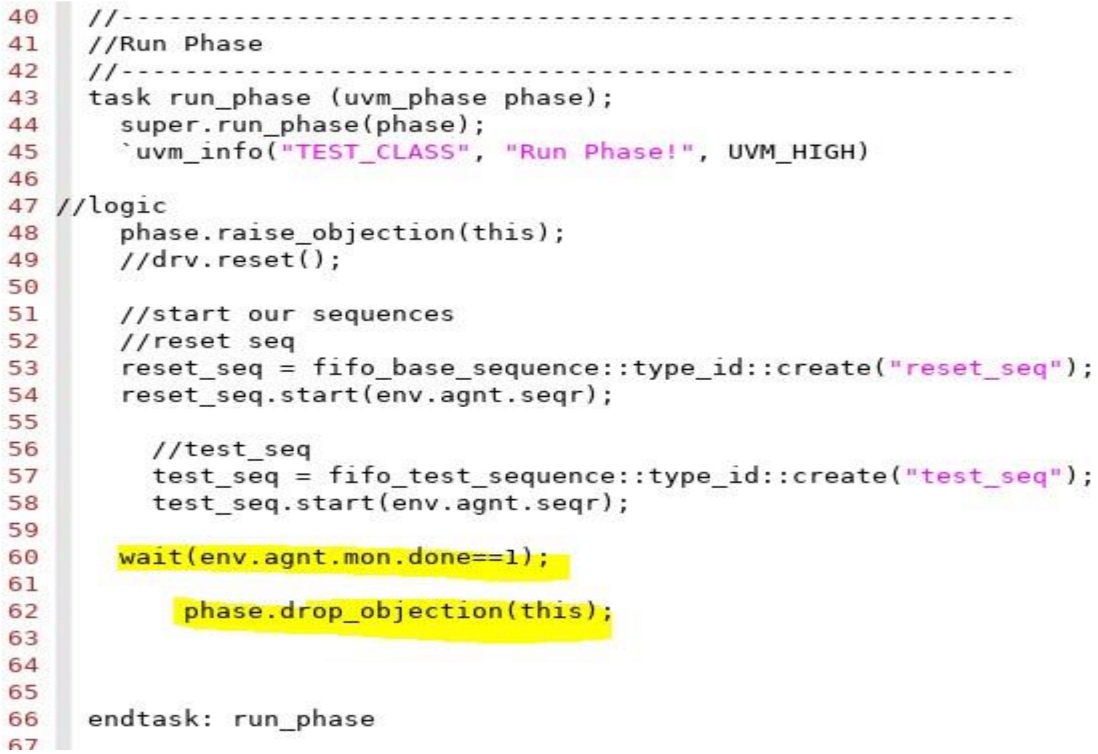
   - The simulation is completing before all rdata transactions are fully received.
   - The **drop_objection** in the test file is not called at the appropriate time.
   - The objection might be dropped too early or too late in the test phase.
   - This is causing simulation to complete before all the rdata is received.

2. **Root Cause:**

   - Identified Cause: Misplacement of drop_objection in the test file.
   - Nature of the Issue: The objection is not being dropped at the expected UVM phase.

3. **Solution:**

   - After adding wait resolved the issue.



```
  //----------------------------------------------------------
  //Run Phase
  //----------------------------------------------------------
  task run_phase (uvm_phase phase);
    super.run_phase(phase);
    `uvm_info("TEST_CLASS", "Run Phase!", UVM_HIGH)

//logic
    phase.raise_objection(this);
    //drv.reset();

    //start our sequences
    //reset seq
    reset_seq = fifo_base_sequence::type_id::create("reset_seq");
    reset_seq.start(env.agnt.seqr);

      //test_seq
      test_seq = fifo_test_sequence::type_id::create("test_seq");
      test_seq.start(env.agnt.seqr);

    wait(env.agnt.mon.done==1);

        phase.drop_objection(this);



  endtask: run_phase
```

4. Bug Report: Scoreboard Write and Read Timing Mismatch

Bug Details:

- Bug Identification: Scoreboard Timing Mismatch
- Issue Type: Data Timing Synchronization
- Severity**:** Medium

Bug Description:

1. **Symptoms:**
    - Timing mismatch observed between write (**wdata**) and read (**rdata**) operations in the scoreboard.
    - Incorrect comparison results due to asynchronous write and read timings.
2. **Root Cause:**
    - Identified Cause: Discrepancy in the timing of writing and reading data in the scoreboard.
    - Nature of the Issue**:** Asynchronous timing of **wdata** and **rdata** operations leading to comparison mismatches.
3. **Solution:**
    - Ensure synchronization of write (wdata) and read (rdata) timings in the scoreboard.
    - Implemented a mechanism to push wdata into the FIFO at the rising edge of wclk and pop rdata from the FIFO at the rising edge of rclk and when rinc is enabled resolved this issue.

5. Bug Report: Mismatch in rdata due to DQ Error

Bug Details:

Bug Identification:

- Issue Type: Data Mismatch
- Severity: Medium
- Frequency: Once in 20 Test Cases **Bug Description:**

1. **Symptoms:**
    - Mismatch observed in the **rdata** between two consecutive states (**n** and **n+1**).
    - **rdata** reads the same value in both states when it should be different.

2. **Root Cause:**
    - Identified Cause: Data Queue (DQ) error where rinc is not enabled when the clock is active.
    - Nature of the Issue**:** The absence of **rinc** during clocking resulted in a data miss in the FIFO.
3. **Solution**
    - Enable rinc with a non-blocking assignment during clocking to ensure synchronized read operations.
    - This resolves the DQ error and ensures that rdata is read when rinc is active.

6. Bug Report: Unique ID Generation Issue

Bug Details:

Bug Identification:

- Issue Type: Unique ID Generation
- Severity: Low
- Frequency**:** Occurred in Randomized Test Cases **Bug Description:**

1. **Symptoms:**
    - Continuous generation of unique IDs for consecutive direct test cases.
    - Again Reset and regeneration of unique IDs from 0 in randomized test cases.
    - Different values for the same **uniq_id** in randomized test cases.
2. **Root Cause:**
    - Identified Cause: Directly modifying uniq_id in the packet caused unexpected behavior during randomized test cases.
    - Nature of the Issue: The uniq_id was not maintained consistently, leading to discrepancies.
3. **Solution:**
    - Maintain a separate variable to store the uniq_id and pass this variable to both the sequence and update the actual pkt.uniq_id afterward.
    - This ensures consistent handling of uniq_id across direct and randomized test cases.

7. Bug Report: Simulation Looping Due to Mismatched Inputs

Bug Details:

Bug Identification:

- Issue Type: Simulation Looping
- Severity: Medium
- Frequency**:** Occurred when Actual Inputs Exceeded Expected Inputs

Bug Description:

1. **Symptoms:**
    - Continuous looping of the simulation.
    - The simulation did not complete within the expected time frame.
    - Logs or warnings indicating a mismatch between actual inputs and expected inputs.
2. **Root Cause:**
    - Identified Cause: The actual inputs provided to the testbench exceeded the expected inputs, causing a loop in the simulation.
    - Nature of the Issue**:** Testbench expected a certain number of inputs, but the actual stimuli provided were more than anticipated.
3. **Solution:**
    - Increase the expected inputs in the testbench to accommodate the actual inputs provided.
    - Ensure that the testbench can handle a larger set of inputs without entering an infinite loop.

8. Bug Report: Unhandled 'X' and 'Z' Values in Testbench Inputs

Bug Details:

Bug Identification:

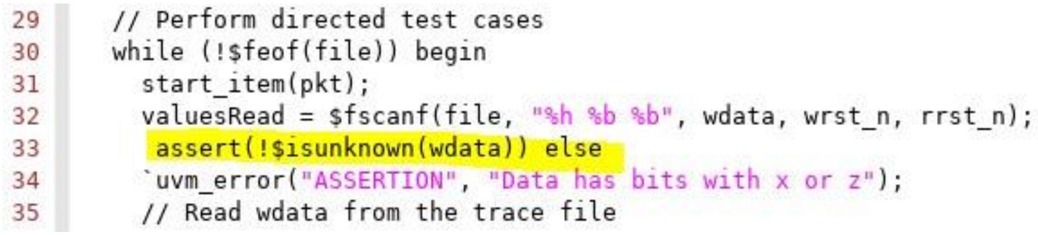
- Issue Type: Unhandled 'X' and 'Z' Values

- Severity: Medium
- Frequency**:** Detected When 'X' and 'Z' Values Were Present in Inputs **Bug**

Description:

1. **Symptoms:**
    - Testbench did not handle 'X' (unknown) and 'Z' (high impedance) values in inputs.
    - Simulation results may have inconsistencies due to unhandled 'X' and 'Z' values.
2. **Root Cause:**
    - Identified Cause: 'X' and 'Z' values in inputs were not handled explicitly in the testbench.
    - Nature of the Issue: Unhandled 'X' and 'Z' values could lead to unexpected behavior and inaccuracies in simulation results.
3. **Solution:**

- Explicitly handle 'X' and 'Z' values in the testbench while scanning the trace file.
- Add assertions to detect 'X' and 'Z' values and report errors for investigation.

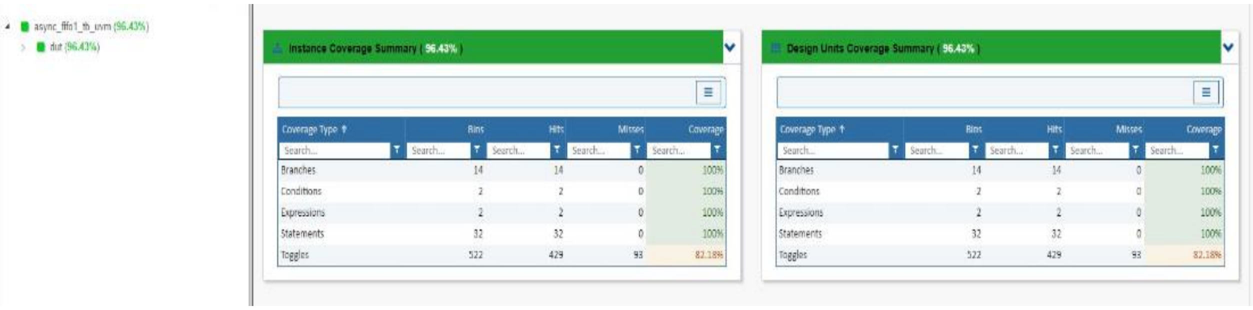


```
// Perform directed test cases
while (!$feof(file)) begin
  start_item(pkt);
  valuesRead = $fscanf(file, "%h %b %b", wdata, wrst_n, rrst_n);
   assert(!$isunknown(wdata)) else
  `uvm_error("ASSERTION", "Data has bits with x or z");
  // Read wdata from the trace file
```

Coverage Info:

```
Covergroup Coverage:
    Covergroups                      1       na        na    100.00%
        Coverpoints/Crosses          9       na        na         na
            Covergroup Bins         30       30         0    100.00%
----------------------------------------------------------------------------------------------------------
Covergroup                                             Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------------
 TYPE /async_fifo1_tb_uvm/fifo_coverage               100.00%        100           -   Covered
    covered/total bins:                                    30         30           -
    missing/total bins:                                     0         30           -
    % Hit:                                            100.00%        100           -
```



- async_fifo1_tb_uvm (96.43%)
  - dut (96.43%)

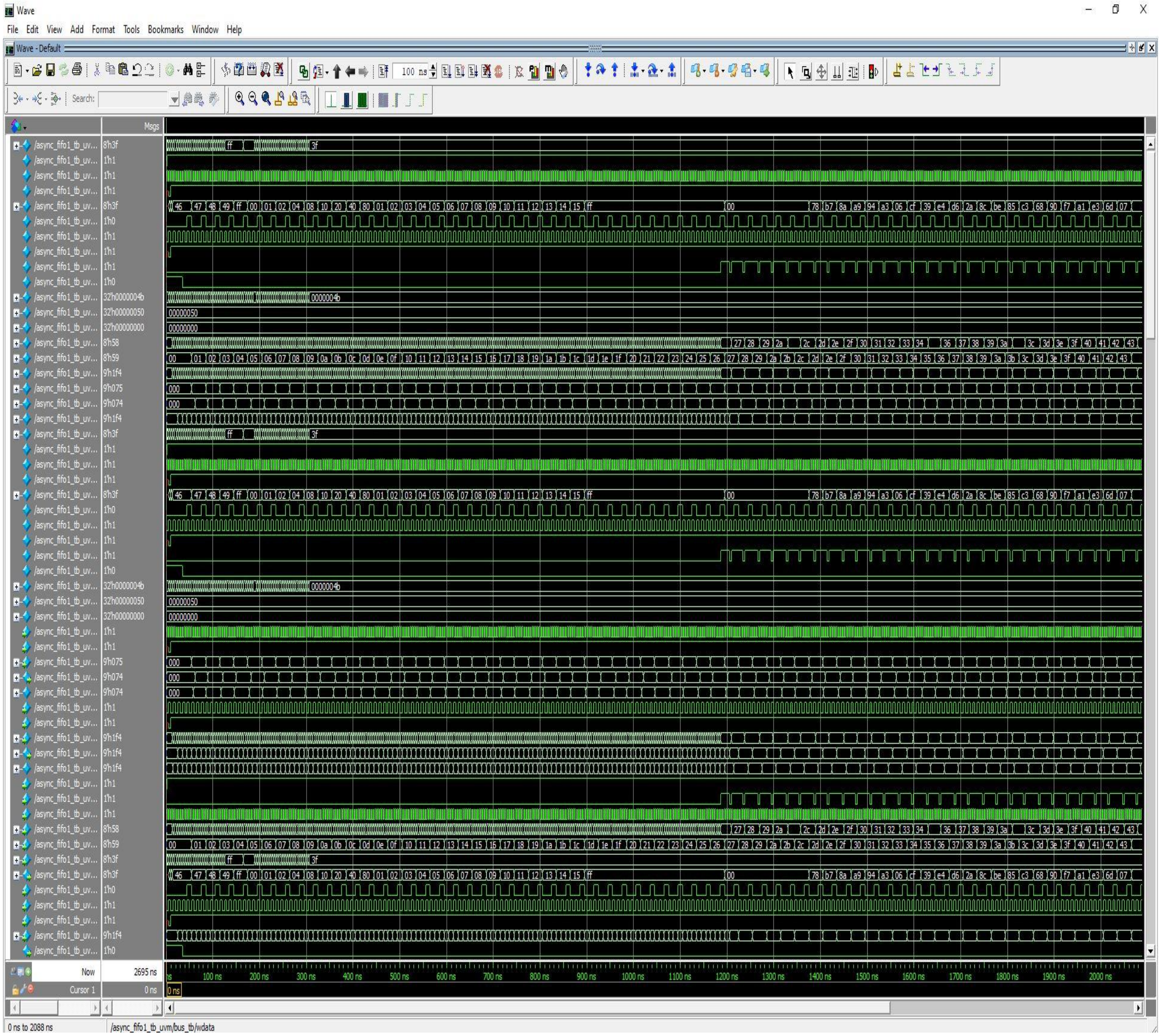
Instance Coverage Summary (96.43%)

Coverage Type	Bins	Hits	Misses	Coverage
Branches	14	14	0	100%
Conditions	2	2	0	100%
Expressions	2	2	0	100%
Statements	32	32	0	100%
Toggles	522	429	93	82.18%

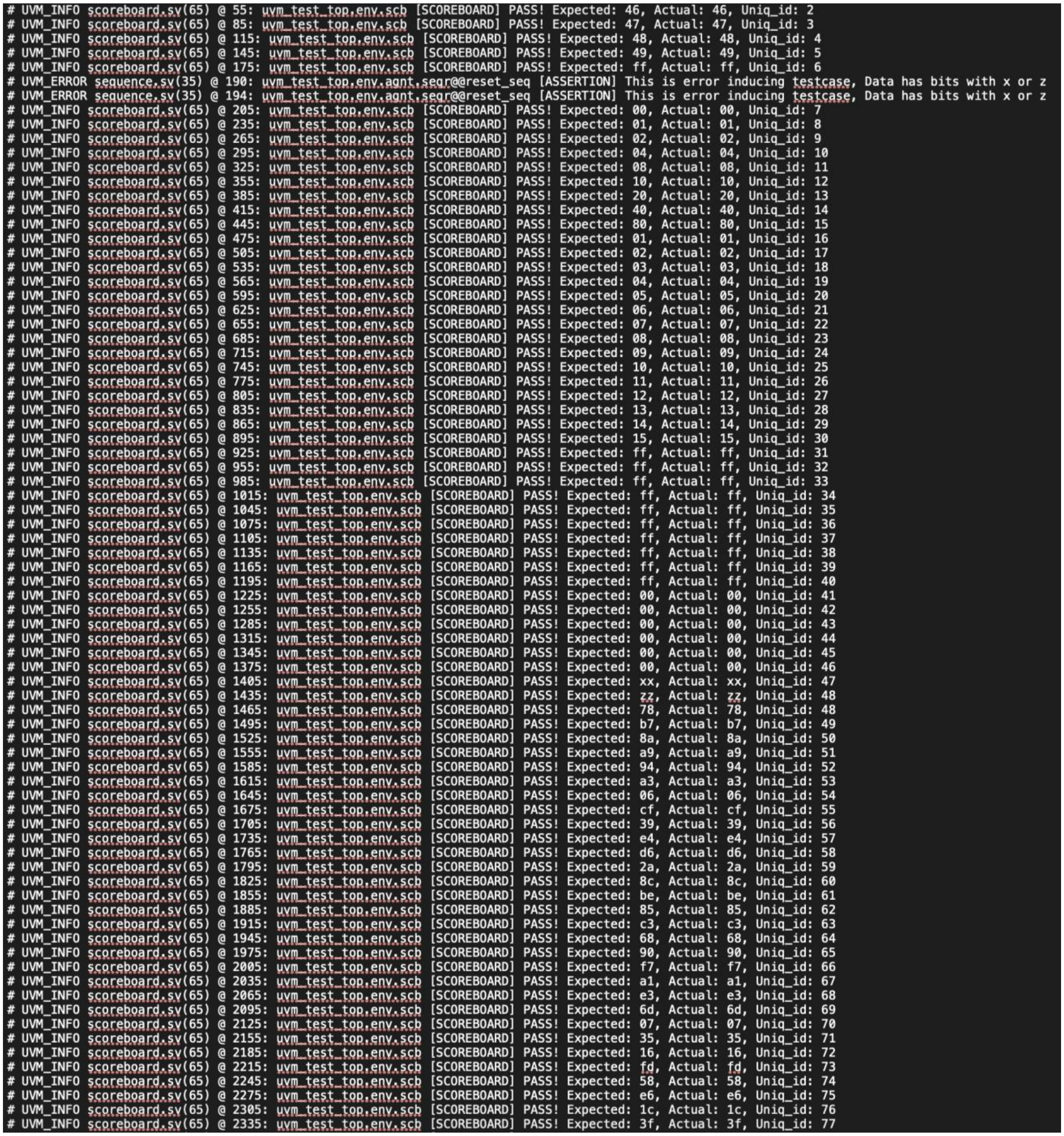
Design Units Coverage Summary (96.43%)

Coverage Type	Bins	Hits	Misses	Coverage
Branches	14	14	0	100%
Conditions	2	2	0	100%
Expressions	2	2	0	100%
Statements	32	32	0	100%
Toggles	522	429	93	82.18%

Waveform:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
100 ns
Msgs
/async_fifo1_tb_uv...
8'h3f
1'h1
1'h0
32'h0000004b
32'h00000050
32'h00000000
8'h58
8'h59
9'h1f4
9'h075
9'h074
Now 2695 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns 1000 ns 1100 ns 1200 ns 1300 ns 1400 ns 1500 ns 1600 ns 1700 ns 1800 ns 1900 ns 2000 ns
0 ns to 2088 ns
/async_fifo1_tb_uvm/bus_tb/wdata

Transcript:



```
# UVM_INFO scoreboard.sv(65) @ 55: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 46, Actual: 46, Uniq_id: 2
# UVM_INFO scoreboard.sv(65) @ 85: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 47, Actual: 47, Uniq_id: 3
# UVM_INFO scoreboard.sv(65) @ 115: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 48, Actual: 48, Uniq_id: 4
# UVM_INFO scoreboard.sv(65) @ 145: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 49, Actual: 49, Uniq_id: 5
# UVM_INFO scoreboard.sv(65) @ 175: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 6
# UVM_ERROR sequence.sv(35) @ 190: uvm_test_top.env.agnt.seqr@@reset_seq [ASSERTION] This is error inducing testcase, Data has bits with x or z
# UVM_ERROR sequence.sv(35) @ 194: uvm_test_top.env.agnt.seqr@@reset_seq [ASSERTION] This is error inducing testcase, Data has bits with x or z
# UVM_INFO scoreboard.sv(65) @ 205: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 7
# UVM_INFO scoreboard.sv(65) @ 235: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 01, Actual: 01, Uniq_id: 8
# UVM_INFO scoreboard.sv(65) @ 265: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 02, Actual: 02, Uniq_id: 9
# UVM_INFO scoreboard.sv(65) @ 295: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 04, Actual: 04, Uniq_id: 10
# UVM_INFO scoreboard.sv(65) @ 325: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 08, Actual: 08, Uniq_id: 11
# UVM_INFO scoreboard.sv(65) @ 355: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 10, Actual: 10, Uniq_id: 12
# UVM_INFO scoreboard.sv(65) @ 385: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 20, Actual: 20, Uniq_id: 13
# UVM_INFO scoreboard.sv(65) @ 415: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 40, Actual: 40, Uniq_id: 14
# UVM_INFO scoreboard.sv(65) @ 445: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 80, Actual: 80, Uniq_id: 15
# UVM_INFO scoreboard.sv(65) @ 475: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 01, Actual: 01, Uniq_id: 16
# UVM_INFO scoreboard.sv(65) @ 505: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 02, Actual: 02, Uniq_id: 17
# UVM_INFO scoreboard.sv(65) @ 535: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 03, Actual: 03, Uniq_id: 18
# UVM_INFO scoreboard.sv(65) @ 565: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 04, Actual: 04, Uniq_id: 19
# UVM_INFO scoreboard.sv(65) @ 595: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 05, Actual: 05, Uniq_id: 20
# UVM_INFO scoreboard.sv(65) @ 625: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 06, Actual: 06, Uniq_id: 21
# UVM_INFO scoreboard.sv(65) @ 655: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 07, Actual: 07, Uniq_id: 22
# UVM_INFO scoreboard.sv(65) @ 685: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 08, Actual: 08, Uniq_id: 23
# UVM_INFO scoreboard.sv(65) @ 715: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 09, Actual: 09, Uniq_id: 24
# UVM_INFO scoreboard.sv(65) @ 745: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 10, Actual: 10, Uniq_id: 25
# UVM_INFO scoreboard.sv(65) @ 775: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 11, Actual: 11, Uniq_id: 26
# UVM_INFO scoreboard.sv(65) @ 805: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 12, Actual: 12, Uniq_id: 27
# UVM_INFO scoreboard.sv(65) @ 835: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 13, Actual: 13, Uniq_id: 28
# UVM_INFO scoreboard.sv(65) @ 865: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 14, Actual: 14, Uniq_id: 29
# UVM_INFO scoreboard.sv(65) @ 895: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 15, Actual: 15, Uniq_id: 30
# UVM_INFO scoreboard.sv(65) @ 925: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 31
# UVM_INFO scoreboard.sv(65) @ 955: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 32
# UVM_INFO scoreboard.sv(65) @ 985: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 33
# UVM_INFO scoreboard.sv(65) @ 1015: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 34
# UVM_INFO scoreboard.sv(65) @ 1045: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 35
# UVM_INFO scoreboard.sv(65) @ 1075: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 36
# UVM_INFO scoreboard.sv(65) @ 1105: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 37
# UVM_INFO scoreboard.sv(65) @ 1135: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 38
# UVM_INFO scoreboard.sv(65) @ 1165: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 39
# UVM_INFO scoreboard.sv(65) @ 1195: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: ff, Actual: ff, Uniq_id: 40
# UVM_INFO scoreboard.sv(65) @ 1225: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 41
# UVM_INFO scoreboard.sv(65) @ 1255: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 42
# UVM_INFO scoreboard.sv(65) @ 1285: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 43
# UVM_INFO scoreboard.sv(65) @ 1315: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 44
# UVM_INFO scoreboard.sv(65) @ 1345: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 45
# UVM_INFO scoreboard.sv(65) @ 1375: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 00, Actual: 00, Uniq_id: 46
# UVM_INFO scoreboard.sv(65) @ 1405: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: xx, Actual: xx, Uniq_id: 47
# UVM_INFO scoreboard.sv(65) @ 1435: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: zz, Actual: zz, Uniq_id: 48
# UVM_INFO scoreboard.sv(65) @ 1465: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 78, Actual: 78, Uniq_id: 48
# UVM_INFO scoreboard.sv(65) @ 1495: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: b7, Actual: b7, Uniq_id: 49
# UVM_INFO scoreboard.sv(65) @ 1525: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 8a, Actual: 8a, Uniq_id: 50
# UVM_INFO scoreboard.sv(65) @ 1555: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: a9, Actual: a9, Uniq_id: 51
# UVM_INFO scoreboard.sv(65) @ 1585: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 94, Actual: 94, Uniq_id: 52
# UVM_INFO scoreboard.sv(65) @ 1615: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: a3, Actual: a3, Uniq_id: 53
# UVM_INFO scoreboard.sv(65) @ 1645: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 06, Actual: 06, Uniq_id: 54
# UVM_INFO scoreboard.sv(65) @ 1675: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: cf, Actual: cf, Uniq_id: 55
# UVM_INFO scoreboard.sv(65) @ 1705: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 39, Actual: 39, Uniq_id: 56
# UVM_INFO scoreboard.sv(65) @ 1735: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: e4, Actual: e4, Uniq_id: 57
# UVM_INFO scoreboard.sv(65) @ 1765: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: d6, Actual: d6, Uniq_id: 58
# UVM_INFO scoreboard.sv(65) @ 1795: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 2a, Actual: 2a, Uniq_id: 59
# UVM_INFO scoreboard.sv(65) @ 1825: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 8c, Actual: 8c, Uniq_id: 60
# UVM_INFO scoreboard.sv(65) @ 1855: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: be, Actual: be, Uniq_id: 61
# UVM_INFO scoreboard.sv(65) @ 1885: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 85, Actual: 85, Uniq_id: 62
# UVM_INFO scoreboard.sv(65) @ 1915: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: c3, Actual: c3, Uniq_id: 63
# UVM_INFO scoreboard.sv(65) @ 1945: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 68, Actual: 68, Uniq_id: 64
# UVM_INFO scoreboard.sv(65) @ 1975: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 90, Actual: 90, Uniq_id: 65
# UVM_INFO scoreboard.sv(65) @ 2005: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: f7, Actual: f7, Uniq_id: 66
# UVM_INFO scoreboard.sv(65) @ 2035: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: a1, Actual: a1, Uniq_id: 67
# UVM_INFO scoreboard.sv(65) @ 2065: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: e3, Actual: e3, Uniq_id: 68
# UVM_INFO scoreboard.sv(65) @ 2095: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 6d, Actual: 6d, Uniq_id: 69
# UVM_INFO scoreboard.sv(65) @ 2125: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 07, Actual: 07, Uniq_id: 70
# UVM_INFO scoreboard.sv(65) @ 2155: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 35, Actual: 35, Uniq_id: 71
# UVM_INFO scoreboard.sv(65) @ 2185: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 16, Actual: 16, Uniq_id: 72
# UVM_INFO scoreboard.sv(65) @ 2215: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: fd, Actual: fd, Uniq_id: 73
# UVM_INFO scoreboard.sv(65) @ 2245: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 58, Actual: 58, Uniq_id: 74
# UVM_INFO scoreboard.sv(65) @ 2275: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: e6, Actual: e6, Uniq_id: 75
# UVM_INFO scoreboard.sv(65) @ 2305: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 1c, Actual: 1c, Uniq_id: 76
# UVM_INFO scoreboard.sv(65) @ 2335: uvm_test_top.env.scb [SCOREBOARD] PASS! Expected: 3f, Actual: 3f, Uniq_id: 77
```