UVM_HIERARCHY

Top Level TB (tb_top):

Responsibilities:

- Instantiate the UVM testbench components.
- Connect the DUT to the testbench environment.
- Set up the simulation environment.
- Connect the DUT to the UVM components using appropriate interfaces.
- Control simulation flow.

Environment (env):

Responsibilities:

- Coordinate interactions between different agents.
- Manage global configuration and resources.
- Instantiate the UVM scoreboard and other analysis components.
- Manage and distribute test configuration.
- Instantiate and connect agents.
- Monitor the progress of the simulation.

Agent (fifo_agent):

Responsibilities:

- Combine the sequencer, driver, and monitor for a specific interface.
- Interface with the DUT.
- Instantiate the sequencer, driver, and monitor for a specific FIFO interface.
- Provide a unified interface to the DUT.

Driver (fifo_driver):

Responsibilities:

- Drive transactions onto the Asynchronous FIFO interface.
- Convert high-level transactions from the sequencer into low-level signals for the DUT.
- Translate transactions into signals compatible with the DUT interface.
- Drive these signals onto the FIFO interface.

Monitor (fifo_monitor):

Responsibilities:

- Monitor the transactions on the FIFO interface.
- Collect data for scoreboarding and analysis.
- Observe and capture relevant signals from the FIFO interface.
- Extract data for subsequent scoreboarding.

Sequencer (fifo_sequencer):
Responsibilities:

- Generate sequences of transactions for the Asynchronous FIFO.
- Control the flow of transactions to the respective agents.
- Create sequences for various write and read scenarios.
- Control the rate and order of transactions.
- Interface with the sequencer to manage the transaction flow.

Sequence (fifo_sequence):
Responsibilities

- Develop the test sequences.
- (fifo_base_sequence.sv and fifo_test_sequence.sv) that focus on both the reset sequence and functional test scenarios.

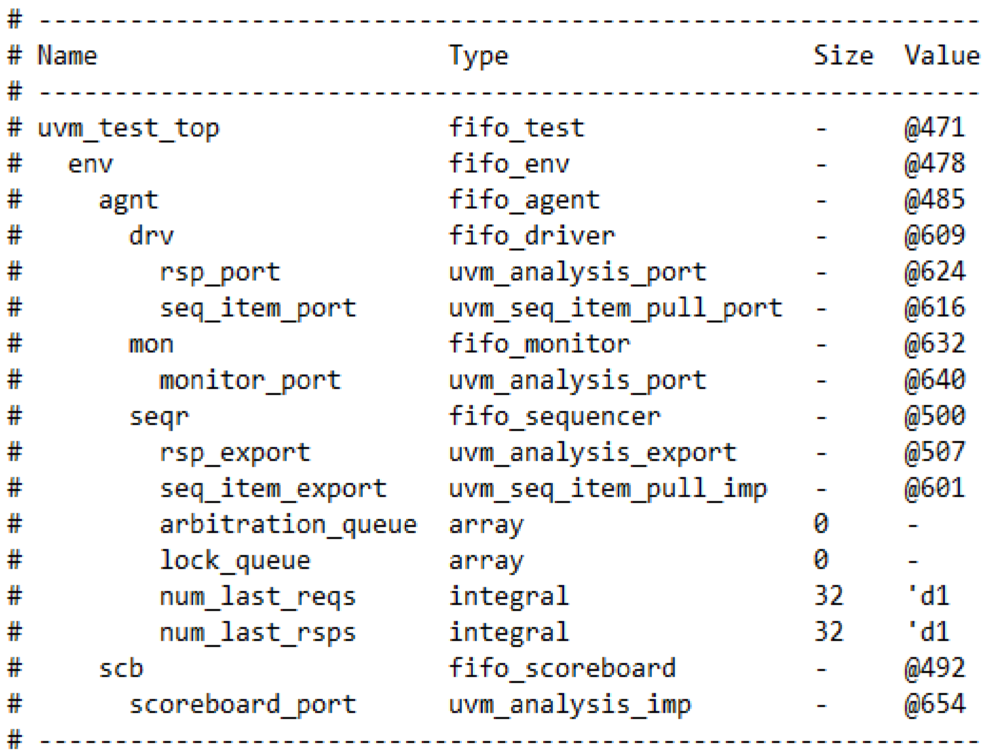
Sequence Item (fifo_sequence_item):
Responsibilities:

- A fifo_sequence_item represents a single transaction in the testbench. It encapsulates the data and control information that will be passed between different components of the testbench.
- Store transaction-specific data such as write data, read data, and unique identifiers.
- Implement randomization for generating diverse transactions during simulation.
- Randomly set values for parameters like write data, read data, and unique identifiers.
- Ensure the sequence item is compatible with the DUT's interface requirements.
- Contain fields corresponding to the signals on the DUT's interface.

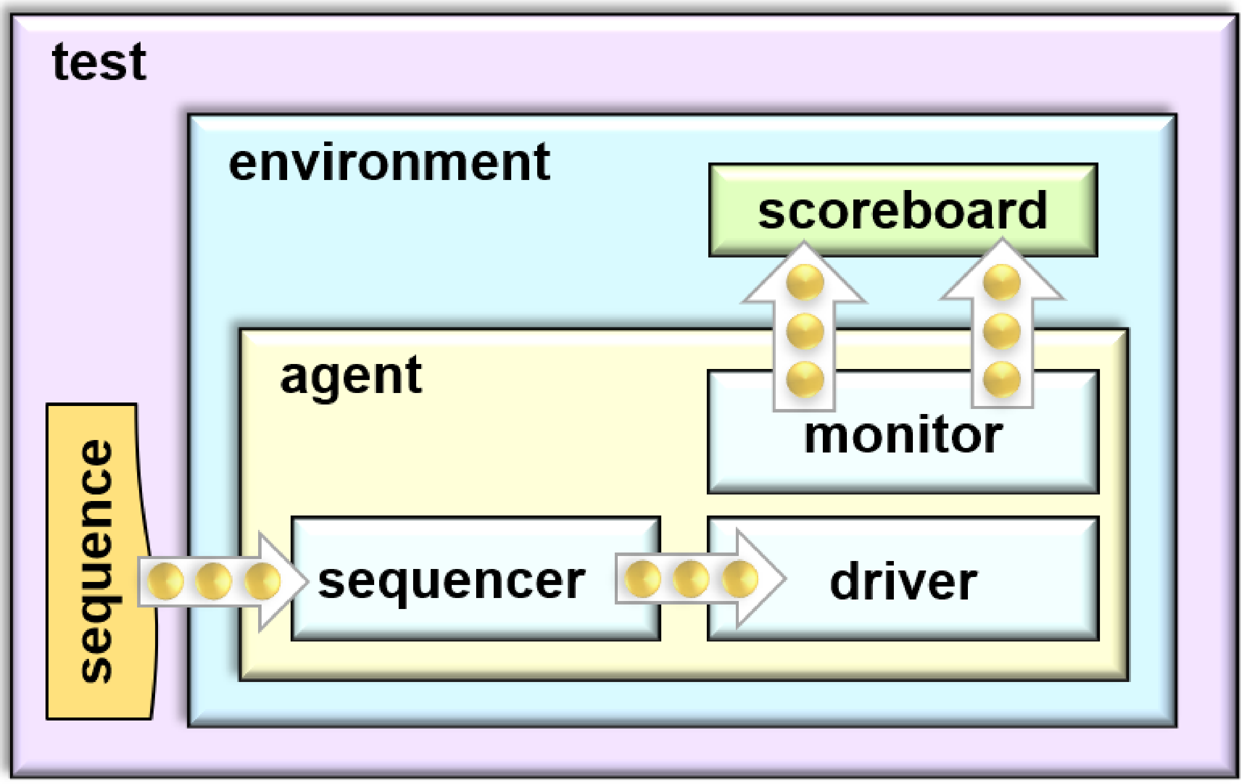
Scoreboard (fifo_scoreboard):
Responsibilities:

- Compare expected results with the actual results.
- Raise objections or report errors when discrepancies are found.
- Receive data from the monitor.
- Compare monitored data with expected results.
- Raise objections or report errors for further investigation.

Diagram:



```
# --------------------------------------------------------------
# Name                       Type                    Size  Value
# --------------------------------------------------------------
# uvm_test_top               fifo_test               -     @471
#   env                      fifo_env                -     @478
#     agnt                   fifo_agent              -     @485
#       drv                  fifo_driver             -     @609
#         rsp_port           uvm_analysis_port       -     @624
#         seq_item_port      uvm_seq_item_pull_port  -     @616
#       mon                  fifo_monitor            -     @632
#         monitor_port       uvm_analysis_port       -     @640
#       seqr                 fifo_sequencer          -     @500
#         rsp_export         uvm_analysis_export     -     @507
#         seq_item_export    uvm_seq_item_pull_imp   -     @601
#         arbitration_queue  array                   0     -
#         lock_queue         array                   0     -
#         num_last_reqs      integral                32    'd1
#         num_last_rsps      integral                32    'd1
#     scb                    fifo_scoreboard         -     @492
#       scoreboard_port      uvm_analysis_imp        -     @654
# --------------------------------------------------------------
```


test
environment
scoreboard
agent
monitor
sequence
sequencer
driver