**Testcases plan**

**Test Case 1: Basic Read and Write**

**Purpose:** Validate the fundamental functionality of the closed-page DDR5 design by executing simple read and write operations, ensuring correct data transfer.

**Test Case 2: Sequential Access within the Same Row**

**Purpose:** Confirm that sequential read and write operations within the same row exhibit the expected closed-page behaviour, minimizing latency for consecutive accesses.

**Test Case 3: Concurrent Access to Different Banks**

**Purpose:** Assess the concurrent access capability of the memory controller by issuing read and write requests to different banks simultaneously, ensuring efficient parallelism.

**Test Case 4: Row Precharge Timing**

**Purpose:** Evaluate the timing of row precharge commands following read or write operations to ensure optimal memory access and prevent unnecessary delays.

**Test Case 5: Row Hit and Miss Handling**

**Purpose:** Test the memory controller's response to row hits and misses, observing the activation, read or write, and precharge sequence for different scenarios.

**Test Case 6: Bank-Level Parallelism**

**Purpose:** Verify that the design effectively utilizes bank-level parallelism, issuing commands to multiple banks concurrently to maximize memory throughput.

**Test Case 7: Back-to-Back Operations**

**Purpose:** Assess the ability of the memory controller to handle consecutive read or write operations issued in rapid succession, checking for sustained performance.

**Test Case 8: Stress Testing**

**Purpose:** Apply stress to the system by continuously issuing read and write requests, evaluating the design's stability, error recovery mechanisms, and sustained performance.

**Test Case 9: Boundary Testing**

**Purpose:** Explore edge cases, such as maximum and minimum values for addresses and data, ensuring the closed-page DDR5 design handles extreme scenarios robustly.

**Test Case 10: Randomized Testing**

**Purpose:** Implement randomized testing with various sequences of read and write commands to uncover potential corner cases and enhance the design's resilience to unpredictable scenarios.

**Test Case 14: Command Pipelining**

**Purpose:** Verify the memory controller's support for command pipelining by issuing new commands while previous commands are still in progress, evaluating overall system efficiency.

**Test Case 15: CPU clock instruction**

**Purpose:**

Testcase 1: To test if there is new instruction on CPU clock after a long gap

Testcase 2: To test if there is new instruction on every CPU clock without any gap

Testcase3: Test for zero simulation/CPU clock time

Testcase4: Test for giving request at the maximum simulation time/CPU clock

**Test Case 16: Queue testing**

Testcase 1: Check for queue empty

Testcase 2: Check for queue full

Testcase3: Check for queue full and adding and removing request at the same time

Testcase4: Check for adding and removing request at the same time without queue is full

**Test Case 17: Output commands testing in DIMM cycle**

Testcase 1: what time can be the maximum for a request to enter so that on worst case all the command are getting executed in dimm cycle

Stall CPU request after that time