Verilog Assignment 7
Register Bank Report
Group 24

Gorantla Thoyajakshi - 21CS10026
Ashwin Prasanth - 21CS30009

- We made a register bank of 18 bits - R0 to R5, SP and PC
- There are three 5-bit inputs: **sr1, sr2 and dr** to denote the two source registers to read from, and the destination register to write to
- The data to write is taken as a 32-bit input: **wrData**
- The read data - from both ports, is obtained as two 32-bit outputs: **rData1 and rData2**
- Two signals are used - **write and reset**
    - **write** is used to initiate the writing into the register
    - **reset** is used to reset the value in all registers to 0

- The diagram is the same as the one made as part of the datapath