Group 24

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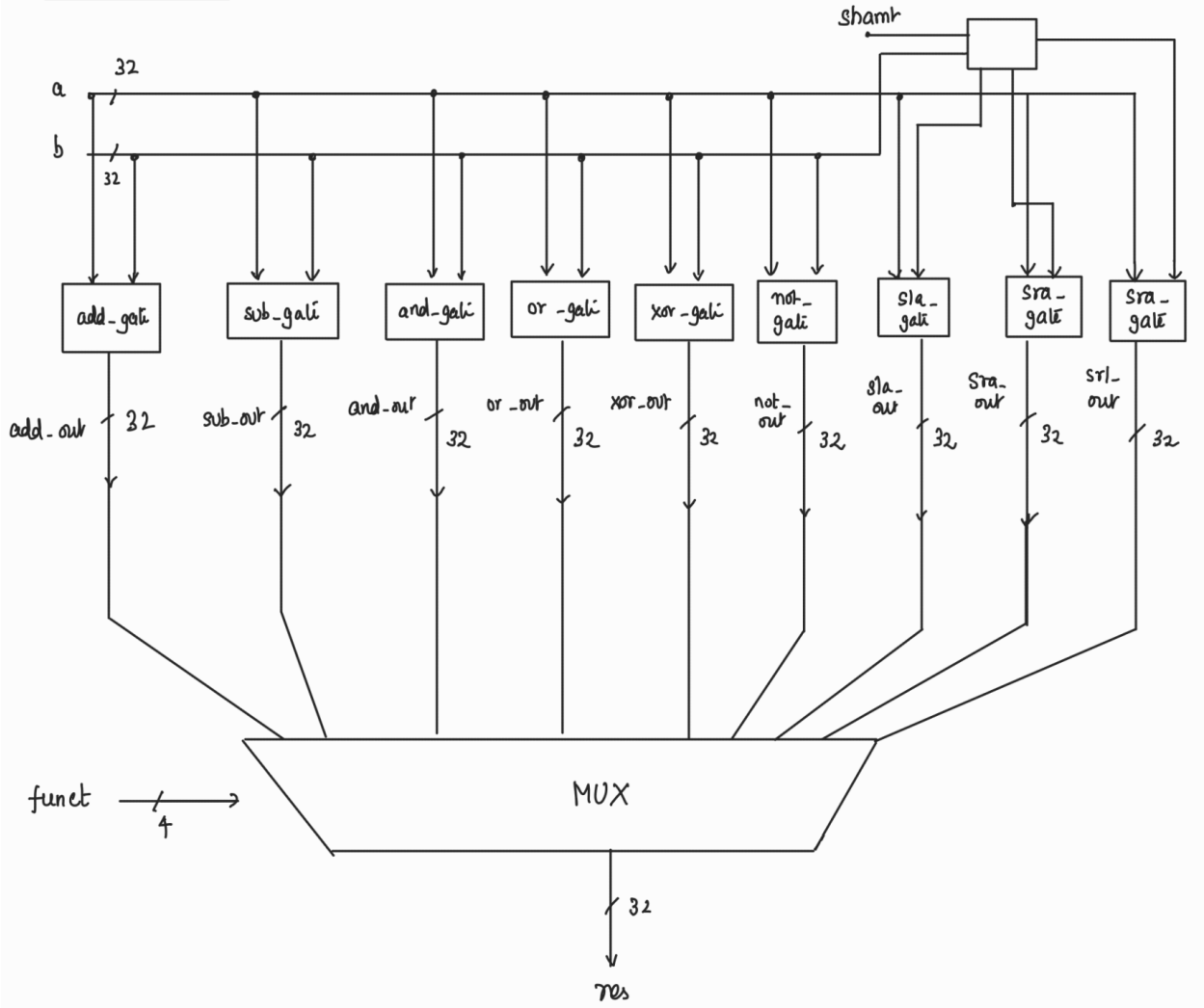
Computer Organization and Architecture Lab
Verilog Assignment 7 - Part 1

- We instantiated modules to support the following ALU operations:
    - ADD (Addition)
    - SUB (Subtraction)
    - AND (Bitwise And)
    - OR (Bitwise Or)
    - XOR (Bitwise Xor)
    - NOT (Bitwise Not of first input)
    - SLA (Arithmetic Left Shift)
    - SRA (Arithmetic Right Shift)
    - SRL (Logical Right Shift)
- Shift instructions were implemented as follows:
    - There is an optional 5 bit ‘shamt’ input
    - If ‘shamt’ is zero, then the shift amount is LSB of the 2nd input
    - Else, the shift amount is ‘shamt’

- Additionally, 4 bits are used to specify the required operation (‘funct’)
- Depending on the ‘funct’, using a ‘case’ block, the necessary output is obtained

ALU Module :


shamt
a
b
32
32
add_gati
sub_gali
and_gali
or_gali
xor_gali
not_gali
sla_gali
sra_gali
srl_gali
add_out
sub_out
and_out
or_out
xor_out
not_out
sla_out
sra_out
srl_out
32
funct
4
MUX
res