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Computer Organisation and Architecture Lab

Verilog Assignment 4

- We made three modules, booth,adder and subtractor
- In the module booth, Multiplicand and multiplier(both 8-bits) (M,Q)are taken as inputs along with clock and output the final multiplication result(16-bits) .Three intermediate registers,A , Q_reg and Q_1(which is assumed to be the Q-1) are initialized to 8-bit zeros, Q and zero respectively respectively.We instantiated adder, subtractor and shifter and then used them according to the Booth's multiplication algorithm as described below
  - (Q0Q-1) == 00 || 11, then do arithmetic right shift to (A.Q_reg.Q_1).
  - (Q0Q-1) == 01, then update A->A+M and then do arithmetic right shift to (A.Q_reg.Q_1).
  - (Q0Q-1) == 10, then update A->A-M and then do arithmetic right shift to (A.Q_reg.Q_1).

  After repeating the above steps 8 times (n times for a multiplier of n-bits), the final 16 bits of (A.Q_reg.Q_1) without the LSB is the output. To perform the arithmetic right shift, these steps were performed:
  - A = {A[7],A[7:1]}
  - Q_reg= {A[0],Q_reg[7:1]}
  - Q_1 = Q_reg[0]

- To implement **adder** module, we created a 4bit carry look ahead adder and cascaded two such units to get the sum of the 8-bit inputs

- To implement the **subtractor** module, we initially complemented the second input and then added it to the first input using the adder module.