

ML Computation Graph Operator Fission and Fusion

Ashwin Venkatram² and Gabriele Oliaro¹

¹Department of Computer Science, Carnegie Mellon University

²Department of Electrical and Computer Engineering, Carnegie Mellon University

Abstract

The execution of deep neural networks (DNNs) on modern hardware accelerators can be approached as a mapping problem from tensor operators to hardware-specific kernels. Previous works apply operator fusion for this mapping. Usually governed by human heuristics, operator fusion with greedy approach has always been suboptimal.

Traditionally, graph level operator fusion respects the boundary of each operator and is constrained to silicon-vendor provided library support for accelerated kernels.

We propose that operator fission to generate a primitive operator graph exposes inter-operator optimization opportunities for a global search algorithm. We hypothesize that TVM’s global genetic algorithm can find better fusion opportunities on a fissioned graph.

1 Introduction

The paper introduces a new method to optimize kernel mapping for tensor programs to enable efficient execution of deep neural networks (DNNs). The current bottleneck in DNN execution is the mapping of a high-level DNN representation to hardware-specific computations that can be executed on accelerators. Existing frameworks use heuristic based operator fusion to map DNN operators to hardware-specific kernels, but this approach has limitations. The paper proposes a new approach that applies operator fission to decompose tensor operators into basic primitives and then uses the global genetic search algorithm in TVM to find and codegen more performant kernels for GPU hardware execution.

1.1 Related works

The most relevant existing works focus can be divided into three groups, based on what they focus on:

- Kernel mapping: frameworks such as DNNFusion [19], or PyTorch 2.0 use rule-based fusion strategies to map

tensor operators to the best pick among a set of existing kernels. DNNFusion, for example, first classifies the operator in a DNN into five groups (One-to-One, One-to-Many, Many-to-Many, Reorganize, and Shuffle) depending on the relation between the input and output tensors. Then, it picks the One-on-One operators whose fusion has the potential to yield the best performance gains (fusion seed operators). Then, it tries to greedily fuse the successors and predecessors. Unlike these systems, our system uses a more systematic approach to optimize kernel mapping by first applying operator fission to decompose tensor operators into basic primitives and then using TVM [6] to perform the code generation that will discover an optimal kernel execution strategy for each graph of primitives.

- Graph optimization: Several existing frameworks in the ML compilation sphere perform optimizations by transforming a DNN’s computational graph. Systems such as TensorFlow [3], TensorRT [27], and MetaFlow [15], for example, apply graph transformation rules designed by domain experts. Other frameworks, such as TASO [14] and PET [29], attempt to generate the graph transformations automatically, and use backtracking search to apply the generated transformations. These works are complementary to our technique, as kernel mapping optimizations can be combined with existing graph-level optimizations. For instance, our system can use the graph transformations discovered by TASO to optimize the primitive graphs.
- Hardware-specific kernel generation: Frameworks such as Halide [18, 24], as well as many popular deep learning compilers, such as FlexTensor or TVM [6, 33], separate algorithm and schedule in two distinct components and automatically generate hardware-specific kernels for DNN computation. In particular, Halide proposes several strategies to discover highly optimized schedules, whereas TVM [7] uses a learning-based approach to predicting the cost of a schedule and discovering efficient

schedules in a pre-defined schedule space. Finally, Anzor [31] automatically generates schedule templates, resulting in more performant schedules than TVM. These techniques are also orthogonal to the optimizations proposed in our system; in fact, we directly use TVM and Anzor for generating high-performance kernels for a given set of primitives.

2 Design

2.1 Operator Fission

To represent the primitive operator computation graph, we use ONNX. ONNX is an open source format for AI models, and its operators. The operator fission pass implemented in Onnx GraphSurgeon takes an ONNX graph as input, performs operator fission leveraging ONNX primitives and outputs the modified computation graph.

As a case-study, we examine operator fission and associated speed-up for the Softmax operator. Other operators such as InstanceNorm, BatchNorm, etc can also leverage this innovation once proven.

For example, consider the commonly-used softmax operator, which converts a vector of numbers to a vector of probabilities:

$$\text{softmax}(x_i) = e^{x_i} / \sum_j e^{x_j} \quad (1)$$

The softmax operator includes three element-wise computations: the exponential function, a vector-wise aggregation (summation term in the denominator), and vector-wise broadcast (i.e., the scaling factor $s = 1/\sum_j e^{x_j}$ is used to compute all output elements). These components in softmax involve different degrees of parallelism and memory access patterns, making it challenging to generate a single high-performance kernel for softmax.

Understandably, the bottleneck is in the calculation of the summation term in the denominator. This also blocks any fusion opportunity with downstream nodes.

An example of Softmax operator fission is shown in Fig. 1.

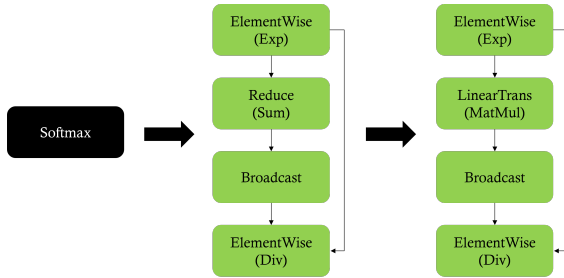


Figure 1: SoftMax Operator Fission

If fissioned, it is possible to generate a dedicated kernel for each of these components. However, this would be inef-

ficient due to high kernel launch overhead and unnecessary instantiations of intermediate results. We could obtain significant improvements by performing inter-operator fusion of the operator’s subcomponents at a finer-grained level if fusion opportunities exist with preceding or succeeding operator.

A key innovation in this operator fission is to treat the ReduceSum operator in Softmax as a linear transformation, MatMul operation. This enables potential fusion with downstream MatMul operations, if any. In the sub-graph example shown in Fig. 2, we explicitly include a MatMul node. The division operation can be performed later, while still preserving semantic equivalence, and the MatMuls can be horizontally fused as a single operation. The only overhead here is the insertion of Concat and Split node to access the desired tensors at a later stage.

Note that the Exp primitive operation within Softmax requires normalized input, and hence the primitive fissioned graph will show the ReduceMax operation as well.

With this approach, downstream code-gen can be efficient. HPC techniques can be leveraged for efficient data-forwarding from one CUDA kernel call to the next, and reduce system calls for DRAM allocations. We believe that TVM’s efficient code-gen backend will handle this.

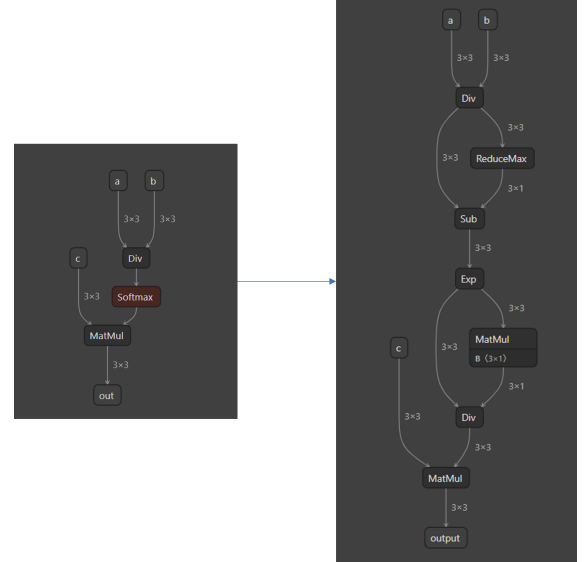


Figure 2: SoftMax Operator Fission

2.2 TVM Kernel Codegen

We leverage MetaSchedule [25], a probabilistic scheduler DSL developed in Tensor IR (TIR), to auto-generate high performing kernels for the computation graph and target GPU hardware. MetaSchedule accepts an ONNX graph input, lowers it to TIR schedule given pre-defined scheduling rules, and leverages Anzor backend to generate the best-performing schedule. The profiler then returns the latency measurement

of each kernel task as well as the end-to-end cost of model execution.

2.3 Experiment Setup

Platform Our evaluation is performed on Nvidia V100 GPU and A100 GPU. For Nvidia V100 GPU, we use an AWS p3 series instance [1] with Deep Learning AMI GPU PyTorch 1.13.0 (Ubuntu 20.04), which is equipped with a 8-core Intel Xeon CPU, a V100 16GB SXM GPU and CUDA 11.7.

We utilize ONNX-GraphSurgeon and TVM to implement this work and leverage TVM runtime to benchmark our results. We also compare with TensorRT where possible.

Workloads We selected to run our experience on the following test cases:

1. Linear Attention subgraph
2. Softmax-subgraph
3. Segformer model (resolution: 512x512) - a vision transformer for semantic segmentation

Note: All the DNNs are run with FP32 precision

2.4 Results

Linear Attention Subgraph TensorRT has particular optimizations targeting linear attention. For the QKV linear attention sub-block with Softmax, we observe a **2X speed-up over TensorRT**.

Softmax Subgraph Examining the Softmax subgraph in isolation, we observe a **1.11X speed-up over TensorRT**.

In both subgraph cases, we attribute the speedup observed to the two key innovations detailed in the earlier section. Primitive operator fission does expose better fusion search opportunities. Expressing ReduceSum as a Linear Transformation (MatMul) enables discovery of further fusion with upstream and downstream nodes for efficient kernel codegen by TVM Metaschedule.

Segformer ViT Vanilla Segformer TVM #tasks: 130 with mean E2E running time of 5ms. Op fission Segformer TVM #tasks: 119. We expect results of fewer tasks to complete faster than vanilla Segformer

3 Surprises and Lessons learned

We applied the learnings from this class to develop a generalized heuristic for operator fission and applied it to the Softmax testcase.

We believe this work has potential and can be extended to other operators as well.

4 Conclusion and Future Work

In conclusion, we show that operator fission to a primitive subgraph exposes more fusion opportunities with preceding and succeeding DL operators.

This can be automated and integrated into industry-grade deep learning compilers and systems stack.

Potential directions to extend this work:

1. Integrate operator fission pass from ONNX-GraphSurgeon (python) into TVM Relay and MLIR graph backend passes (C++)
2. Build on top of this proof-of-concept pass to create a generalized operator fission pass that can be applicable to other Reduction nodes such as InstanceNorm, BatchNorm, to name a few

5 Distribution of Work

50%-50% split between both team members.

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