



**Intel® Silicon Photonics SPTEMZZZFB
Power Management and Control IC
Preliminary Data Sheet
Intel Confidential
Revision 0.4**

Important Note:

All specifications, technical data, and other information contained in this document are preliminary in nature. All information is subject to change. Please contact Intel for more information.





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1 Overview

The SPTEMZZZFB ASIC is a power management and control IC designed and optimized for optical transceiver or optical engine applications. The ASIC includes multiple DACs designed to provide bias currents and control voltages to laser diodes, modulators, heaters, and other elements inside an optical transceiver or optical engine, multiple ADCs and amplifiers for use in detection circuitry for monitoring of photodetector current as well as supply and bias voltages, and a variety of digital interfaces for control of and communication with various ICs and other elements inside the optical module. The ASIC also includes a full on-chip microcontroller used to support communication with host equipment through I2C and other interfaces. The ASIC is designed in the TSMC 40nm embedded Flash ULP process.

2 Acronym Definitions

- O2E_IC - Optical to Electrical IC
- E2O_IC - Electrical to Optical IC
- PD: Photo Diode
- CDR: Clock Data Recovery
- ADC: Analog-to-Digital Converter
- DAC: Digital-to-Analog Converter
- LD: Laser Diode
- QBD: Quadrature Bias Diode
- LDO: Low DropOut voltage regulator
- FCCSP: Flip Chip Scale Package



3 Main Features

- Programmable current outputs for biasing lasers, temperature diodes, heaters, and other optical elements
- Built-in amplifiers for photodetector current and other monitoring circuits
- On-chip ADC to monitor various on-chip and external signals
- External voltage inputs for monitoring various supply voltages in the system
- Support for the following serial peripheral interfaces: I2C, I3C, UART, SPI, MDIO
- Tensilica LX7 based microcontroller to enable a firmware monitored optical transceiver system
- Supports on chip embedded flash up to 4MB
- Hardware initialized I2C for debug support (supported only in Test Mode)
- On-chip LDOs for digital core and ADC
- Brown out detector to alert the host of supply voltage drops
- Support to observe various internal node voltages in Analog Test Mode
- Support for on-die temperature sensors
- In-built memory: DRAM = 512K, IRAM = 512K
- Temperature range of -40C to 125C

4 Package Options

Available package options are described below:

Table 1 Packaging options

Name	Package
Die	Bare die (full functionality)
FCCSP	FCCSP – Flip-chip chip-scale package (subset of functionality)

5 Block Diagram

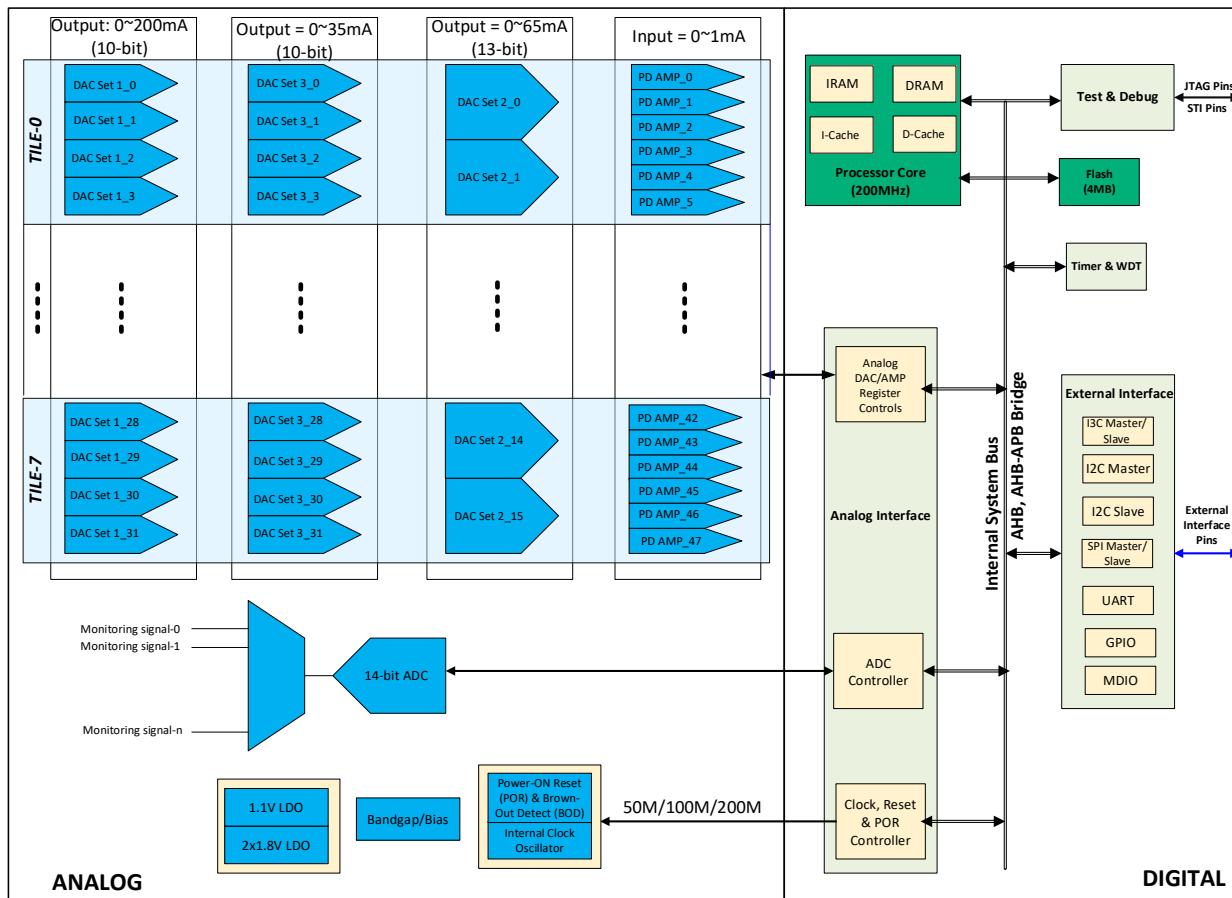


Figure 1 Microcontroller/PMIC Functional Block Diagram



6 Product Specifications

6.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings⁽¹⁾

Symbol	Parameter	Min	Max	Units
VDDA_2P5, VDD_2P5, VDDA_2P5_ADC, VDD_2P5_LDO	2.5V Supply Voltage	-0.3	2.75	V
VDDIO1, VDDIO2	Digital I/O Supply Voltage	-0.3	3.6	V
VDD_OP9 ⁽²⁾	Digital Core Supply Voltage	-0.3	1.21	V
VPP ⁽³⁾	Flash power supply	-0.3	5.6	V
VANA	Analog I/O pins	-0.3	VDD* ⁽⁴⁾	V
VDIG	Digital I/O pins	-0.3	VDD* ⁽⁴⁾	V
VHBM	ESD HBM on each pin		2000 ⁽⁵⁾	V
VCDM	ESD CDM on each pin		200 ⁽⁵⁾	V
VSTORAGE	Storage Temperature	-40	125	°C

⁽¹⁾Crossing Max/Min limits cause permanent damage. The Max/Min limits indicate stress limits only and performance is not guaranteed.

⁽²⁾Recommended to use internal LDO.

⁽³⁾Used for flash test only (otherwise should be kept as floating).

⁽⁴⁾Min/max voltage of the voltage domains of the pin in the pinlist.

⁽⁵⁾Design target, subject to change.



6.2 Recommended Operating Conditions

Table 3 Recommended operating conditions⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDDA_2P5, VDD_2P5, VDDA_2P5_ADC, VDD_2P5_LDO	2.5V Supply Voltage	2.42	2.5	2.58	V	At IC bump
VDDIO1, VDDIO2	Digital I/O Supply Voltage	-7%	3.3 or 2.5	+5%	V	At IC bump
VDD_0P9	Digital Core Supply Voltage	0.99	1.1	1.21	V	At IC bump, if supplied externally
V _{0p9vnoi,25vnoi, IOvnoi}	Dynamic Noise on 1.1V, 2.5V and VDDIO supply			30	mVpp	See Note (2).
F _{0p9vnoi, 25vnoi, 33vnoi}	Dynamic Noise frequency on 1.1V, 2.5V and VDDIO supply	50		100M	Hz	
VDD33ramp	3.3V supply ramp-up time	1			ms	
VDD_2P5_ramp	2.5V supply ramp-up time	1			ms	
VDD0p9ramp	1.1V supply ramp-up time	1			ms	If supplied externally
T _A	Operating temperature	-40		100	°C	
T _j	Junction temperature			125	°C	

⁽¹⁾Performance is measured under this condition.

⁽²⁾The ripple should not exceed the Min/Max limits.



6.3 Input/Output Threshold for Digital I/O

Table 4 DC electrical characteristics for all digital I/O

Symbol	Parameter	Min	Typ	Max	Units	Notes
VIH	Input HIGH level, input, and I/O pins	2.0		VDDIO1/2	V	Guaranteed logic HIGH level
VIL	Input LOW level, input, and I/O pins	VSS		0.8	V	Guaranteed logic LOW level
VOH	Output HIGH voltage	2.4		VDDIO1/2	V	VDD_OP9 = minimum, VDDIO1/2 = minimum, IOH = -2mA, -4mA, -8 mA, and -12mA
VOL	Output LOW voltage	VSS		0.4	V	VDD_OP9 = minimum, VDDIO1/2 = minimum, IOL = 2mA, 4mA, 8mA, and 12mA



6.4 Power Consumption Specifications

Table 5 Power consumption at normal operating conditions (bare die version)⁽¹⁾

Description	Typ	Max	Unit
Total 2.5V supply current for analog circuits with all DAC/PD OFF	18	21	mA
Total 2.5V supply current for analog circuits with "all" DAC/PD ON (Iout=0)	142	185	mA
Total 2.5V supply current for digital circuits (f=100MHz)	49	61	mA
Total power with "all" DAC/PD OFF	166	204	mW
Total power with "all" DAC/PD ON (Iout=0)	478	615	mW

⁽¹⁾Does not include VDDIO1/2 power

Table 6 Power consumption at normal operating conditions (FCCSP version)⁽¹⁾

Description	Typ	Max	Unit
Total 2.5V supply current for analog circuits with all DAC/PD OFF	18	21	mA
Total 2.5V supply current for analog circuits with "all" DAC/PD ON (Iout=0)	65	83	mA
Total 2.5V supply current for digital circuits (f=100MHz)	49	61	mA
Total power with "all" DAC/PD OFF	166	204	mW
Total power with "all" DAC/PD ON (Iout=0)	284	360	mW

⁽¹⁾Does not include VDDIO1/2 power



6.5 Electrical Specifications

All values specified are at “Recommended Operating Conditions” described in **Table 3 Recommended operating conditions⁽¹⁾** above.

Table 7 Analog peripheral summary

Symbol	Description	#/Tile	Total available for bare die	Total available for FCCSP package
DAC SET1	10-Bit DAC, 200mA current sink	4	32	8
DAC SET2	13-Bit DAC, 65mA current sink	2	16	8
DAC SET3	10-Bit DAC, 35mA current source	4	32	16
PD AMP	PD output sense amplifier	6	48	16
ADC	ADC for Voltage Sense (10 external differential input channels)	-	1	1
TEMP SENSE	External Temp Diode Support	-	4	4
CLOCK	Internal clock generator	-	1	1
POR & BOD	Power-ON-Reset and Brown-Out-Detect	-	1	1
LDO1P1	1.1V linear regulators (for internal usage)	-	1	1
LDO1P8	1.8V linear regulators (for external usage)		1	1



6.5.1 Digital-to-Analog Converter Set 1 (200mA current sink, 10-bit resolution)

DAC set 1 provides 200 mA current sink DAC outputs with 10-bit resolution. These outputs can be used to provide laser bias current or for other applications requiring a high-resolution DAC with characteristics as shown below.

Table 8 DAC Set 1 characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
BIT	Resolution	-			10	Bits
DNL	Differential Nonlinearity	Excludes +/-10% of min/max codes		± 0.2	± 0.5	LSB
INL	Integral Nonlinearity	Excludes +/-10% of min/max codes		± 2	± 5	LSB
VLD_DR	Dynamic Range	DAC code = 0		0.8		mA
		DAC code = 0x3FF, FS trim=0x0	200 ⁽¹⁾			
		DAC code = 0x3FF, FS trim=0x1	166			
		DAC code = 0x3FF, FS trim=0x2	126			
		DAC code = 0x3FF, FS trim=0x3	100			
VDAC	Voltage across DAC	-	0.4		2.5	V
VLD_noise	Noise laser driver current	DAC Programmed to 0xFF (BW = 0~2MHz).			200	μ Arms
Tsettling	Output settling time	95% of target current	2		20	μ S
I_LD	Current Consumption	Excludes output DAC current			650	μ A

⁽¹⁾10-bit resolution is guaranteed for 200 mA output setting.



6.5.2 Digital-to-Analog Converter Set 2 (65 mA current sink, 13-bit resolution)

DAC set 2 provides 65 mA current sink DAC outputs with 13-bit resolution, for use in modulator biasing, driving heating elements, or other applications requiring a very high-resolution DAC with characteristics as shown below.

Table 9 DAC Set 2 Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
BIT	Resolution	-			13	Bits
DNL	Differential Nonlinearity	Excludes +/-10% of min/max codes		± 0.2	± 0.5	LSB
INL	Integral Nonlinearity	Excludes +/-10% of min/max codes		± 2	± 5	LSB
VRH_DR	Dynamic Range	DAC code = 0		0.8		mA
		DAC code = 0x1FFF, FS trim=0x0	65 ⁽¹⁾			
		DAC code = 0x1FFF, FS trim=0x1	54			
		DAC code = 0x1FFF, FS trim=0x2	43			
		DAC code = 0x1FFF, FS trim=0x3	32			
VDAC	Voltage across DAC	-	0.4		2.5 ⁽²⁾	V
Tsettling	Output settling time	95% of target current	2		20	μ S
VRH_noise	Noise laser driver current	DAC programmed to 0xFF (BW = 0~2MHz).			4	μ Arms
I_RH	Current Consumption	Excludes output DAC current (From 2.5V supply)			1.5	mA

⁽¹⁾13-bit resolution is guaranteed for 65 mA output setting.

⁽²⁾DAC output ESD supports up to 2.5V. Product needs to ensure voltage at the DAC output does not cross the safe value.



6.5.3 Digital-to-Analog Converter Set 3 (35 mA current source, 10-bit resolution)

DAC set 3 provides 35 mA current source DAC outputs with 10-bit resolution, for use in modulator biasing or other applications requiring a high-resolution DAC with characteristics as shown below.

Table 10 DAC Set 3 Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
BIT	Resolution	-			10	Bits
DNL	Differential Nonlinearity	Excludes +/-10% of min/max codes		± 0.2	± 0.5	LSB
INL	Integral Nonlinearity	Excludes +/-10% of min/max codes		± 2	± 5	LSB
VQB_DR	Dynamic Range	DAC code = 0		0.8		mA
		DAC code = 0x3FF, FS trim=0x0	35 ⁽¹⁾			
		DAC code = 0x3FF, FS trim=0x1	29			
		DAC code = 0x3FF, FS trim=0x2	23			
		DAC code = 0x3FF, FS trim=0x3	17.5			
VDAC	Voltage across DAC output to ground	-			1.7	V
Tsettling	Output settling time	95% of target current	2		20	μS
VQB_noise	Noise laser driver current	DAC Programmed to 0xFF (BW = 0~2MHz).			30	μArms
I_QB	Current Consumption	Excludes output DAC current (From 2.5V supply)			0.8	mA

⁽¹⁾10-bit resolution is guaranteed for 35 mA output setting.



6.5.4 Transimpedance Amplifier

The transimpedance amplifier is designed for use in receiver/photodetector input power monitoring circuitry.

Table 11 Amplifier Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
lin	Input current	For switch setting 11	10		80	µA
		For switch setting 10	53		240	µA
		For switch setting 01	106		480	µA
		For switch setting 00	177		1000	µA
RTERM	Termination resistance	Gain setting 11		3670		Ohms
		Gain setting 10		1223		Ohms
		Gain setting 01		611.6		Ohms
		Gain setting 00		367		Ohms
Vin_cm	Amplifier input voltage range = lin x RTERM	Any switch setting	50		350	mV
GAIN	Fixed gain of the non-inverting amplifier	Any switch setting		4		V/V
Vout	Output voltage for monitoring through ADC	Any switch setting	100		1400	mV
Vnoise	Amplifier output noise voltage	Integrated across BW 0.5 Hz to 2MHz	103		155	uVrms
BW	Bandwidth	Any setting			2	MHz
VIN_OFFSET	Input referred offset	3 sigma	-3		3	mV
I_PD	Current Consumption	From 2.5V supply			1.9	mA



6.5.5 Analog-to-Digital Converter and Multiplexer

Table 12 ADC and Mux Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
BIT	Resolution			12		bits
VFS	Peak Single ended input signal	Referenced to ground		1.8		V
FCLK	ADC clock frequency			50		MHz
FRATE	Conversion rate			3.125		MSPS
DNL	Differential Nonlinearity	Excludes +/-10% of min/max codes			± 1	LSB
INL	Integral Nonlinearity	Excludes +/-10% of min/max codes			± 2	LSB
OFFS_ERROR	Offset error				± 6	LSB
GAIN_ERROR	Gain error				± 6	LSB
TOTAL_ERROR	Total unadjusted error				± 14	LSB
EXT_CHANNEL	External channel for signal monitoring					
	Latency					
	Current Consumption	2.5V supply			2	mA



6.5.6 Clock Oscillator

On-chip RC oscillator that provides clock to the digital core and ADC.

Table 13 Oscillator Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Units
OSC_FULL	Oscillator frequency before trimming ⁽²⁾		150	200	250	MHz
OSC_FULL_T	Oscillator frequency after trimming ⁽²⁾		190	200	210	MHz
OSC_HALF	Oscillator frequency before trimming ⁽³⁾		75	100	125	MHz
OSC_HALF_T	Oscillator frequency after trimming ⁽³⁾		95	100	105	MHz
DC_T	Duty Cycle after trimming		45		55	%
TJ	Pk-pk period jitter after trimming	At specified power supply noise			5	%
Tsett	Clock settling after trim code change				1	µs
ICLK	Supply current				1	mA

⁽¹⁾Internal oscillator operates in VDD_OP9 supply domain.

⁽²⁾POR for bare die version.

⁽³⁾POR for FCCSP version.



6.5.7 Power On Reset (POR) and Brown-Out Detector (BOD)

Power on Reset ensures that the chip is awakens properly to a predetermined state, and only when the external supply voltage reaches a valid state. Whenever the supply falls below the supported voltage, POR resets the chip again. BOD generates a Brown Out Signal that indicates that supply voltage to the IC is falling and the shutdown procedure, if any, should be initiated.

Table 14 POR & BOD Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Units
VSUP	Supply voltage used to generate POR control			VDDA_2P5		
VTH_POR_RISE	POR rising threshold		2	2.1	2.2	V
VTH_POR_FALL	POR falling threshold		1.8	1.9	2	V
VTH_POR_HYST	Threshold hysteresis			280		mV
TPOR_DELAY	Internal delay to POR while Supply is ramping up	10 mS using RC in analog & remaining 40mS using untrimmed Clock	50			ms
VTH_BOD_FALL	Brown out falling threshold		2.04	2.1	2.2	V
VTH_BOD_HYST	Threshold hysteresis			50		mV
IPOR	POR Current Consumption			400	600	µA
IBOD	BOD Current Consumption			400	600	µA

⁽¹⁾All the PMIC analog blocks meet parametric specifications for a supply voltage of 2.5V +/-10% and remain functional until the supply voltage falls to a level 100mV below the brown out threshold.

The BOD and POR thresholds are programmable through configuration bits.

Table 15 Definition of POR Falling Threshold Control⁽¹⁾

SI.No	por_fth_select<1:0> bits definition	POR falling threshold with respect to default
1	00	Default
2	01	Default Value +100 mV
3	10	Default Value -50mV
4	11	Default Value -100 mV

⁽¹⁾POR rising threshold is not affected by the value of por_fth_select<1:0> bits.



Table 16 Definition of BOD Falling Threshold Control

Sl.No	bod_th_select<1:0> bits Definition	BOD Threshold with respect to default
1	00	Default
2	01	+50 mV
3	10	-50 mV
4	11	-100 mV

6.5.8 1.1V Low Dropout Voltage Regulator

The 1.1V LDO supports the internal digital core functionalities.

Table 17 1.1V LDO Characteristics (Output pin = VDD_OP9)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VSUP	Supply voltage for the LDO			VDDA_2P5_LDO		
VOUT_PRE	Output voltage (pre trim)		1.05	1.1	1.2	V
VOUT_T	Output voltage (post trim)		1.09	1.1	1.12	V
IOUT	Output DC current				200	mA
TWAKE	Wake-up time after supply voltage is up				200	µs
LINE	Line regulation (Supply = 2.25V ~ 2.75V)				30	mV
LOAD	Load regulation					
PSRR	Power-supply rejection ratio				-15	dB



6.5.9 1.8V Low Dropout Voltage Regulator

The 1.8V LDO output is available for external use.

Table 18 1.8V LDO Characteristics (output pin = LDO_OUT_1P8)

Symbol	Parameter	Condition	Min	Typ	Max	Units
VSUP	Supply voltage for the LDO			VDDA_2P5		
VOUT_PRE	Output voltage (pre trim)		1.6	1.8	2.0	V
VOUT_T	Output voltage (post trim)		1.75	1.8	1.85	V
IOUT	Output DC current				25	mA
TWAKE	Wake-up time after supply voltage is up				200	µs
LINE	Line regulation (Supply = 2.25V ~ 2.75V)				30	mV
LOAD	Load regulation (current 0~25mA)				70	mV
PSRR	Power-supply rejection ratio				-15	dB



6.6 Digital Peripherals

This section describes digital peripheral overview and integration details. Micro-architecture, timing characteristics, and memory/register configuration details are described in the Digital Design Document.

Table 19 Digital Peripheral Summary

Symbol	Description	Size/#	Bare Die Version		FCCSP Version	
			VDDIO1/VSSIO1	VDDIO2/VSSIO2	VDDIO1/VSS	VDDIO2/VSS
I2C-M	I2C Master Instance	5	3	2	1	1
I2C-S	I2C Slave Instance	3	3	0	3	0
I3C-M	I3C Master Instance	1	1	0	1	0
I3C-S	I3C Slave Instance	1	1	0	1	0
SPI	SPI Master or Slave Instance	1 (4 Slave select lines)	1	0	1	0
UART	UART Instance	1	1	0	1	0
MDIO	MDIO Master Instance	1	1	0	1	0
GPIO	General Purpose I/O	32	24	8	17	6
UC	Micro-controller	1	1		1	
FLASH	Embedded flash	4MB	4MB		4MB	

Note 1: VDDIO1/2 supports 3.3V or 2.5V.

Note 2: Primary use for VDDIO1 is 3.3V and VDDIO2 is 2.5V.

6.6.1 I2C Master

Table 20 I2C Master power domain and Bare die / FCCSP allocation

I2C-Master	Power/Ground	Bare die	FCCSP
M0	VDDIO1/VSSIO1	Yes	Yes
M1	VDDIO1/VSSIO1	Yes	No
M2	VDDIO1/VSSIO1	Yes	No
M3	VDDIO2/VSSIO2	Yes	Yes
M4	VDDIO2/VSSIO2	Yes	No



6.6.2 Microcontroller block

This block contains the microcontroller and firmware image, with this it controls the internal and external components of the system. It contains the local instruction RAM (up to 512KB), local data RAM (up to 512KB) and Flash memory (up to 4MB) which helps in data/instruction/code storage. It also contains the bridge to move the information across different buses, watch dog timer and timers for micro controller usage.

6.6.3 External interface block

This block contains the various serial peripheral interfaces. The microcontroller ASIC supports:

- 5 I2C master instances
- 3 I2C slave instances
- 1 I3C master instance
- 1 I3C slave instance
- 1 SPI master with 4 slave select lines or be configured as 1 SPI slave with 4 slave select lines
- 1 UART instance
- 1 MDIO master instance

The PMIC/microcontroller ASIC can communicate with the external components of the system using these serial peripheral interfaces.

The I2C master is used to program the registers of the external chip. The I2C slave interface allows an external host to communicate with the on-chip micro controller. The SPI master/slave interface is used to communicate with a SPI slave/master in the system. MDIO and UART are used for performance monitoring and telemetry. An I3C interface is also provided for future extensibility. The IC also contains a GPIO block which can be used to capture the bootstrap values from the GPIO pin and also for external and internal interrupts or event indication.

6.6.4 System controller block

This block monitors the POR signals and releases the reset of the entire chip once the clock is running. It also contains pins/registers to control the boot related and low power features. The debug and test block contains circuitry related to the debug of the micro controller, flash and analog components. It also contains the logic required for the DFT of the PMIC ASIC.



6.6.5 GPIO

Table 21 GPIO power domain, FCCSP BGA routing, and defaults at power on

GPIO	Power/Ground	Bare die	FCCSP	At power ON
0	VDDIO1/VSSIO1 ⁽¹⁾	Yes	Yes	Pull-down
1	VDDIO1/VSSIO1	Yes	Yes	Pull-down
2	VDDIO1/VSSIO1	Yes	Yes	Pull-down
3	VDDIO1/VSSIO1	Yes	Yes	Pull-down
4	VDDIO1/VSSIO1	Yes	Yes	Pull-up
5	VDDIO1/VSSIO1	Yes	Yes	Pull-up
6	VDDIO1/VSSIO1	Yes	Yes	Pull-up
7	VDDIO1/VSSIO1	Yes	Yes	Pull-up
8	VDDIO1/VSSIO1	Yes	Yes	HiZ
9	VDDIO1/VSSIO1	Yes	Yes	HiZ
10	VDDIO1/VSSIO1	Yes	Yes	HiZ
11	VDDIO1/VSSIO1	Yes	Yes	HiZ
12	VDDIO1/VSSIO1	Yes	Yes	HiZ
13	VDDIO1/VSSIO1	Yes	Yes	HiZ
14	VDDIO1/VSSIO1	Yes	Yes	HiZ
15	VDDIO1/VSSIO1	Yes	Yes	HiZ
16	VDDIO1/VSSIO1	Yes	Yes	Pull-down
17	VDDIO2/VSSIO2 ⁽²⁾	Yes	Yes	Pull-down
18	VDDIO2/VSSIO2	Yes	Yes	Pull-up
19	VDDIO2/VSSIO2	Yes	Yes	Pull-up
20	VDDIO2/VSSIO2	Yes	Yes	HiZ
21	VDDIO2/VSSIO2	Yes	Yes	HiZ
22	VDDIO2/VSSIO2	Yes	Yes	HiZ
23	VDDIO2/VSSIO2	Yes	No	HiZ
24	VDDIO2/VSSIO2	Yes	No	HiZ
25	VDDIO1/VSSIO1	Yes	No	HiZ
26	VDDIO1/VSSIO1	Yes	No	HiZ
27	VDDIO1/VSSIO1	Yes	No	HiZ
28	VDDIO1/VSSIO1	Yes	No	HiZ
29	VDDIO1/VSSIO1	Yes	No	HiZ
30	VDDIO1/VSSIO1	Yes	No	HiZ
31	VDDIO1/VSSIO1	Yes	No	HiZ

⁽¹⁾VDDIO1/VSSIO1 primarily use 3.3V

⁽²⁾VDDIO2/VSSIO2 primarily use 2.5V



GPIO[0] & GPIO[1]:

At power ON/Reset, these pins should be set as logic 0/HIZ to set the IC at normal operating condition. If there is no external pull-up, at reset/after reset is released these pins will be set as input mode with internal pull-down enabled which later can be reconfigured by FW as needed. On PCB -- it is recommended to add weak pull-down (100k) to these pins or keep as HIZ.

GPIO[19]:

At power ON/Reset, this pin should be set as logic 1/HIZ to set the IC at normal operating condition. If there is no external pull-down, at reset/after reset is released this pin will be set as input mode with internal pull-up enabled which later can be reconfigured by FW as needed. On PCB -- it is recommended to add weak pull-up (100k) to this pin or keep as HIZ.

6.7 Pin Specifications

6.7.1 Ground Connections

The IC includes following ground options.

Table 22 Ground connections

Name	Description	Bare die	FCCSP
VSSA	Analog ground	Short with other grounds at substrate level	Shorted with other grounds at FCCSP package level (VSS)
VSSD	Digital ground	Short with other grounds at substrate level	Shorted with other grounds at FCCSP package level (VSS)
VSSIO	Digital I/O ground	Short with other grounds at substrate level	Shorted with other grounds at FCCSP package level (VSS)



6.7.2 Die Version for Engine

6.7.2.1 Die Information

- Die size – 7.63mm x 7.74mm
- Total number of bumps – 672
- Bump size – 90um with Polyimide opening of 63um
- Bump spacing – 282um

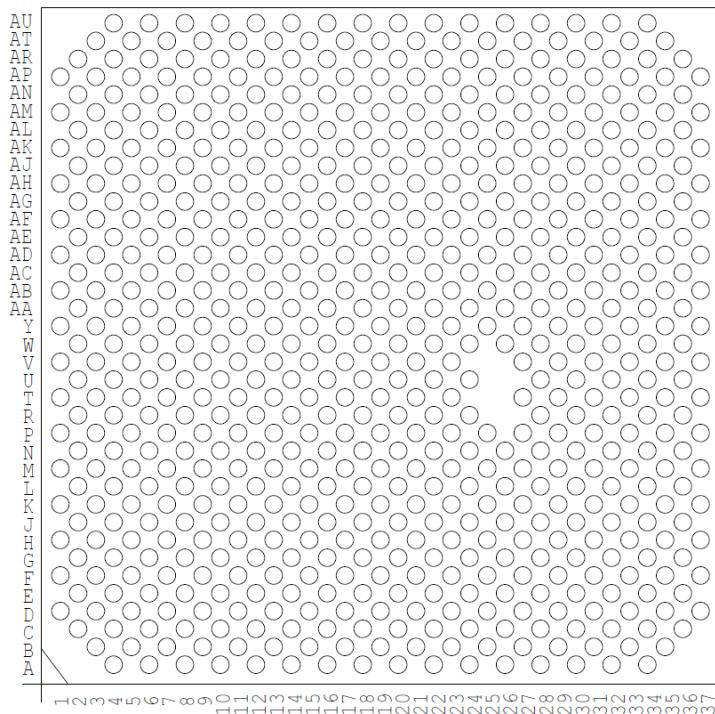
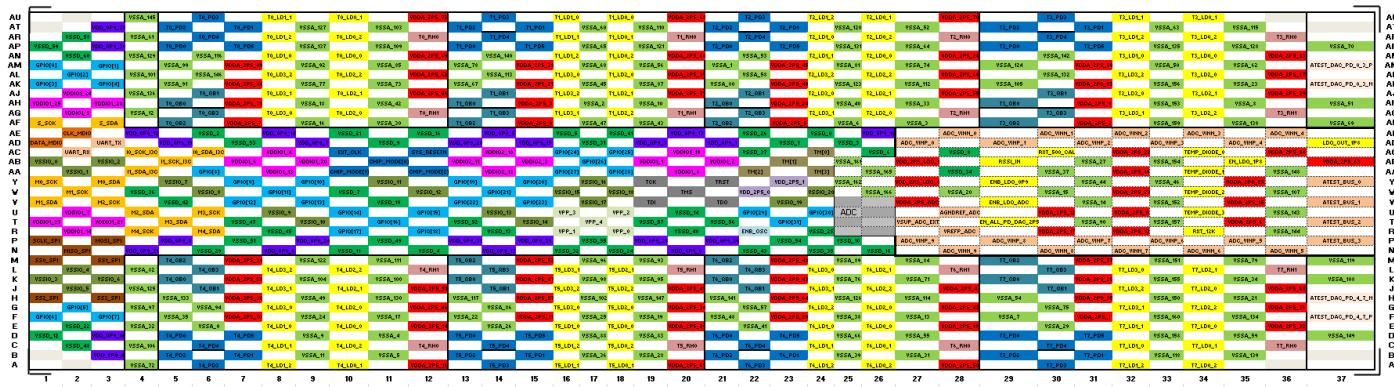


Figure 2 Bump map – bare die version [dead-bug view]



6.7.2.2 Pin List

Table 23 Pin list (bare die version)

Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
1	AE28	5562	4968	ADC_VINN_0		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
2	AE30	5958	4968	ADC_VINN_1		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
3	AE32	6354	4968	ADC_VINN_2		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
4	AE34	6750	4968	ADC_VINN_3		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
5	AE36	7146	4968	ADC_VINN_4		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
6	N36	7146	2592	ADC_VINN_5		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
7	N34	6750	2592	ADC_VINN_6		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
8	N32	6354	2592	ADC_VINN_7		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
9	N30	5958	2592	ADC_VINN_8		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
10	N28	5562	2592	ADC_VINN_9		Input	Analog	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
11	AD27	5364	4770	ADC_VINP_0		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
12	AD29	5760	4770	ADC_VINP_1		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
13	AD31	6156	4770	ADC_VINP_2		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
14	AD33	6552	4770	ADC_VINP_3		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
15	AD35	6948	4770	ADC_VINP_4		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
16	P35	6948	2790	ADC_VINP_5		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
17	P33	6552	2790	ADC_VINP_6		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
18	P31	6156	2790	ADC_VINP_7		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
19	P29	5760	2790	ADC_VINP_8		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
20	P27	5364	2790	ADC_VINP_9		Input	Analog	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs
21	U28	5562	3384	AGNDREF_ADC		Input	Analog	VDDA_2P5_ADC /VSSA		Negative Reference Voltage for ADC	L=30Z: Ferrite bead (e.g. BLM21PG300SN1D from Murata) between VSSA & AGNDREF_ADC
22	Y37	7344	3978	ATEST_BUS_0		Input/ Output	Analog	VDDA_2P5/ VSSA	-	Pin 0 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.	For wafer sort and bench test
23	V37	7344	3582	ATEST_BUS_1		Input/ Output	Analog	VDDA_2P5/ VSSA	-	Pin 1 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.	For wafer sort and bench test
24	T37	7344	3186	ATEST_BUS_2		Input/ Output	Analog	VDDA_2P5/ VSSA	-	Pin 2 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.	For wafer sort and bench test
25	P37	7344	2790	ATEST_BUS_3		Input/ Output	Analog	VDDA_2P5/ VSSA	-	Pin 3 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.	For wafer sort and bench test
26	AK37	7344	5958	ATEST_DAC_PD_0_3_N		Input/ Output	Analog	VDDA_2P5/ VSSA		Differential N Output pin- for ATEST but for DAC-PD Tiles 0-3. In production board, bring to a test point.	For wafer sort and bench test
27	AM37	7344	6354	ATEST_DAC_PD_0_3_P		Input/ Output	Analog	VDDA_2P5/ VSSA		Differential P Output pin- for ATEST but for DAC-PD Tiles 0-3. In production board, bring to a test point.	For wafer sort and bench test
28	H37	7344	1602	ATEST_DAC_PD_4_7_N		Input/ Output	Analog	VDDA_2P5/ VSSA		Differential N Output pin- for ATEST but for DAC-PD Tiles 4-7. In production board, bring to a test point.	For wafer sort and bench test
29	F37	7344	1206	ATEST_DAC_PD_4_7_P		Input/ Output	Analog	VDDA_2P5/ VSSA		Differential P Output pin- for ATEST but for DAC-PD Tiles 4-7. In production board, bring to a test point.	For wafer sort and bench test
30	AB11	2196	4374	CHIP_MODE[0]		Input	Digital	VDDIO1/VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.	Route to a test-point, 10k to ground
31	AA10	1998	4176	CHIP_MODE[1]		Input	Digital	VDDIO1/VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.	Route to a test-point, 10k to ground

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
32	AA12	2394	4176	CHIP_MODE[2]		Input	Digital	VDDIO1/VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.	Route to a test-point, 10k to ground
33	AE2	414	4968	CLK_MDIO		Output	Clock	VDDIO1/VSSIO		Clock for MDIO Interface. fmax = 2.5MHz CMOS input/output level = 0~VDDIO1.	1.5K pull-up resistor to VDDIO1 .
34	AD1	216	4770	DATA_MDIO		Input/ Output	Digital	VDDIO1/VSSIO		Data for MDIO Interface. fmax = 2.5MHz CMOS input/output level = 0~VDDIO1.	1.5K pull-up resistor to VDDIO1 .
35	Y29	5760	3978	ENB_LDO_OP9		Input	Digital	VDD_2P5_LDO/ VSSD	0 (100k to VSSD)	Power down (2.5V domain) of Digital Core LDO. When High, Internal Digital Core LDO is powered down. Internal to ASIC, this pin is pulled down using 100Kohm Resistor.	Tie 10K to ground
36	V29	5760	3582	ENB_LDO_ADC		Input	Digital	VDDA_2P5_ADC /VSSA	0 (100k to VSSD)	Power down (2.5V domain) of ADC LDO. When High, Internal ADC LDO is powered down. Internal to ASIC, this pin is pulled down using 100Kohm Resistor.	Tie 10K to ground
37	R22	4374	2988	ENB_OSC		Input	Digital	VDDIO1/VSSIO	0 (10k to VSSD)	Power Down Internal Oscillator. When High, internal oscillator is turned off. Clock needs to be supplied through EXT_CLK pin.	For wafer sort and bench test
38	T29	5760	3186	EN_ALL_PD_D AC_2P5		Input	Digital	VDDA_2P5/ VSSA	2.5V (100k to 2.5V)	Master enable control for all DAC and PD amplifiers. Enable=2.5V, Disable = 0V. When kept open firmware takes enable/disable control of the DAC/PD amplifier.	Route in module (first release)
39	AB35	6948	4374	EN_LDO_1P8		Input	Digital	VDD_2P5_LDO/ VSSD	0 (100k to VSSD)	Power down of 1.8V LDO. When Low, 1.8V LDO is powered down.	Route in module depending on product requirement
40	AC10	1998	4572	EXT_CLK		Input	Clock	VDDIO1/VSSIO		External clock. Used for testing. fmax = 400MHz. CMOS input/output level = 0~VDDIO1.	For wafer sort and bench test
41	AM1	216	6354	GPIO[0]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	10K resistor to ground at PCB level (to keep provision for override for test/debug)
42	Y9	1800	3978	GPIO[10]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
43	W8	1602	3780	GPIO[11]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
44	V7	1404	3582	GPIO[12]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
45	V9	1800	3582	GPIO[13]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
46	U10	1998	3384	GPIO[14]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
47	U12	2394	3384	GPIO[15]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
48	T11	2196	3186	GPIO[16]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
49	R10	1998	2988	GPIO[17]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
50	R12	2394	2988	GPIO[18]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
51	Y13	2592	3978	GPIO[19]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	10K resistor to VDDIO2 at PCB level (to keep provision for override for test/debug)
52	AM3	612	6354	GPIO[1]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	10K resistor to ground at PCB level (to keep provision for override for test/debug)
53	Y15	2988	3978	GPIO[20]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
54	W14	2790	3780	GPIO[21]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
55	V13	2592	3582	GPIO[22]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
56	V15	2988	3582	GPIO[23]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
57	AC16	3186	4572	GPIO[24]		Input/ Output	Digital	VDDIO2/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2.	External pull-up/pull-down depends on usage.
58	AC18	3582	4572	GPIO[25]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
59	AB17	3384	4374	GPIO[26]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
60	AA16	3186	4176	GPIO[27]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
61	AA18	3582	4176	GPIO[28]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
62	U22	4374	3384	GPIO[29]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
63	AL2	414	6156	GPIO[2]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
64	U24	4770	3384	GPIO[30]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
65	T23	4572	3186	GPIO[31]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
66	AK1	216	5958	GPIO[3]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
67	AK3	612	5958	GPIO[4]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
68	G2	414	1404	GPIO[5]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
69	F1	216	1206	GPIO[6]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
70	F3	612	1206	GPIO[7]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
71	AA6	1206	4176	GPIO[8]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
72	Y7	1404	3978	GPIO[9]		Input/ Output	Digital	VDDIO1/VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1.	External pull-up/pull-down depends on usage.
73	AC4	810	4572	IO_SCK_I3C		Input/ Output	Clock	VDDIO1/VSSIO		Clock for I3C Instance 0. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
74	AC6	1206	4572	IO_SDA_I3C		Input/ Output	Digital	VDDIO1/VSSIO		Data for I3C Instance 0. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
75	AB5	1008	4374	I1_SCK_I3C		Input/ Output	Clock	VDDIO1/VSSIO		Clock for I3C Instance 1. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
76	AA4	810	4176	I1_SDA_I3C		Input/ Output	Digital	VDDIO1/VSSIO		Data for I3C Instance 1. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
77	AD37	7344	4770	LDO_OUT_1P8		Input/ Output	Analog	VDD_2P5_LDO/ VSSA	-	Regulated voltage by on chip LDO for 1.8V supply voltage for external use.	Route with a thick trace. Add Cap - 10uF , 100nF , 1nF to VSSA closest to DUT .
78	Y1	216	3978	M0_SCK		Output	Clock	VDDIO1/VSSIO		I2C Master 0 clock. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
79	Y3	612	3978	M0_SDA		Input/ Output	Digital	VDDIO1/VSSIO		I2C Master 0 Data. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
80	W2	414	3780	M1_SCK		Output	Clock	VDDIO1/VSSIO		I2C Master 1 clock. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
81	V1	216	3582	M1_SDA		Input/ Output	Digital	VDDIO1/VSSIO		I2C Master 1 Data. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
82	V3	612	3582	M2_SCK		Output	Clock	VDDIO1/VSSIO		I2C Master 2 clock. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
83	U4	810	3384	M2_SDA		Input/ Output	Digital	VDDIO1/VSSIO		I2C Master 2 Data. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
84	U6	1206	3384	M3_SCK		Output	Clock	VDDIO2/VSSIO		I2C Master 3 clock. CMOS input/output level = 0~VDDIO2.	External pull-up=1K to VDDIO2
85	T5	1008	3186	M3_SDA		Input/ Output	Digital	VDDIO2/VSSIO		I2C Master 3 Data. CMOS input/output level = 0~VDDIO2.	External pull-up=1K to VDDIO2
86	R4	810	2988	M4_SCK		Output	Clock	VDDIO2/VSSIO		I2C Master 4 clock. CMOS input/output level = 0~VDDIO2.	External pull-up=1K to VDDIO2
87	R6	1206	2988	M4_SDA		Input/ Output	Digital	VDDIO2/VSSIO		I2C Master 4 Data. CMOS input/output level = 0~VDDIO2.	External pull-up=1K to VDDIO2
88	N2	414	2592	MISO_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Master In Slave Out for SPI Interface.	
89	P3	612	2790	MOSI_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Master Out Slave In for SPI Interface.	
90	AB29	5760	4374	RSSI_IN		Input	Analog	VDDA_2P5/ VSSA	-	Input to sink RSSI current from RXIC/TIA.	Route in module
91	R34	6750	2988	RXT_12K		Output	Analog	VDDA_2P5/ VSSA	-	External 12k+/-0.5 % tolerance resistor to ground for calibration and bias generation.	Route in module. Reduce routing cap <5pF cap with total routing resistance < 1ohms.
92	AC30	5958	4572	RXT_500_CAL		Output	Analog	VDDA_2P5/ VSSA	-	External 500-Ohm precision resistor for calibration of internal reference currents.	Add 0.5k+/-0.5% precision resistor to VSSA
93	P1	216	2790	SCLK_SPI		Output	Clock	VDDIO1/VSSIO		Clock for the SPI Interface.	
94	M1	216	2394	SS0_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Slave select line for SPI.	Route in module
95	M3	612	2394	SS1_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Slave select line for SPI.	Route in module
96	H1	216	1602	SS2_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Slave select line for SPI.	Route in module
97	H3	612	1602	SS3_SPI		Input/ Output	Digital	VDDIO1/VSSIO		Slave select line for SPI.	Route in module
98	AC12	2394	4572	SYS_RESETN		Input	Digital	VDDIO1/VSSIO		External system reset.	Route to module
99	AF1	216	5166	S_SCK		Input/ Output	Clock	VDDIO1/VSSIO		I2C Interface clock for the slave. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1
100	AF3	612	5166	S_SDA		Input/ Output	Digital	VDDIO1/VSSIO		I2C Interface data for the slave. CMOS input/output level = 0~VDDIO1.	External pull-up=1K to VDDIO1

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
101	AN10	1998	6552	T0_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 0 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
102	AU10	1998	7344	T0_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 0 (200mA)	
103	AR10	1998	6948	T0_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 0 (200mA)	
104	AN8	1602	6552	T0_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 1 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
105	AU8	1602	7344	T0_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 1 (200mA)	
106	AR8	1602	6948	T0_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 1 (200mA)	
107	AG10	1998	5364	T0_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 2 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
108	AJ10	1998	5760	T0_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 2 (200mA)	
109	AL10	1998	6156	T0_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 2 (200mA)	
110	AG8	1602	5364	T0_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 3 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
111	AJ8	1602	5760	T0_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 3 (200mA)	
112	AL8	1602	6156	T0_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 3 (200mA)	
113	AP5	1008	6750	T0_PD0		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 0 (1mA)	Route in module
114	AT7	1404	7146	T0_PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 1 (1mA)	Route in module
115	AT5	1008	7146	T0_PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 2 (1mA)	Route in module
116	AU6	1206	7344	T0_PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 3 (1mA)	Route in module
117	AR6	1206	6948	T0_PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 4 (1mA)	Route in module
118	AP7	1404	6750	T0_PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 5 (1mA)	Route in module
119	AH5	1008	5562	T0_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 0 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
120	AJ6	1206	5760	T0_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 1 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
121	AF5	1008	5166	T0_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 2 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
122	AG6	1206	5364	T0_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 3 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
123	AR12	2394	6948	T0_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current driver 0 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
124	AG12	2394	5364	T0_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current driver 1 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
125	AU18	3582	7344	T1_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 4 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
126	AR18	3582	6948	T1_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 4 (200mA)	
127	AN18	3582	6552	T1_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 4 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
128	AU16	3186	7344	T1_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 5 (200mA)	
129	AR16	3186	6948	T1_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 5 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
130	AN16	3186	6552	T1_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 5 (200mA)	
131	AL18	3582	6156	T1_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 6 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
132	AJ18	3582	5760	T1_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 6 (200mA)	
133	AG18	3582	5364	T1_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 6 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
134	AL16	3186	6156	T1_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 7 (200mA)	
135	AG16	3186	5364	T1_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 7 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
136	AJ16	3186	5760	T1_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 7 (200mA)	
137	AP13	2592	6750	T1_PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 6 (1mA)	Route in module
138	AT15	2988	7146	T1_PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 7 (1mA)	Route in module
139	AT13	2592	7146	T1_PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 8 (1mA)	Route in module
140	AU14	2790	7344	T1_PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 9 (1mA)	Route in module
141	AR14	2790	6948	T1_PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 10 (1mA)	Route in module
142	AP15	2988	6750	T1_PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 11 (1mA)	Route in module

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
143	AH13	2592	5562	T1_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 4 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
144	AJ14	2790	5760	T1_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 5 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
145	AF13	2592	5166	T1_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 6 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
146	AG14	2790	5364	T1_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 7 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
147	AR20	3978	6948	T1_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 2 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
148	AG20	3978	5364	T1_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 3 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
149	AN26	5166	6552	T2_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 8 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
150	AU26	5166	7344	T2_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 8 (200mA)	
151	AR26	5166	6948	T2_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 8 (200mA)	
152	AR24	4770	6948	T2_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 9 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
153	AN24	4770	6552	T2_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 9 (200mA)	
154	AU24	4770	7344	T2_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 9 (200mA)	
155	AG26	5166	5364	T2_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 10 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
156	AJ26	5166	5760	T2_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 10 (200mA)	
157	AL26	5166	6156	T2_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 10 (200mA)	
158	AJ24	4770	5760	T2_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 11 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other
159	AG24	4770	5364	T2_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 11 (200mA)	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
160	AL24	4770	6156	T2_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 11 (200mA)	destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
161	AP21	4176	6750	T2_PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 12 (1mA)	Route in module
162	AT23	4572	7146	T2_PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 13 (1mA)	Route in module
163	AT21	4176	7146	T2_PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 14 (1mA)	Route in module
164	AU22	4374	7344	T2_PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 15 (1mA)	Route in module
165	AR22	4374	6948	T2_PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 16 (1mA)	Route in module
166	AP23	4572	6750	T2_PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 17 (1mA)	Route in module
167	AH21	4176	5562	T2_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 8 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
168	AJ22	4374	5760	T2_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 9 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
169	AF21	4176	5166	T2_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 10 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
170	AG22	4374	5364	T2_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 11 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
171	AR28	5562	6948	T2_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 4 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
172	AG28	5562	5364	T2_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 5 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
173	AN34	6750	6552	T3_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 12 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
174	AU34	6750	7344	T3_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 12 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
175	AR34	6750	6948	T3_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 12 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
176	AN32	6354	6552	T3_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 13 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other
177	AU32	6354	7344	T3_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 13 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
178	AR32	6354	6948	T3_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 13 (200mA)	destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
179	AL34	6750	6156	T3_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 14 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
180	AJ34	6750	5760	T3_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 14 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
181	AG34	6750	5364	T3_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 14 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
182	AJ32	6354	5760	T3_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 15 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
183	AG32	6354	5364	T3_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 15 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
184	AL32	6354	6156	T3_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 15 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
185	AP29	5760	6750	T3 PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 18 (1mA)	Route in module
186	AT31	6156	7146	T3 PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 19 (1mA)	Route in module
187	AT29	5760	7146	T3 PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 20 (1mA)	Route in module
188	AU30	5958	7344	T3 PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 21 (1mA)	Route in module
189	AR30	5958	6948	T3 PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 22 (1mA)	Route in module
190	AP31	6156	6750	T3 PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 23 (1mA)	Route in module
191	AH29	5760	5562	T3_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 12 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
192	AJ30	5958	5760	T3_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 13 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
193	AF29	5760	5166	T3_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 14 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
194	AG30	5958	5364	T3_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 15 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
195	AR36	7146	6948	T3_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 6 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
196	AG36	7146	5364	T3_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 7 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
197	E10	1998	1008	T4_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 16 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
198	A10	1998	216	T4_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 16 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
199	C10	1998	612	T4_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 16 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
200	E8	1602	1008	T4_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 17 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
201	C8	1602	612	T4_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 17 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
202	A8	1602	216	T4_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 17 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
203	G10	1998	1404	T4_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 18 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
204	J10	1998	1800	T4_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 18 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
205	L10	1998	2196	T4_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 18 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
206	G8	1602	1404	T4_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 19 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
207	J8	1602	1800	T4_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 19 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
208	L8	1602	2196	T4_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 19 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
209	D5	1008	810	T4 PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 24 (1mA)	Route in module
210	B7	1404	414	T4 PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 25 (1mA)	Route in module
211	B5	1008	414	T4 PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 26 (1mA)	Route in module
212	A6	1206	216	T4 PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 27 (1mA)	Route in module
213	C6	1206	612	T4 PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 28 (1mA)	Route in module
214	D7	1404	810	T4 PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 29 (1mA)	Route in module
215	K5	1008	1998	T4_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 16 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
216	J6	1206	1800	T4_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 17 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
217	M5	1008	2394	T4_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 18 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
218	L6	1206	2196	T4_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 19 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
219	C12	2394	612	T4_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 8 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
220	L12	2394	2196	T4_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 9 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
221	E18	3582	1008	T5_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 20 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
222	A18	3582	216	T5_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 20 (200mA)	
223	C18	3582	612	T5_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 20 (200mA)	
224	E16	3186	1008	T5_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 21 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
225	A16	3186	216	T5_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 21 (200mA)	
226	C16	3186	612	T5_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 21 (200mA)	
227	G18	3582	1404	T5_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 22 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
228	L18	3582	2196	T5_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 22 (200mA)	
229	J18	3582	1800	T5_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 22 (200mA)	
230	G16	3186	1404	T5_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 23 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
231	L16	3186	2196	T5_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 23 (200mA)	
232	J16	3186	1800	T5_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 23 (200mA)	
233	D13	2592	810	T5 PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 30 (1mA)	Route in module
234	B15	2988	414	T5 PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 31 (1mA)	Route in module
235	B13	2592	414	T5 PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 32 (1mA)	Route in module
236	A14	2790	216	T5 PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 33 (1mA)	Route in module

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
237	C14	2790	612	T5_PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 34 (1mA)	Route in module
238	D15	2988	810	T5_PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 35 (1mA)	Route in module
239	K13	2592	1998	T5_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 20 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
240	J14	2790	1800	T5_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 21 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
241	M13	2592	2394	T5_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 22 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
242	L14	2790	2196	T5_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 23 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
243	C20	3978	612	T5_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 10 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
244	L20	3978	2196	T5_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 11 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
245	E26	5166	1008	T6_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 24 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
246	C26	5166	612	T6_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 24 (200mA)	
247	A26	5166	216	T6_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 24 (200mA)	
248	E24	4770	1008	T6_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 25 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
249	C24	4770	612	T6_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 25 (200mA)	
250	A24	4770	216	T6_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 25 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
251	G26	5166	1404	T6_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 26 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
252	L26	5166	2196	T6_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 26 (200mA)	
253	J26	5166	1800	T6_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 26 (200mA)	
254	L24	4770	2196	T6_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 27 (200mA)	Route all 3 pins (_0/1/2) with equal resistance

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
255	J24	4770	1800	T6_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 27 (200mA)	and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
256	G24	4770	1404	T6_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 27 (200mA)	
257	D21	4176	810	T6 PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 36 (1mA)	Route in module
258	B23	4572	414	T6 PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 37 (1mA)	Route in module
259	B21	4176	414	T6 PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 38 (1mA)	Route in module
260	A22	4374	216	T6 PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 39 (1mA)	Route in module
261	C22	4374	612	T6 PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 40 (1mA)	Route in module
262	D23	4572	810	T6 PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 41 (1mA)	Route in module
263	K21	4176	1998	T6_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 24 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
264	J22	4374	1800	T6_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 25 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
265	M21	4176	2394	T6_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 26 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
266	L22	4374	2196	T6_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 27 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
267	C28	5562	612	T6_RH0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 12 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
268	L28	5562	2196	T6_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 13 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
269	E34	6750	1008	T7_LD0_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 28 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
270	C34	6750	612	T7_LD0_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 28 (200mA)	
271	A34	6750	216	T7_LD0_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 28 (200mA)	
272	C32	6354	612	T7_LD1_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 29 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
273	E32	6354	1008	T7_LD1_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 29 (200mA)	trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
274	A32	6354	216	T7_LD1_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 29 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
275	J34	6750	1800	T7_LD2_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 30 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
276	L34	6750	2196	T7_LD2_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 30 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
277	G34	6750	1404	T7_LD2_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 30 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
278	L32	6354	2196	T7_LD3_0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 31 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
279	G32	6354	1404	T7_LD3_1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 31 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
280	J32	6354	1800	T7_LD3_2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 1 current sink 31 (200mA)	Route all 3 pins (_0/1/2) with equal resistance and combine into 1 thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
281	D29	5760	810	T7 PDO		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 41 (1mA)	Route in module
282	B31	6156	414	T7 PD1		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 42 (1mA)	Route in module
283	B29	5760	414	T7 PD2		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 43 (1mA)	Route in module
284	A30	5958	216	T7 PD3		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 44 (1mA)	Route in module
285	C30	5958	612	T7 PD4		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 45 (1mA)	Route in module
286	D31	6156	810	T7 PD5		Input	Analog	VDDA_2P5/ VSSA	-	Transimpedance amplifier input 46 (1mA)	Route in module
287	K29	5760	1998	T7_QB0		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 28 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
288	J30	5958	1800	T7_QB1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 29 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
289	M29	5760	2394	T7_QB2		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 30 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
290	L30	5958	2196	T7_QB3		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 3 current source 31 (35mA)	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
291	C36	7146	612	T7_RHO		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 14 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
292	L36	7146	2196	T7_RH1		Output	Analog	VDDA_2P5/ VSSA	-	DAC Set 2 current sink 15 (65 mA)	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
293	Y19	3780	3978	TCK		Input/ Clock	Digital	VDDIO1/VSSIO		JTAG Clock pin.	Route in module
294	V19	3780	3582	TDI		Input	Digital	VDDIO1/VSSIO		JTAG serial data input.	Route in module
295	V21	4176	3582	TDO		Input/ Output	Digital	VDDIO1/VSSIO		JTAG data output.	Route in module
296	AC34	6750	4572	TEMP_DIODE_0		Output	Analog	VDDA_2P5/ VSSA	-	Internal Current Source to be connected through pad to external temperature diodes.	Route in module
297	AA34	6750	4176	TEMP_DIODE_1		Output	Analog	VDDA_2P5/ VSSA	-	Internal Current Source to be connected through pad to external temperature diodes.	Route in module
298	W34	6750	3780	TEMP_DIODE_2		Output	Analog	VDDA_2P5/ VSSA	-	Internal Current Source to be connected through pad to external temperature diodes.	Route in module
299	U34	6750	3384	TEMP_DIODE_3		Output	Analog	VDDA_2P5/ VSSA	-	Internal Current Source to be connected through pad to external temperature diodes.	Route in module
300	W20	3978	3780	TMS		Input	Digital	VDDIO1/VSSIO		JTAG mode select pin.	Route in module
301	AC24	4770	4572	TM[0]		Input/Out put	Analog	VDD_2P5/VSSD		Flash Test mode pins.	Should be floating. 200ohm resistor for ESD/LUP protection has been implemented inside macro.
302	AB23	4572	4374	TM[1]		Input/Out put	Analog	VDD_2P5/VSSD		Flash Test mode pins.	Should be floating. 200ohm resistor for ESD/LUP protection has been implemented inside macro.
303	AA22	4374	4176	TM[2]		Input/ Output	Analog	VDD_2P5/VSSD		Flash Test mode pins.	Should be floating. 200ohm resistor for ESD/LUP protection has been implemented inside macro.
304	AA24	4770	4176	TM[3]		Input/ Output	Analog	VDD_2P5/VSSD		Flash Test mode pins.	Should be floating. 200ohm resistor for ESD/LUP protection has been implemented inside macro.
305	Y21	4176	3978	TRST		Input	Digital	VDDIO1/VSSIO		JTAG reset pin.	Route in module
306	AC2	414	4572	UART_RX		Input	Digital	VDDIO1/VSSIO		UART receive.	Add 1K pull-up resistor to VDDIO1.
307	AD3	612	4770	UART_TX		Output	Digital	VDDIO1/VSSIO		UART transmit.	Add 1K pull-up resistor to VDDIO1.
308	N20	3978	2592	VDD_OP9_0	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	Combine all VDD_OP9_* pin to 1 plane. And connect Capacitors - 2x (1uF, 100nF & 10nF) caps between VDD_OP9 plane & VSSD plane at substrate level. 1 capacitor set per IC side (north & south). Bring the plane to the PCB and connect to 10uF cap to the global ground.
309	AD21	4176	4770	VDD_OP9_1	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
310	AE4	810	4968	VDD_OP9_12	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
311	AE20	3978	4968	VDD_OP9_13	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
312	AE8	1602	4968	VDD_OP9_14	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
313	AD15	2988	4770	VDD_OP9_15	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
314	D3	612	810	VDD_OP9_16	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
315	N14	2790	2592	VDD_OP9_17	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
316	AE26	5166	4968	VDD_OP9_18	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
317	AD5	1008	4770	VDD_OP9_19	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
318	AD13	2592	4770	VDD_OP9_20	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
319	N4	810	2592	VDD_OP9_21	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
320	AT3	612	7146	VDD_OP9_23	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
321	P9	1800	2790	VDD_OP9_24	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
322	P21	4176	2790	VDD_OP9_26	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
323	P19	3780	2790	VDD_OP9_28	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
324	P15	2988	2790	VDD_OP9_29	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
325	AD19	3780	4770	VDD_OP9_3	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
326	AP3	612	6750	VDD_OP9_30	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
327	P13	2592	2790	VDD_OP9_31	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
328	B3	612	414	VDD_OP9_4	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
329	AE14	2790	4968	VDD_OP9_5	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
330	N8	1602	2592	VDD_OP9_6	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
331	AD9	1800	4770	VDD_OP9_7	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
332	P5	1008	2790	VDD_OP9_8	Connected to VDD_OP9	Input/ Output	Power	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.	
333	W22	4374	3780	VDD_2P5_0	Connected to VDD_2P5	Input	Power	VDD_2P5/VSSD		2.5V dedicated power supply for FLASH	Combine all VDD_2P5_* pin to 1 plane. And connect Capacitors - 1x (10uF, 1uF, 100nF & 10nF) caps between VDD_2P5 plane & VSSD plane at substrate level. Add 10uF cap to the global ground at PCB level.
334	Y23	4572	3978	VDD_2P5_1	Connected to VDD_2P5	Input	Power	VDD_2P5/VSSD		2.5V dedicated power supply for FLASH	
335	Y27	5364	3978	VDD_2P5_LDO_0	Connected to VDD_2P5_L DO	Input	Power	VDD_2P5_LDO/ VSSD		2.5V Power supply for Core (0.9V) LDO	Combine all VDD_2P5_LDO* pin to 1 plane. And connect Capacitors - 1x (10uF, 1uF, 100nF, & 10nF) caps between VDD_2P5_LDO plane & VSSD plane at substrate level. Add 10uF cap to the global ground at PCB level.
336	AB27	5364	4374	VDD_2P5_LDO_1	Connected to VDD_2P5_L DO	Input	Power	VDD_2P5_LDO/ VSSD		2.5V Power supply for Core (0.9V) LDO	
337	U32	6354	3384	VDDA_2P5_0	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	Combine all VDDA_2P5_* pins into 1 plane. Cap - 4x100nF & 4x10nF caps between VDDA_2P5 plane & VSSA plane on substrate; Cap - 10uF, 1uF, 100nF & 10nF caps between VDDA_2P5 plane & common ground on PCB.
338	F31	6156	1206	VDDA_2P5_1	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
339	F7	1404	1206	VDDA_2P5_10	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
340	F15	2988	1206	VDDA_2P5_11	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
341	U30	5958	3384	VDDA_2P5_12	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
342	R32	6354	2988	VDDA_2P5_13	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
343	E12	2394	1008	VDDA_2P5_14	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
344	V35	6948	3582	VDDA_2P5_15	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
345	A12	2394	216	VDDA_2P5_16	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
346	R30	5958	2988	VDDA_2P5_17	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
347	E28	5562	1008	VDDA_2P5_18	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
348	AA32	6354	4176	VDDA_2P5_19	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
349	AF31	6156	5166	VDDA_2P5_2	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
350	F23	4572	1206	VDDA_2P5_20	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
351	E20	3978	1008	VDDA_2P5_21	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
352	AC32	6354	4572	VDDA_2P5_22	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
353	W32	6354	3780	VDDA_2P5_23	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
354	AH23	4572	5562	VDDA_2P5_24	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
355	Y35	6948	3978	VDDA_2P5_25	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
356	K31	6156	1998	VDDA_2P5_26	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
357	AK15	2988	5958	VDDA_2P5_27	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
358	AN28	5562	6552	VDDA_2P5_28	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
359	AJ36	7146	5760	VDDA_2P5_29	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
360	AH15	2988	5562	VDDA_2P5_3	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
361	H7	1404	1602	VDDA_2P5_30	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
362	AL20	3978	6156	VDDA_2P5_31	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
363	E36	7146	1008	VDDA_2P5_32	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
364	AN36	7146	6552	VDDA_2P5_33	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
365	G20	3978	1404	VDDA_2P5_34	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
366	H31	6156	1602	VDDA_2P5_35	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
367	G36	7146	1404	VDDA_2P5_36	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
368	M31	6156	2394	VDDA_2P5_37	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	

Combine all VDDA_2P5_* pins into 1 plane. Cap - 4x100nF & 4x10nF caps between VDDA_2P5 plane & VSSA plane on substrate;
Cap - 10uF, 1uF, 100nF & 10nF caps between VDDA_2P5 plane & common ground on PCB.

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
369	AM15	2988	6354	VDDA_2P5_38	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	Combine all VDDA_2P5_* pins into 1 plane. Cap - 4x100nF & 4x10nF caps between VDDA_2P5 plane & VSSA plane on substrate; Cap - 10uF, 1uF, 100nF & 10nF caps between VDDA_2P5 plane & common ground on PCB.
370	M7	1404	2394	VDDA_2P5_39	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
371	J28	5562	1800	VDDA_2P5_4	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
372	AK23	4572	5958	VDDA_2P5_40	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
373	J20	3978	1800	VDDA_2P5_41	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
374	G28	5562	1404	VDDA_2P5_42	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
375	K23	4572	1998	VDDA_2P5_43	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
376	AK7	1404	5958	VDDA_2P5_44	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
377	AM23	4572	6354	VDDA_2P5_45	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
378	G12	2394	1404	VDDA_2P5_46	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
379	K15	2988	1998	VDDA_2P5_47	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
380	M23	4572	2394	VDDA_2P5_48	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
381	AM7	1404	6354	VDDA_2P5_49	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
382	AF23	4572	5166	VDDA_2P5_5	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
383	A28	5562	216	VDDA_2P5_50	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
384	J12	2394	1800	VDDA_2P5_51	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
385	M15	2988	2394	VDDA_2P5_52	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
386	AK31	6156	5958	VDDA_2P5_53	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
387	AC36	7146	4572	VDDA_2P5_54	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
388	AJ28	5562	5760	VDDA_2P5_55	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
389	AJ12	2394	5760	VDDA_2P5_56	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
390	H15	2988	1602	VDDA_2P5_57	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
391	K7	1404	1998	VDDA_2P5_58	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
392	AM31	6156	6354	VDDA_2P5_59	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
393	T35	6948	3186	VDDA_2P5_6	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
394	AN20	3978	6552	VDDA_2P5_60	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
395	A20	3978	216	VDDA_2P5_61	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
396	AL12	2394	6156	VDDA_2P5_62	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
397	AB37	7344	4374	VDDA_2P5_63	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
398	H23	4572	1602	VDDA_2P5_64	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
399	J36	7146	1800	VDDA_2P5_65	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
400	AL28	5562	6156	VDDA_2P5_66	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
401	AL36	7146	6156	VDDA_2P5_67	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
402	AU20	3978	7344	VDDA_2P5_68	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
403	AN12	2394	6552	VDDA_2P5_69	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
404	AF7	1404	5166	VDDA_2P5_7	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
405	AU28	5562	7344	VDDA_2P5_70	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
406	AJ20	3978	5760	VDDA_2P5_71	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
407	AU12	2394	7344	VDDA_2P5_72	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
408	AH7	1404	5562	VDDA_2P5_73	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
409	AF15	2988	5166	VDDA_2P5_8	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
410	AH31	6156	5562	VDDA_2P5_9	Connected to VDDA_2P5	Input	Power	VDDA_2P5/ VSSA	-	2.5V Analog Supply Voltage.	
411	V27	5364	3582	VDDA_2P5_ADC		Input	Power	VDDA_2P5_ADC/ VSSA		2.5V Power supply for ADC	Cap - 100nF & 10nF caps between VDDA_2P5_ADC & VSSA on substrate; Cap - 10uF , 1uF, 100nF & 10nF caps between VDDA_2P5_ADC & common ground on PCB.
412	AB19	3780	4374	VDDIO1_1	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO	-	VDDIO1 digital IO supply.	Combine all VDDIO1_* pins into 1 plane. Cap - 100nF & 10nF caps between VDDIO1 plane & VSSIO plane on substrate; Cap - 10uF , 1uF, 100nF & 10nF caps between VDDIO1 plane & common ground on PCB.
413	AA8	1602	4176	VDDIO1_13	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
414	R2	414	2988	VDDIO1_14	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
415	AC20	3978	4572	VDDIO1_19	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
416	AB21	4176	4374	VDDIO1_2	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
417	AB9	1800	4374	VDDIO1_20	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
418	T3	612	3186	VDDIO1_21	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
419	AJ2	414	5760	VDDIO1_24	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
420	AH1	216	5562	VDDIO1_25	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
421	T1	216	3186	VDDIO1_27	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
422	AH3	612	5562	VDDIO1_28	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
423	AC8	1602	4572	VDDIO1_4	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
424	AG2	414	5364	VDDIO1_5	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
425	AB7	1404	4374	VDDIO1_6	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
426	U2	414	3384	VDDIO1_7	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
427	AA20	3978	4176	VDDIO1_8	Connected to VDDIO1	Input	Power	VDDIO1/VSSIO		VDDIO1 digital IO supply.	
428	AC14	2790	4572	VDDIO2_10	Connected to VDDIO2	Input	Power	VDDIO2/VSSIO		VDDIO2 digital IO supply.	
429	AB13	2592	4374	VDDIO2_11	Connected to VDDIO2	Input	Power	VDDIO2/VSSIO		VDDIO2 digital IO supply.	
430	AA14	2790	4176	VDDIO2_18	Connected to VDDIO2	Input	Power	VDDIO2/VSSIO		VDDIO2 digital IO supply.	
431	AB15	2988	4374	VDDIO2_3	Connected to VDDIO2	Input	Power	VDDIO2/VSSIO		VDDIO2 digital IO supply.	
432	R18	3582	2988	VPP_0	Connected to VPP	Input	Power	VPP/VSSIO		Flash test supply.	
433	R16	3186	2988	VPP_1	Connected to VPP	Input	Power	VPP/VSSIO		Flash test supply.	
434	U18	3582	3384	VPP_2	Connected to VPP	Input	Power	VPP/VSSIO		Flash test supply.	
435	U16	3186	3384	VPP_3	Connected to VPP	Input	Power	VPP/VSSIO		Flash test supply.	
436	T17	3384	3186	VPP_4	Connected to VPP	Input	Power	VPP/VSSIO		Flash test supply.	
437	R28	5562	2988	VREFP_ADC		Input	Analog	VREFP_ADC/ AGNDREF_ADC		Positive Reference Voltage for ADC	
438	E6	1206	1008	VSSA_0	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
439	AM21	4176	6354	VSSA_1	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
440	AH19	3780	5562	VSSA_10	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
441	K11	2196	1998	VSSA_100	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
442	AL4	810	6156	VSSA_101	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
443	H17	3384	1602	VSSA_102	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
444	AT11	2196	7146	VSSA_103	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
445	K9	1800	1998	VSSA_104	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
446	AK29	5760	5958	VSSA_105	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
447	C4	810	612	VSSA_106	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
448	W36	7146	3780	VSSA_107	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
449	K37	7344	1998	VSSA_108	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
450	AP11	2196	6750	VSSA_109	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
451	B9	1800	414	VSSA_11	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
452	AT19	3780	7146	VSSA_110	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
453	M11	2196	2394	VSSA_111	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
454	AK27	5364	5958	VSSA_112	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
455	AL14	2790	6156	VSSA_113	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
456	H27	5364	1602	VSSA_114	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
457	AT35	6948	7146	VSSA_115	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
458	AN6	1206	6552	VSSA_116	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
459	H13	2592	1602	VSSA_117	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
460	B33	6552	414	VSSA_118	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
461	M37	7344	2394	VSSA_119	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
462	AG4	810	5364	VSSA_12	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
463	AT25	4968	7146	VSSA_120	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
464	AP19	3780	6750	VSSA_121	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
465	M9	1800	2394	VSSA_122	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
466	AK25	4968	5958	VSSA_123	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
467	AM29	5760	6354	VSSA_124	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
468	J4	810	1800	VSSA_125	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
469	H25	4968	1602	VSSA_126	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
470	AT9	1800	7146	VSSA_127	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
471	AP35	6948	6750	VSSA_128	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
472	AN4	810	6552	VSSA_129	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
473	F27	5364	1206	VSSA_13	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
474	H11	2196	1602	VSSA_130	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
475	AP25	4968	6750	VSSA_131	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
476	AL30	5958	6156	VSSA_132	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
477	H5	1008	1602	VSSA_133	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
478	F35	6948	1206	VSSA_134	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
479	AP33	6552	6750	VSSA_135	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
480	AJ4	810	5760	VSSA_136	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
481	AP9	1800	6750	VSSA_137	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
482	AF35	6948	5166	VSSA_138	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
483	B35	6948	414	VSSA_139	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
484	V31	6156	3582	VSSA_14	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
485	AN14	2790	6552	VSSA_140	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
486	H21	4176	1602	VSSA_141	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
487	AN30	5958	6552	VSSA_142	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
488	U36	7146	3384	VSSA_143	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
489	R36	7146	2988	VSSA_144	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
490	AU4	810	7344	VSSA_145	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
491	AL6	1206	6156	VSSA_146	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
492	H19	3780	1602	VSSA_147	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
493	AA36	7146	4176	VSSA_148	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
494	D37	7344	810	VSSA_149	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
495	W30	5958	3780	VSSA_15	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
496	H33	6552	1602	VSSA_150	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
497	M33	6552	2394	VSSA_151	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
498	V33	6552	3582	VSSA_152	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
499	AH33	6552	5562	VSSA_153	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
500	AB33	6552	4374	VSSA_154	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
501	K33	6552	1998	VSSA_155	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
502	AK33	6552	5958	VSSA_156	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
503	T33	6552	3186	VSSA_157	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
504	D33	6552	810	VSSA_158	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
505	AF33	6552	5166	VSSA_159	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
506	AF9	1800	5166	VSSA_16	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
507	F33	6552	1206	VSSA_160	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
508	AB25	4968	4374	VSSA_161	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
509	Y25	4968	3978	VSSA_162	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
510	AA26	5166	4176	VSSA_165	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
511	W26	5166	3780	VSSA_166	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
512	F11	2196	1206	VSSA_17	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
513	AH9	1800	5562	VSSA_18	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
514	F19	3780	1206	VSSA_19	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
515	AH17	3384	5562	VSSA_2	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
516	W28	5562	3780	VSSA_20	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
517	H35	6948	1602	VSSA_21	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
518	F13	2592	1206	VSSA_22	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
519	AK35	6948	5958	VSSA_23	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
520	F9	1800	1206	VSSA_24	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
521	F17	3384	1206	VSSA_25	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
522	E14	2790	1008	VSSA_26	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
523	AB31	6156	4374	VSSA_27	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
524	B19	3780	414	VSSA_28	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
525	E30	5958	1008	VSSA_29	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
526	AF27	5364	5166	VSSA_3	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
527	AF11	2196	5166	VSSA_30	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	
528	B27	5364	414	VSSA_31	Connected to VSSA	Input	Ground	VSSA	-	OV Analog Ground Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
529	E4	810	1008	VSSA_32	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
530	AH27	5364	5562	VSSA_33	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
531	K35	6948	1998	VSSA_34	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
532	F5	1008	1206	VSSA_35	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
533	B17	3384	414	VSSA_36	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
534	AA30	5958	4176	VSSA_37	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
535	F25	4968	1206	VSSA_38	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
536	B25	4968	414	VSSA_39	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
537	D11	2196	810	VSSA_4	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
538	AH25	4968	5562	VSSA_40	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
539	E22	4374	1008	VSSA_41	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
540	AH11	2196	5562	VSSA_42	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
541	AF19	3780	5166	VSSA_43	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
542	Y31	6156	3978	VSSA_44	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
543	AK17	3384	5958	VSSA_45	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
544	Y33	6552	3978	VSSA_46	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
545	AF17	3384	5166	VSSA_47	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
546	F21	4176	1206	VSSA_48	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
547	H9	1800	1602	VSSA_49	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
548	B11	2196	414	VSSA_5	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
549	AM33	6552	6354	VSSA_50	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
550	AH37	7344	5562	VSSA_51	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
551	AT27	5364	7146	VSSA_52	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
552	AN22	4374	6552	VSSA_53	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
553	H29	5760	1602	VSSA_54	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
554	D27	5364	810	VSSA_55	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
555	AM19	3780	6354	VSSA_56	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
556	G22	4374	1404	VSSA_57	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
557	AL22	4374	6156	VSSA_58	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
558	D35	6948	810	VSSA_59	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
559	AF25	4968	5166	VSSA_6	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
560	AT17	3384	7146	VSSA_60	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
561	AR4	810	6948	VSSA_61	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
562	AM35	6948	6354	VSSA_62	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
563	AT33	6552	7146	VSSA_63	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
564	AP27	5364	6750	VSSA_64	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
565	AP17	3384	6750	VSSA_65	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
566	D25	4968	810	VSSA_66	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
567	AK13	2592	5958	VSSA_67	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
568	AM17	3384	6354	VSSA_68	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
569	AF37	7344	5166	VSSA_69	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
570	F29	5760	1206	VSSA_7	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
571	AP37	7344	6750	VSSA_70	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
572	K27	5364	1998	VSSA_71	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
573	A4	810	216	VSSA_72	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
574	AK11	2196	5958	VSSA_73	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
575	AM27	5364	6354	VSSA_74	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
576	G30	5958	1404	VSSA_75	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
577	K25	4968	1998	VSSA_76	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
578	AK9	1800	5958	VSSA_77	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
579	AM13	2592	6354	VSSA_78	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
580	M35	6948	2394	VSSA_79	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
581	AH35	6948	5562	VSSA_8	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
582	AK21	4176	5958	VSSA_80	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
583	AM25	4968	6354	VSSA_81	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
584	L4	810	2196	VSSA_82	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
585	D19	3780	810	VSSA_83	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
586	M27	5364	2394	VSSA_84	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
587	AM11	2196	6354	VSSA_85	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
588	G14	2790	1404	VSSA_86	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
589	AK19	3780	5958	VSSA_87	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
590	D17	3384	810	VSSA_88	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
591	M25	4968	2394	VSSA_89	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
592	D9	1800	810	VSSA_9	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
593	T31	6156	3186	VSSA_90	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
594	AK5	1008	5958	VSSA_91	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
595	AM9	1800	6354	VSSA_92	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
596	M19	3780	2394	VSSA_93	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
597	G6	1206	1404	VSSA_94	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
598	K19	3780	1998	VSSA_95	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
599	M17	3384	2394	VSSA_96	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
600	G4	810	1404	VSSA_97	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
601	K17	3384	1998	VSSA_98	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
602	AM5	1008	6354	VSSA_99	Connected to VSSA	Input	Ground	VSSA	-	0V Analog Ground Voltage.	
603	AE24	4770	4968	VSSD_0	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	

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Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
604	AD23	4572	4770	VSSD_1	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
605	P25	4968	2790	VSSD_10	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
606	N10	1998	2592	VSSD_11	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
607	D1	216	810	VSSD_12	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
608	R14	2790	2988	VSSD_13	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
609	U20	3978	3384	VSSD_14	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
610	AE12	2394	4968	VSSD_16	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
611	N26	5166	2592	VSSD_18	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
612	V11	2196	3582	VSSD_19	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
613	AE6	1206	4968	VSSD_2	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
614	AE10	1998	4968	VSSD_21	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
615	E2	414	1008	VSSD_22	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
616	N18	3582	2592	VSSD_24	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
617	R24	4770	2988	VSSD_25	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
618	AE22	4374	4968	VSSD_26	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
619	N6	1206	2592	VSSD_29	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
620	AD25	4968	4770	VSSD_3	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
621	AD17	3384	4770	VSSD_31	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
622	N16	3186	2592	VSSD_32	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
623	AA28	5562	4176	VSSD_34	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
624	N24	4770	2592	VSSD_35	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
625	W4	810	3780	VSSD_36	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
626	AC22	4374	4572	VSSD_37	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
627	N12	2394	2592	VSSD_4	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
628	R20	3978	2988	VSSD_40	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
629	AE18	3582	4968	VSSD_41	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
630	V5	1008	3582	VSSD_42	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
631	N22	4374	2592	VSSD_43	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
632	R8	1602	2988	VSSD_45	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
633	T7	1404	3186	VSSD_47	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
634	C2	414	612	VSSD_48	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
635	P11	2196	2790	VSSD_49	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
636	AE16	3186	4968	VSSD_5	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
637	P7	1404	2790	VSSD_51	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
638	T13	2592	3186	VSSD_52	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
639	AD7	1404	4770	VSSD_53	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	

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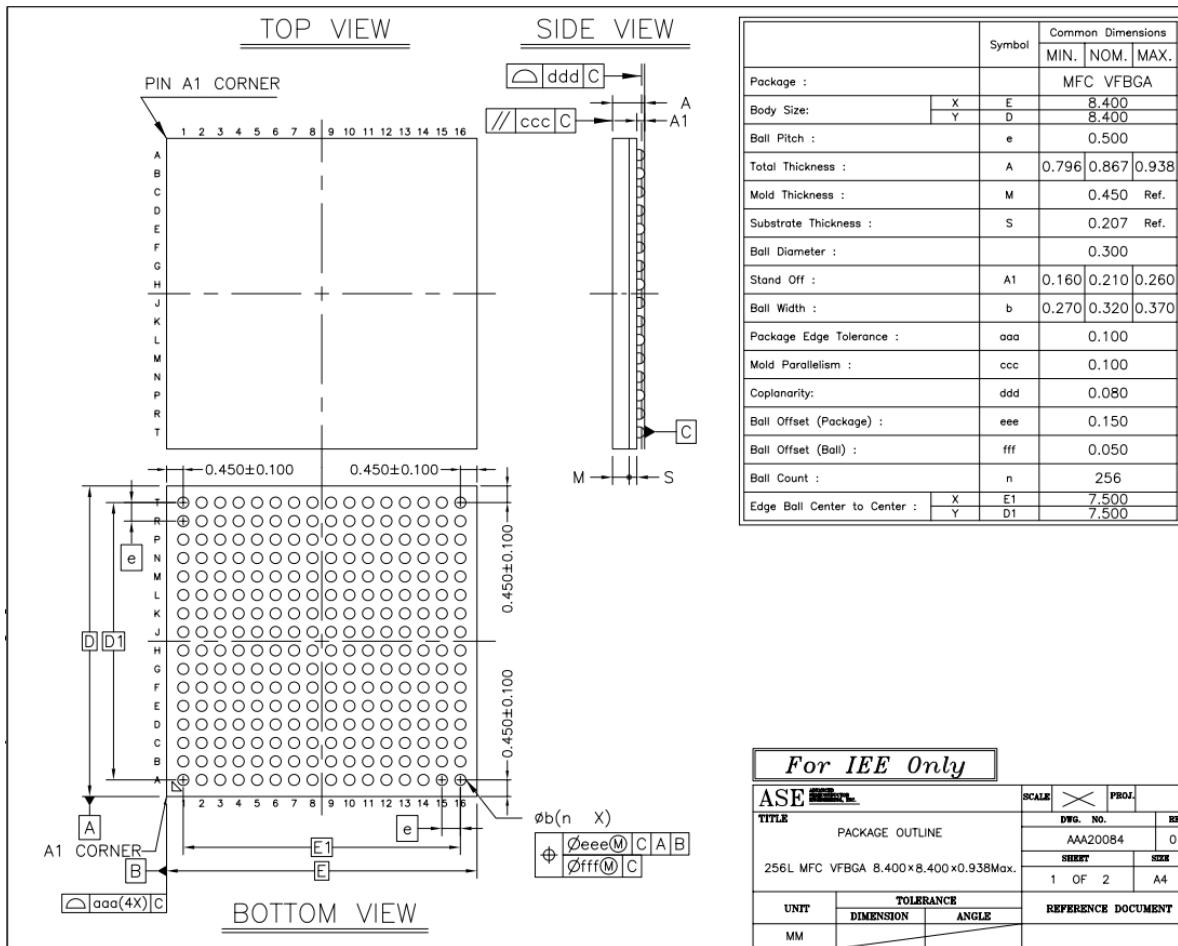


Pin #	Alpha numeric Pin #	X	Y	Pin Name	Power/ Ground notes	Direction	Type	Domain	Default	Description	Comments
640	P23	4572	2790	VSSD_54	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
641	P17	3384	2790	VSSD_55	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
642	T21	4176	3186	VSSD_56	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
643	T19	3780	3186	VSSD_57	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
644	AR2	414	6948	VSSD_58	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
645	AP1	216	6750	VSSD_59	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
646	AC26	5166	4572	VSSD_6	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
647	AN2	414	6552	VSSD_60	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
648	W10	1998	3780	VSSD_7	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
649	AC28	5562	4572	VSSD_8	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
650	AD11	2196	4770	VSSD_9	Connected to VSSD	Input	Ground	VSSD		0V Digital ground voltage.	
651	AB1	216	4374	VSSIO_0	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
652	AA2	414	4176	VSSIO_1	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
653	T9	1800	3186	VSSIO_10	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
654	Y11	2196	3978	VSSIO_11	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
655	W12	2394	3780	VSSIO_12	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
656	U14	2790	3384	VSSIO_13	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
657	T15	2988	3186	VSSIO_14	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
658	V23	4572	3582	VSSIO_19	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
659	AB3	612	4374	VSSIO_2	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
660	W24	4770	3780	VSSIO_20	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
661	K1	216	1998	VSSIO_3	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
662	L2	414	2196	VSSIO_4	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
663	J2	414	1800	VSSIO_5	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
664	K3	612	1998	VSSIO_6	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
665	Y5	1008	3978	VSSIO_7	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
666	W6	1206	3780	VSSIO_8	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
667	U8	1602	3384	VSSIO_9	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
668	W16	3186	3780	VSSIO_15	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
669	Y17	3384	3978	VSSIO_16	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
670	V17	3384	3582	VSSIO_17	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
671	W18	3582	3780	VSSIO_18	Connected to VSSIO	Input	Ground	VSSIO		0V Digital IO ground voltage.	
672	T27	5364	3186	VSUP_ADC_EXT		Input / Output	Analog	VSUP_ADC_EXT /VSSA		Analog power supply for ADC	Cap - 1uF , 100nF & 10nF caps between VSUP_ADC_EXT & VSSA at substrate level. Add 10uF cap to the global ground at PCB level.



6.7.3 FCCSP (Flip Chip Scale Package)

6.7.3.1 Mechanical Information



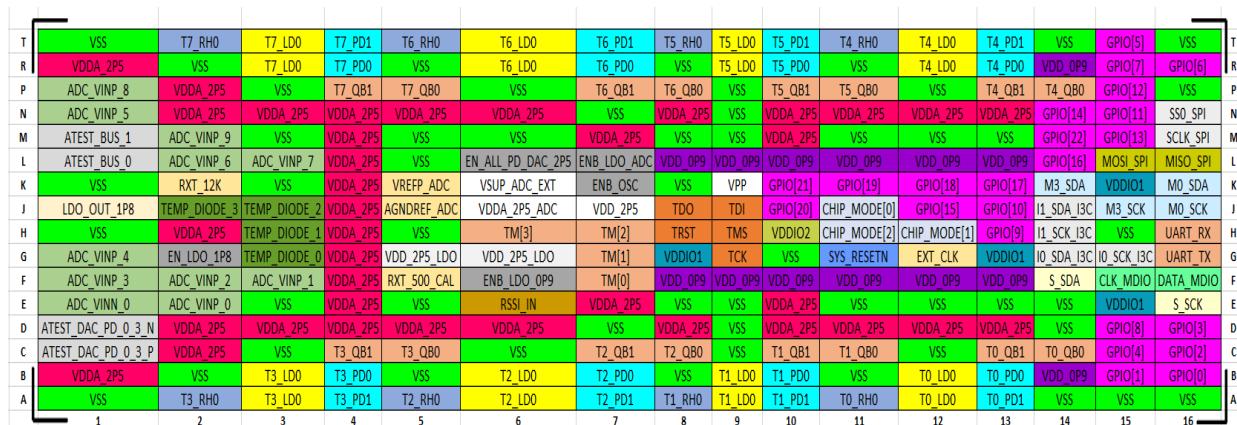


Figure 3 BGA map (FCCSP package – dead-bug view)

6.7.3.2 BGA List

Table 24 Pin list (FCCSP package)

BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
E1	ADC_VINN_0	VDDA_2P5/ VSSA	-	Differential N Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Match length for the differential pairs
E2	ADC_VINP_0	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Match length for the differential pairs
F3	ADC_VINP_1	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
F2	ADC_VINP_2	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
F1	ADC_VINP_3	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
G1	ADC_VINP_4	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
N1	ADC_VINP_5	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
L2	ADC_VINP_6	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
L3	ADC_VINP_7	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
P1	ADC_VINP_8	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise
M2	ADC_VINP_9	VDDA_2P5/ VSSA	-	Differential P Input for ADC. This input directly connects to ADC mux before ADC. Signal range is 0 to 2V.	Match length for the differential pairs	Avoid coupling with noise

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
J5	AGNDREF_ADC	VDDA_2P5_ADC/ VSSA		Negative Reference Voltage for ADC	Avoid noise coupling. Treat ADC_VREF and AGNREF_ADC as matched differential pair.	Treat ADC_VREF and AGNREF_ADC as matched differential pair. L=30Z: Ferrite bead (e.g. BLM21PG300SN1D from Murata) between VSSA & AGNDREF_ADC
L1	ATEST_BUS_0	VDDA_2P5/ VSSA	-	Pin 0 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.		Connect to test point
M1	ATEST_BUS_1	VDDA_2P5/ VSSA	-	Pin 1 of Analog Test Bus ATEST_BUS[3:0]. In production board, bring to a test point.		Connect to test point
D1	ATEST_DAC_PD_0_3_N	VDDA_2P5/ VSSA		Differential N Output pin- for ATEST but for DAC-PD Tiles 0-3. In production board, bring to a test point.		Connect to test point
C1	ATEST_DAC_PD_0_3_P	VDDA_2P5/ VSSA		Differential P Output pin- for ATEST but for DAC-PD Tiles 0-3. In production board, bring to a test point.		Connect to test point
J11	CHIP_MODE[0]	VDDIO1/ VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.		10K to Ground
H12	CHIP_MODE[1]	VDDIO1/ VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.		10K to Ground
H11	CHIP_MODE[2]	VDDIO1/ VSSIO	0 (10k to VSSD)	Chip mode control. CMOS input/output level = 0~VDDIO1.		10K to Ground
F15	CLK_MDIO	VDDIO1/ VSSIO		Clock for MDIO Interface. fmax = 2.5MHz CMOS input/output level = 0~VDDIO1.		1.5k to VDDIO1
F16	DATA_MDIO	VDDIO1/ VSSIO		Data for MDIO Interface. fmax = 2.5MHz CMOS input/output level = 0~VDDIO1.		1.5k to VDDIO1
F6	ENB_LDO_0P9	VDD_2P5_LDO/ VSSD	0 (100k to VSSD)	Power down (2.5V domain) of Digital Core LDO. When High, Internal Digital Core LDO is powered down. Internal to ASIC, this pin is pulled down using 100Kohm Resistor.		10K to Ground
L7	ENB_LDO_ADC	VDDA_2P5_ADC/ VSSA	0 (100k to VSSD)	Power down (2.5V domain) of ADC LDO. When High, Internal ADC LDO is powered down. Internal to ASIC, this pin is pulled down using 100Kohm Resistor.		10K to Ground
K7	ENB_OSC	VDDIO1/ VSSIO	0 (10k to VSSD)	Power Down Internal Oscillator. When High, internal oscillator is turned off. Clock needs to be supplied through EXT_CLK pin.		10K to Ground
L6	EN_ALL_PD_DAC_2P5	VDDA_2P5/ VSSA	2.5V (100k to 2.5V)	Master enable control for all DAC and PD amplifiers. Enable=2.5V, Disable = 0V. When kept open firmware takes enable/disable control of the DAC/PD amplifier.		10K to VDDA_2P5
G2	EN_LDO_1P8	VDD_2P5_LDO/ VSSD	0 (100k to VSSD)	Power down of 1.8V LDO. When Low, 1.8V LDO is powered down.		10K to VDD_2P5_LDO
G12	EXT_CLK	VDDIO1/ VSSIO		External clock. Used for testing. fmax = 400MHz. CMOS input/output level = 0~VDDIO1	fmax=200MHz CMOS clock (Zo = 50-Ohm routing)	Connect to test point, 10K to Ground
B16	GPIO[0]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	10K to Ground
J13	GPIO[10]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
N15	GPIO[11]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
P15	GPIO[12]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
M15	GPIO[13]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
N14	GPIO[14]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
J12	GPIO[15]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
L14	GPIO[16]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
K13	GPIO[17]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
K12	GPIO[18]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	
K11	GPIO[19]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	10K to VDDIO2
B15	GPIO[1]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	10K to Ground
J10	GPIO[20]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	
K10	GPIO[21]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	
M14	GPIO[22]	VDDIO2/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	
C16	GPIO[2]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
D16	GPIO[3]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
C15	GPIO[4]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
T15	GPIO[5]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
R16	GPIO[6]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
R15	GPIO[7]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
D15	GPIO[8]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
H13	GPIO[9]	VDDIO1/ VSSIO		General Purpose IO. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	
G15	IO_SCK_I3C	VDDIO1/ VSSIO		Clock for I3C Instance 0. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
G14	IO_SDA_I3C	VDDIO1/ VSSIO		Data for I3C Instance 0. CMOS input/output level = 0~VDDIO	fmax=50MHz CMOS	1k to VDDIO1
H14	I1_SCK_I3C	VDDIO1/ VSSIO		Clock for I3C Instance 1. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
J14	I1_SDA_I3C	VDDIO1/ VSSIO		Data for I3C Instance 1. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
J1	LDO_OUT_1P8	VDD_2P5_LDO/ VSSA	-	Regulated voltage by on chip LDO for 1.8V supply voltage for external use	Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Cap - 1x2.2uF, 1x100nF
J16	M0_SCK	VDDIO1/ VSSIO		I2C Master 0 clock. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
K16	M0_SDA	VDDIO1/ VSSIO		I2C Master 0 Data. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
J15	M3_SCK	VDDIO2/ VSSIO		I2C Master 3 clock. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	1k to VDDIO2
K14	M3_SDA	VDDIO2/ VSSIO		I2C Master 3 Data. CMOS input/output level = 0~VDDIO2	fmax=50MHz CMOS	1k to VDDIO2
L16	MISO_SPI	VDDIO1/ VSSIO		Master In Slave Out for SPI Interface	fmax=50MHz CMOS	Connect to slave
L15	MOSI_SPI	VDDIO1/ VSSIO		Master Out Slave In for SPI Interface	fmax=50MHz CMOS	Connect to slave
E6	RSSI_IN	VDDA_2P5/ VSSA	-	Input to sink RSSI current from RXIC/TIA	Avoid coupling with noise. Route with a thick trace (Imax = 5mA, Rs < 100mOhm).	Avoid coupling with noise
K2	RXT_12K	VDDA_2P5/ VSSA	-	External 12k+/-0.5 % tolerance resistor to ground for calibration and bias generation	Avoid coupling with noise. Route with a thick trace (Imax = 1mA, Rs < 100mOhm).	Put >10uF cap with total routing resistance < 4 ohms, Pad to Component.
F5	RXT_500_CAL	VDDA_2P5/ VSSA	-	External 500-Ohm precision resistor for calibration of internal reference currents	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 100mOhm).	Add 0.5k+/-0.5% precision resistor to VSSA
M16	SCLK_SPI	VDDIO1/ VSSIO		Clock for the SPI Interface	fmax=50MHz CMOS	Connect to slave
N16	SSO_SPI	VDDIO1/ VSSIO		Slave select line for SPI	fmax=50MHz CMOS	Connect to slave

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
G11	SYS_RESETN	VDDIO1/ VSSIO		External system reset		Connect to system reset
E16	S_SCK	VDDIO1/ VSSIO		I2C Interface clock for the slave. CMOS input/output level = 0~VDDIO1	fmax=50MHz CMOS	1k to VDDIO1
F14	S_SDA	VDDIO1/ VSSIO		I2C Interface data for the slave. CMOS input/output level = 0~VDDIO1.	fmax=50MHz CMOS	1k to VDDIO1
A12	T0_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 0 (200mA)	Route all 3 pins on die (T0_LDO_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs (Imax = 300mA, Rs < 10mOhm).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
B12	T0_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 1 (200mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
B13	T0 PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 0 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
A13	T0 PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 1 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
C14	T0_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 0 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
C13	T0_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 1 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
A11	T0_RHO	VDDA_2P5/VSSA	-	DAC Set 2 current sink 0 (65 mA)	Avoid coupling with noise. Route with a thick trace (Imax = 100mA, Rs < 20mOhm).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
A9	T1_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 2 (200mA)	Route all 3 pins on die (T1_LDO_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs (Imax = 300mA, Rs < 10mOhm).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
B9	T1_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 3 (200mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
B10	T1 PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 2 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
A10	T1 PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 3 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
C11	T1_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 2 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
C10	T1_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 3 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target $< 80m\Omega$). Add 1 μF capacitor closest to IC pin per DAC.
A8	T1_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 1 (65 mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 100mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target $< 80m\Omega$). Add 1 μF capacitor closest to IC pin per DAC
A6	T2_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 4 (200mA)	Route all 3 pins on die (T2_LD0_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs ($I_{max} = 300mA$, $R_s < 10m\Omega$).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target $< 20m\Omega$). Add 4.7 μF capacitor closest to IC pin per DAC
B6	T2_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 5 (200mA)		
B7	T2_PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 4 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise
A7	T2_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 5 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise
C8	T2_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 4 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target $< 80m\Omega$). Add 1 μF capacitor closest to IC pin per DAC.
C7	T2_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 5 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target $< 80m\Omega$). Add 1 μF capacitor closest to IC pin per DAC.
A5	T2_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 2 (65 mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 100mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target $< 80m\Omega$). Add 1 μF capacitor closest to IC pin per DAC
A3	T3_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 6 (200mA)	Route all 3 pins on die (T3_LD0_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs ($I_{max} = 300mA$, $R_s < 10m\Omega$).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target $< 20m\Omega$). Add 4.7 μF capacitor closest to IC pin per DAC
B3	T3_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 7 (200mA)		
B4	T3_PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 6 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
A4	T3_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 7 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise
C5	T3_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 6 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
C4	T3_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 7 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
A2	T3_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 3 (65 mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 100mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
R12	T4_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 8 (200mA)	Route all 3 pins on die (T4_LDO_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs ($I_{max} = 300mA$, $R_s < 10m\Omega$).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
T12	T4_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 9 (200mA)	Route all 3 pins on die (T4_LDO_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs ($I_{max} = 300mA$, $R_s < 10m\Omega$).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
R13	T4_PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 8 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise
T13	T4_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 9 (1mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 10mA$, $R_s < 20m\Omega$).	Avoid coupling with noise
P14	T4_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 8 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
P13	T4_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 9 (35mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 50mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
T11	T4_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 4 (65 mA)	Avoid coupling with noise. Route with a thick trace ($I_{max} = 100mA$, $R_s < 20m\Omega$).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
R9	T5_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 10 (200mA)	Route all 3 pins on die (T5_LDO_0/1/2) with equal resistance and combine into 2 thick	Combine two BGA outputs into a thick trace before routing to laser or other

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
T9	T5_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 11 (200mA)	traces to two FCCSP BGAs (Imax = 300mA, Rs < 10mOhm).	destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
R10	T5_PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 10 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
T10	T5_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 11 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
P11	T5_QBO	VDDA_2P5/VSSA	-	DAC Set 3 current source 10 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
P10	T5_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 11 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
T8	T5_RHO	VDDA_2P5/VSSA	-	DAC Set 2 current sink 5 (65 mA)	Avoid coupling with noise. Route with a thick trace (Imax = 100mA, Rs < 20mOhm).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
R6	T6_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 12 (200mA)	Route all 3 pins on die (T6_LDO_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs (Imax = 300mA, Rs < 10mOhm).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
T6	T6_LDO	VDDA_2P5/VSSA	-	DAC Set 1 current sink 13 (200mA)		Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
R7	T6_PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 12 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
T7	T6_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 13 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
P8	T6_QBO	VDDA_2P5/VSSA	-	DAC Set 3 current source 12 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
P7	T6_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 13 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
T5	T6_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 6 (65 mA)	Avoid coupling with noise. Route with a thick trace (Imax = 100mA, Rs < 20mOhm).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
R3	T7_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 14 (200mA)	Route all 3 pins on die (T7_LD0_0/1/2) with equal resistance and combine into 2 thick traces to two FCCSP BGAs (Imax = 300mA, Rs < 10mOhm).	Combine two BGA outputs into a thick trace before routing to laser or other destination (with max resistance target < 20m Ohm). Add 4.7 uF capacitor closest to IC pin per DAC
T3	T7_LD0	VDDA_2P5/VSSA	-	DAC Set 1 current sink 15 (200mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
R4	T7 PDO	VDDA_2P5/VSSA	-	Transimpedance amplifier input 14 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
T4	T7_PD1	VDDA_2P5/VSSA	-	Transimpedance amplifier input 15 (1mA)	Avoid coupling with noise. Route with a thick trace (Imax = 10mA, Rs < 20mOhm).	Avoid coupling with noise
P5	T7_QB0	VDDA_2P5/VSSA	-	DAC Set 3 current source 14 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
P4	T7_QB1	VDDA_2P5/VSSA	-	DAC Set 3 current source 15 (35mA)	Avoid coupling with noise. Route with a thick trace (Imax = 50mA, Rs < 20mOhm).	Route 1 thick trace to modulator bias or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC.
T2	T7_RH0	VDDA_2P5/VSSA	-	DAC Set 2 current sink 7 (65 mA)	Avoid coupling with noise. Route with a thick trace (Imax = 100mA, Rs < 20mOhm).	Route 1 thick trace to modulator, heater, or other destination (with max resistance target < 80m Ohm). Add 1 uF capacitor closest to IC pin per DAC
G9	TCK	VDDIO1/VSSIO		JTAG Clock pin	fmax=50MHz CMOS	Route in module
J9	TDI	VDDIO1/VSSIO		JTAG serial data input	fmax=50MHz CMOS	Route in module
J8	TDO	VDDIO1/VSSIO		JTAG data output	fmax=50MHz CMOS	Route in module
G3	TEMP_DIODE_0	VDDA_2P5/VSSA	-	Internal Current Source to be connected through pad to external temperature diodes		Maintain low resistance between external temp diode ground and PCB ground
H3	TEMP_DIODE_1	VDDA_2P5/VSSA	-	Internal Current Source to be connected through pad to external temperature diodes		Maintain low resistance between external temp diode ground and PCB ground
J3	TEMP_DIODE_2	VDDA_2P5/VSSA	-	Internal Current Source to be connected through pad to external temperature diodes		Maintain low resistance between external temp diode ground and PCB ground
J2	TEMP_DIODE_3	VDDA_2P5/VSSA	-	Internal Current Source to be connected through pad to external temperature diodes		Maintain low resistance between external temp diode ground and PCB ground
H9	TMS	VDDIO1/VSSIO		JTAG mode select pin	fmax=50MHz CMOS	Route in module

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
F7	TM[0]	VDD_2P5/VSSD		Flash Test mode pins		Open
G7	TM[1]	VDD_2P5/VSSD		Flash Test mode pins		Open
H7	TM[2]	VDD_2P5/VSSD		Flash Test mode pins		Open
H6	TM[3]	VDD_2P5/VSSD		Flash Test mode pins		Open
H8	TRST	VDDIO1/VSSIO		JTAG reset pin	fmax=50MHz CMOS	Route in module
H16	UART_RX	VDDIO1/VSSIO		UART receive		1k pull-up to VDDIO1
G16	UART_TX	VDDIO1/VSSIO		UART transmit		1k pull-up to VDDIO1
B14	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply	Combine all VDD_OP9_* pin to 1 plane (Imax=1A, Rs <10mOhm)	Cap - 1x2.2uF , 1x10nF caps between VDD_OP9 & Ground (One pair on each of North, South and West)
F8	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
F9	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
F10	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
F11	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
F12	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
F13	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L8	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L9	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L10	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L11	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L12	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
L13	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply		
R14	VDD_OP9	VDD_2P5_LDO/ VSSD		0.9V digital logic power supply.		
J7	VDD_2P5	VDD_2P5/VSSD		2.5V dedicated power supply for FLASH	Combine all VDD_2P5_* pin to 1 plane (Imax=1A, Rs <10mOhm).	Cap - 1x2.2uF, 1x10nF caps between VDD_2P5 & Ground close to the BGA
G5	VDD_2P5_LDO	VDD_2P5_LDO/ VSSD		2.5V Power supply for Core (0.9V) LDO	Combine all VDD_2P5_LDO* pin to 1 plane (Imax=1A, Rs <10mOhm).	Cap - 1x10uF, 1x1uF, 1x100nF caps between VDD_2P5_LDO & Ground close to the BGA
G6	VDD_2P5_LDO	VDD_2P5_LDO/ VSSD		2.5V Power supply for Core (0.9V) LDO		
B1	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage	Combine all VDDA_2P5_* pins into 1 plane (Imax=2A, Rs <10mOhm).	Cap - 1x10uF, 1x1uF, 1x100nF caps between VDDA_2P5 & Ground close to the BGA (One set on each of North, South, East and West)
C2	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D2	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D3	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D5	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D6	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D8	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D10	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D11	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		

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D12	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
D13	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
E4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
E7	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
E10	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
F4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
G4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
H2	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
H4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
J4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
K4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
L4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
M4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
M7	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
M10	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N2	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N3	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N4	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N5	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N6	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N8	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N10	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N11	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N12	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
N13	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
P2	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
R1	VDDA_2P5	VDDA_2P5/VSSA	-	2.5V Analog Supply Voltage		
J6	VDDA_2P5_ADC	VDDA_2P5_ADC/ VSSA		2.5V Power supply for ADC	Avoid noise coupling. Route with thick metal (Imax=100mA, Rs <10mOhm).	Cap - 2.2uF, 100nF & 10nF caps between VDDA_2P5_ADC & VSSA on substrate;
E15	VDDIO1	VDDIO1/VSSIO	-	VDDIO1 digital IO supply	Combine all VDDIO1_* pins into 1 plane (Imax=1A, Rs <10mOhm).	VDDIO1: Cap - 1x2.2uF, 1x100nF, 1x10nF caps between VDDIO1 & Ground (One pair on each of North, South and West)
G8	VDDIO1	VDDIO1/VSSIO		VDDIO1 digital IO supply		
G13	VDDIO1	VDDIO1/VSSIO		VDDIO1 digital IO supply		
K15	VDDIO1	VDDIO1/VSSIO		VDDIO1 digital IO supply		
H10	VDDIO2	VDDIO2/VSSIO		VDDIO2 digital IO supply	Combine all VDDIO2_* pins into 1 plane (Imax=1A, Rs <10mOhm).	VDDIO2: Cap - 1x2.2uF, 1x100nF, 1x10nF caps between VDDIO2 & Ground close to the BGA

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
K9	VPP	VPP/VSSIO		Flash test supply	Combine all VPP_* pins into 1 plane (Imax=1A, Rs <10mOhm).	VPP should be VDD2P5 or floating. VPP should NOT be connected to VSSD.
K5	VREFP_ADC	VREFP_ADC/AGNDREF_ADC		Positive Reference Voltage for ADC	Avoid noise coupling. Treat ADC_VREF and AGNREF_ADC as matched differential pair.	Cap - 10uF, 1nF, 470pF caps between VREFP_ADC & AGNDREF_ADC, L=30Z: Ferrite bead (e.g., BLM21PG300SN1D from Murata) between VSSA & AGNDREF_ADC
A1	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
A14	VSS	VSSA	-	0V Analog Ground Voltage		
A15	VSS	VSSA	-	0V Analog Ground Voltage		
A16	VSS	VSSA	-	0V Analog Ground Voltage		
B2	VSS	VSSA	-	0V Analog Ground Voltage		
B5	VSS	VSSA	-	0V Analog Ground Voltage		
B8	VSS	VSSA	-	0V Analog Ground Voltage		
B11	VSS	VSSA	-	0V Analog Ground Voltage		
C3	VSS	VSSA	-	0V Analog Ground Voltage		
C6	VSS	VSSA	-	0V Analog Ground Voltage		
C9	VSS	VSSA	-	0V Analog Ground Voltage		
C12	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
D7	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
D9	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
D14	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
E3	VSS	VSSA	-	0V Analog Ground Voltage		
E5	VSS	VSSA	-	0V Analog Ground Voltage		
E8	VSS	VSSA	-	0V Analog Ground Voltage		
E9	VSS	VSSA	-	0V Analog Ground Voltage		
E11	VSS	VSSA	-	0V Analog Ground Voltage		
E12	VSS	VSSA	-	0V Analog Ground Voltage		
E13	VSS	VSSA	-	0V Analog Ground Voltage		
E14	VSS	VSSA	-	0V Analog Ground Voltage		
G10	VSS	VSSA	-	0V Analog Ground Voltage		
H1	VSS	VSSA	-	0V Analog Ground Voltage		
H5	VSS	VSSA	-	0V Analog Ground Voltage		

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BGA Ball #	Pin Name	Domain	Default	Description	FCCSP Routing Note	PCB Routing Note
H15	VSS	VSSA	-	0V Analog Ground Voltage	Maintain separate planes for each VSSA_*, VSSD_*, VSSIO_* on substrate. Tie VSSA/VSSD/VSSIO together on PCB.	Combine VSSA/VSSD/VSSIO together in a strong plane.
K1	VSS	VSSA	-	0V Analog Ground Voltage		
K3	VSS	VSSA	-	0V Analog Ground Voltage		
K8	VSS	VSSA	-	0V Analog Ground Voltage		
L5	VSS	VSSA	-	0V Analog Ground Voltage		
M3	VSS	VSSA	-	0V Analog Ground Voltage		
M5	VSS	VSSA	-	0V Analog Ground Voltage		
M6	VSS	VSSA	-	0V Analog Ground Voltage		
M8	VSS	VSSA	-	0V Analog Ground Voltage		
M9	VSS	VSSA	-	0V Analog Ground Voltage		
M11	VSS	VSSA	-	0V Analog Ground Voltage		
M12	VSS	VSSA	-	0V Analog Ground Voltage		
M13	VSS	VSSA	-	0V Analog Ground Voltage		
N7	VSS	VSSA	-	0V Analog Ground Voltage		
N9	VSS	VSSA	-	0V Analog Ground Voltage		
P3	VSS	VSSA	-	0V Analog Ground Voltage		
P6	VSS	VSSA	-	0V Analog Ground Voltage		
P9	VSS	VSSA	-	0V Analog Ground Voltage		
P12	VSS	VSSA	-	0V Analog Ground Voltage		
P16	VSS	VSSA	-	0V Analog Ground Voltage		
R2	VSS	VSSA	-	0V Analog Ground Voltage		
R5	VSS	VSSA	-	0V Analog Ground Voltage		
R8	VSS	VSSA	-	0V Analog Ground Voltage		
R11	VSS	VSSA	-	0V Analog Ground Voltage		
T1	VSS	VSSA	-	0V Analog Ground Voltage		
T14	VSS	VSSA	-	0V Analog Ground Voltage		
T16	VSS	VSSA	-	0V Analog Ground Voltage		
K6	VSUP_ADC_EXT	VSUP_ADC_EXT /VSSA		Analog power supply for ADC	Avoid noise coupling. Route with thick metal (Imax=100mA, Rs <10mOhm).	



7 Register details

7.1 Flash controller

7.1.1 List of registers and offset details

Base Address : FLASH_CNTRL_BASE

Table 25 : Flash controller register list

Register Name	Access Read/Write	Address
Flash Controller Configuration Registers		
IP Version Register (FLASH_CNTRL_VER)	Read	0x00
Interrupt Status Register (FLASH_CNTRL_INT_STA)	Read/Write	0x04
Interrupt Mask Register (FLASH_CNTRL_INT_MASK)	Read/Write	0x08
Memory Configuration Register (FLASH_MEM_CFG_REG)	Read/Write	0x0C
Flash Command Register (FLASH_MEM_CMD)	Read/Write	0x10
Flash Program Address (FLASH_MEM_PROG_ADDR)	Read/Write	0x14
Flash Program Data (FLASH_MEM_PROG_DATA)	Read/Write	0x18
Flash Erase Error Address (FLASH_MEM_ERASE_EADDR)	Read/Write	0x20
Flash Erase Address (FLASH_MEM_ERASE_ADDR)	Read/Write	0x40
Flash Timing Register		
Timing Register 1	Read/Write	0x24
Timing Register 2	Read/Write	0x28
Timing Register 3	Read/Write	0x2C
Timing Register 4	Read/Write	0x30
Timing Register 5	Read/Write	0x34
Timing Register 6	Read/Write	0x38
Timing Register 7	Read/Write	0x3C
Flash erase/program lock register (FLASH_MEM_LOCK)	Read/Write	0x50



7.1.2 Register definition

7.1.2.1 IP Version Register (FLASH_CNTRL_VER)

The IP version register contains the information of the IP Version

Bit #	Type	Name	Comments	Default
7:0	RO	Minor Version Number	Minor Version ID. Is incremented for small metal fixes on IP	8'h0
15-8	RO	Major Version Number	Major Version ID. Is incremented on feature enhancements, bug fixes beyond metal fixes etc.	8'h0
31-16	RO	Reserved	Reserved	16'h0

MINOR VERSION NUMBER:

This is the minor version number. This is incremented on any small changes/bug fixes on the IP that can be implemented as a metal fix

MAJOR VERSION NUMBER:

This is the major version number of the IP. It is incremented on major bug fixes or enhancements that cannot be implemented with a metal fix.

Bit #	Type	Name	Comments	Default
0	RO/Co W1	ERASE_COMPLETE	Interrupt indicating that an erase operation has completed	1'b0
1	RO/Co W1	ERASE_ERROR	Interrupt indicating that the erase operation has an error	1'b0
2	RO/Co W1	PROGRAM_COMPLETE	Interrupt indicating a program operation is complete	1'b0
3	RO/Co W1	PROGRAM_ERROR	Interrupt indicating that the program operation has completed with error	1'b0
4	RO/Co W1	PROGRAM_NOT_POSSIBLE	Interrupt indicating that program is not possible because of a 0 value in a bit location which is going to be programmed by 1	1'b0
5	RO	Reserved		1'b0
6	RO	Reserved		1'b0
7	RO/Co W1	ADDR_BOUND_ERROR	Interrupt indicating that an out of range memory access has	1'b0



Bit #	Type	Name	Comments	Default
			happened either in flash or configuration space.	
8	RO/Co W1	AHB_FLASH_WRITE_ERROR	Interrupt indicating an AHB write is directly initiated to Flash Memory	1'b0
31: 9	RO	Reserved	Reserved	23'h0

7.1.2.2 Interrupt Status Register (FLASH_CNTRL_INT_STA)

The Interrupt Status register stores the status of various interrupt sources to the CPU. The interrupt bits are selectively or in group cleared by writing 1s to the required interrupt status bits. An interrupt mask register is provided to individually mask the bits that cause assertion of the interrupt line. However, the status register values are not masked by the mask register and a read of the register will show even those interrupts that are masked.

ERASE_COMPLETE:

This interrupt status bit indicates an erase operation is complete. Write 1 to clear the interrupt. Writing a 0 by the processor will not have any impact on the status of this bit.

ERASE_ERROR:

This interrupt status bit indicates an erase that has been attempted has not completed successfully. The state machine reads back the pages/ entire memory that has been erased to confirm if the data is all 1, and if not it sets the Error interrupt. Write 1 to clear the interrupt. Writing a 0 by the processor will not have any impact on the status of this bit.

PROGRAM_COMPLETE:

This bit indicates completion of a program operation. This bit is cleared by processor by writing 1 to this bit location. Writing a 0 by the processor will not have any impact on the status of this bit.

PROGRAM_ERROR:

This bit indicates that the program operation has completed with an error. The state machine reads back the location, which has been programmed, and if the data does not match the intended data, it sets this error interrupt. This bit is cleared by processor by writing 1 to this bit location. Writing a 0 by the processor will not have any impact on the status of this bit.

PROGRAM_NOT_POSSIBLE:

This bit indicates that the program operation is not possible, because a bit location that is attempted to be programmed to 1 has a 0. The state machine reads the location before programming and if any bit location, which is already 0, is trying to be programmed to 1, it sets this error interrupt. TSMC flash does not allow more than two consecutive programs to the same location before an erase. This bit is cleared by



processor by writing 1 to this bit location. Writing a 0 by the processor will not have any impact on the status of this bit.

ADDR_BOUND_ERROR:

This bit indicates a memory access other than the address range specified error has occurred in either configuration space or flash memory. It is indicated by writing logic 1 to this bit

AHB_FLASH_WRITE_ERROR:

A write access to flash memory address by the AHB slave is an illegal transfer. This bit indicates an error caused by the above problem. It is indicated by writing logic 1 to this bit.



7.1.2.3 Interrupt Mask Register (FLASH_CNTRL_INT_MASK)

This register is used to mask the interrupt line

Interrupt Mask Register, address 0x08				
Bit #	Type	Name	Comments	Default
0	R/W	ERASE_COMPLETE_MASK	Mask Erase complete interrupt	1'b0
1	R/W	ERASE_ERROR_MASK	Mask the Erase Error interrupt	1'b0
2	R/W	PROGRAM_COMPLETE_MASK	Mask program complete interrupt	1'b0
3	R/W	PROGRAM_ERROR_MASK	Mask the program error interrupt	1'b0
4	R/W	PROGRAM_NOT_POSSIBLE_MASK	Mask the program not possible interrupt	1'b0
5	RO	Reserved		1'b0
6	RO	Reserved		1'b0
7	R/W	ADDR_BOUND_ERROR_MASK	Mask the address bound error interrupt	1'b0
8	R/W	AHB_FLASH_WRITE_ERROR_MASK	Mask the Interrupt indicating an AHB write directly initiated to Flash Memory	1'b0
31: 9	RO	Reserved	Reserved	23'h0

ERASE_COMPLETE_MASK:

Write a 1 to mask Erase complete status from causing a hardware interrupt

ERASE_ERROR_MASK:

Write a 1 to mask Erase Error from causing a hardware interrupt

PROGRAM_COMPLETE_MASK:

Write a 1 to mask program complete status from causing a hardware interrupt.

PROGRAM_ERROR_MASK:

Write a 1 to mask program error from causing a hardware interrupt.

PROGRAM_NOT_POSSIBLE_MASK:

Write a 1 to mask program not possible error from causing a hardware interrupt.

ADDR_BOUND_ERROR_MASK:

Write a 1 to mask address bound occurred status from causing a hardware interrupt.

AHB_FLASH_WRITE_ERROR_MASK:



Write a 1 to mask illegal direct write access to flash memory occurred status from causing a hardware interrupt.

7.1.2.4 Memory Configuration Register (FLASH_MEM_CFG_REG)

This register is used to configure the memory size, page size etc. Also used to enable/disable ECC and configure between access to information region or normal memory region.

Memory Configuration Register, address 0x0C				
Bit #	Type	Name	Comments	Default
1:0	RO	Y_ADDRESS_WIDTH[1:0]	Indicates the size of YMUX	Instantiated parameter value
5:2	RO	WL_ADDRESS_WIDTH[3:0]	Indicates the Word Line Address width,	Instantiated parameter value
7:6	RO	IO_WIDTH[1:0]	Indicates the IO Width that is configured	Instantiated parameter value
8	R/W	IFREN	1= Access is to Information block	1'b0
9	R/W	REDEN	1= Access is to redundancy block IFREN=0, REDEN=0 is to access main memory	1'b0
11:10	RO	PAGE_SIZE[1:0]	Indicates the number of rows in a page	Instantiated parameter value
12	R/W	SLM_EN	Asserted high for sleep mode	1'b0
31:13	RO	Reserved	Reserved	14'b0

Y_ADDRESS_WIDTH[1:0]:

This is a read only field indicating the Y MUX Size. The value reflects the parameter tie off for the IP when instantiated

00 – Y MUX = 32

01 – YMUX = 64

10 – YMUX = 128

11 – YMUX = 256

WL_ADDRESS_WIDTH[3:0]:

Word Line indicates the number of Word lines relevant for flash. The value reflects the parameter tie off when the IP is instantiated



0000 to 0010 - Reserved

0011 – 8 word lines

0100 – 16 Word lines

....

1011 – 2048 word lines

1100 – 4096 word lines

1101 to 1111 - Reserved

IO_WIDTH[1:0]:

Indicates the memory IO Width. The value reflects the parameter tie off when the IP is instantiated

00 to 01 - Reserved

10 – IO Width of 32

11 – IO Width of 64

IFREN:

Indicates whether transfer is to Information block

1 – Transfer to Information Block

REDEN:

Indicates whether transfer is to redundancy block

1 – Transfer to Redundancy Block

In case of IFREN=0 and REDEN=0, transfer to Main Memory Block

PAGE_SIZE[1:0]:

Indicates the number of rows in a page. The value reflects the parameter tie off when the IP is instantiated.

00 – 4 rows per page.

01 – 8 rows per page.

10 – 16 rows per page.

11 – 32 rows per page.



7.1.2.5 Flash Command Register (FLASH_MEM_CMD)

This register holds the command that needs to be executed to the flash.

Flash Command Register, read/write, address 0x10				
Bit #	Type	Name	Comments	Default
1:0	R/W	FLASH_COMMAND	The Flash Command that need to be executed.	2'h0
31:2	R/W	Reserved	Reserved	30'h0

FLASH_COMMAND[1:0]:

This field stores the command to be executed. Firmware would need to program all relevant registers before configuring this field. Once the register is written, it gets auto resets to 0

2'b00 – No Command

2'b01 – Program

2'b10 – Erase

2'b11 – Mass Erase

7.1.2.6 Flash Program Address (FLASH_MEM_PROG_ADDR)

The flash address register stores the address of location that need to be programmed.

Flash Address, read/write, address 0x14				
Bit #	Type	Name	Comments	Default
21:0	R/W	PROGRAM_ADDRESS	Program Memory Address. This value is used during program of flash. {8'h_page_addr, 2'h_wl_addr, 7'h_ymux_addr, 1'b_msb_lsb_wd_addr, 2'b00}	22'b0
31:23	R/W	Reserved	Reserved	10'b0

PROGRAM_ADDRESS[21:0]:

Stores the Address that is relevant for a program operation



7.1.2.7 Flash Program Data (FLASH_MEM_PROG_DATA)

This register stores the flash program 32 bit data. In case the flash IO Width is 32 or 64, only this register is valid.

Flash Program Data, address 0x18				
Bit #	Type	Name	Comments	Default
31:0	R/W	FLASH_MEM_PROG_DATA	Stores the Flash program 32-bit data Least.	32'b0

FLASH_MEM_PROG_DATA[31:0]:

32 bit data that need to be programmed to flash. In case the flash is only 32 bit wide, then this register is alone valid. In case that IO_WIDTH=64, this 32-bit data concatenated with 32'hffff_ffff to form the 64-bit data to be programmed. If Flash_MEM_PROG_ADDR[2]=1, the 64 bit data will be {FLASH_MEM_PROG_DATA, 32'hffff_ffff}, otherwise it will be {32'hffff_ffff, FLASH_MEM_PROG_DATA}.

7.1.2.8 Flash Erase Address (FLASH_MEM_ERASE_ADDR)

The flash address register stores the address of location that need to be erased.

Flash Erase Address 0x40				
Bit #	Type	Name	Comments	Default
11:0	R/W	PROGRAM_ADDRESS	Page erase address. {8'h_page_addr, 4'h_wl_addr}	12'b0
31:12	R/W	Reserved	Reserved	20'b0

ERASE_ADDRESS[11:0]:

Stores the erase page address



7.1.2.9 Erase Error Address

This register stores the Address where an Erase error has occurred

Erase Error Address, address 0x20				
Bit #	Type	Name	Comments	Default
23:0	RO	ERASE_ERROR_ADDRESS	Stores the address where an erase operation Error has occurred	24'hC0_0000
31-24	RO	Reserved	Reserved	8'h0

ERASE_ERROR_ADDRESS[23:0]:

This register contains the address location where an erase error has occurred.

- [23:22] specify whether there exist erase error, if so, which flash block has erase error?
 - 2'b11: No errors
 - 2'b00: Main memory has erase error
 - 2'b01: Redundant block has erase error
 - 2'b10: Information block has erase error
- [21:10]: XADDR
- [9:3]: YADDR
- [2:0]: Tied off

7.1.2.10 Timing Register 1

Flash Timing Register 1

Timing Register 1 , address 0x24				
Bit #	Type	Name	Comments	Default
3:0	R/W	Tacc_count[3:0]	Counter value for determining Data read access time.	4'd10 (180MHz) 4'd5 (100MHz)
7:4	R/W	Tpws_count[3:0]	Counter value for positive pulse of SE	4'd4 (180MHz) 4'd2 (100MHz)
11:8	R/W	Tnws_count[3:0]	Counter value for negative pulse of SE	4'd5 (180MHz) 3'd3 (100MHz)



Timing Register 1 , address 0x24				
Bit #	Type	Name	Comments	Default
15:12	R/W	Txys_count[3:0]	Counter value for setup time for XE/YE/LVE/IFREN1 to SE	4'd3 (180MHz) 4'd2 (100MHz)
31:16	R	Reserved	Reserved	16'd0

TACC_COUNT[3:0]:

This value provides the number of equivalent system clock cycles after which the data will be available on DOUT after any edge transition of signals IFREN, XADR, YADR, XE, YE, and SE.

TPWS_COUNT[3:0]:

This value provides the number of equivalent system clock cycles for which the positive pulse of SE lasts.

TNWS_COUNT[3:0]:

This value provides the number of equivalent system clock cycles for which the negative pulse of SE lasts.

TXYS_COUNT[3:0]

This value provides the number of equivalent system clock cycles of the setup time for XE/YE/LVE/IFREN1 to SE.

7.1.2.11 Timing Register 2

Flash Timing register 2

Timing Register 2 , address 0x28				
Bit #	Type	Name	Comments	Default
15:0	R/W	Tnvs_count[15:0]	Counter value for determining PROG/ERASE to NVSTR set up time.	16'h06A0 (180MHz) 16'h0350 (100MHz)
31:16	R/W	Tnvh_count[15:0]	Counter value for determining NVSTR hold time.	16'h0430 (180MHz) 16'h0218 (100MHz)



TNVS_COUNT[15:0]:

This value provide the minimum number of equivalent system clock cycles for which the PROG/ERASE signal has to be asserted before asserting the NVSTR signal for a program or erase operation.

TNVH_COUNT[15:0]:

This value provides the minimum number of equivalent system clock cycles after which the NVSTR signal can be de-asserted after the de assertion of PROG/ERASE for a program/erase operation.

7.1.2.12 Timing Register 3

Flash timing register 3

Timing Register 3 , address 0x2C				
Bit #	Type	Name	Comments	Default
15:0	R/W	Tnvh1_count[15:0]	Counter value for determining NVSTR hold time (mass erase)	16'h5520 (180MHz) 16'h2910 (100MHz)
31:16	R/W	Tprog_count[15:0]	Counter value for determining Program time.	16'h09E0 (180MHz) 16'h04F0 (100MHz)

TNVH1_COUNT[15:0]:

This value provides the minimum number of equivalent system clock cycles after which the NVSTR signal can be de-asserted after the de assertion ERASE in case of mass erase.

TPROG_COUNT[15:0]:

This value provides the minimum number of equivalent system clock cycles for which YE should be high to enable a program operation

7.1.2.13 Timing Register 4

Flash Timing register 4



Timing Register 4 , address 0x30				
Bit #	Type	Name	Comments	Default
15:0	R/W	Tpgs_count[15:0]	Counter value for determining program set up time.	16'h01B0 (180MHz) 16'h00D8 (100MHz)
20:16	R/W	Tphg_count[4:0]	Counter value for determining Program hold time.	5'h5 (180MHz) 5'h3 (100MHz)
25:21	R/W	Twpr_count[4:0]	Counter value for determining Write prepare time.	5'h1 for both freq.
30:26	R/W	Twhd_count[4:0]	Counter value for determining Write hold time.	5'h1 for both freq.

TPGS_COUNT[15:0]:

This value provides the minimum number of equivalent system clock cycles for which the NVSTR should be kept asserted before YE is asserted for programming an address.

TPGH_COUNT[4:0]:

This value provides the minimum number of equivalent system clock cycles after which the PROG signal can be deasserted after the YE signal is de-asserted after a program operation.

TWPR_COUNT[4:0]:

This will provide the number of equivalent system clock cycles for which the system has to wait before the assertion of ERASE/PROG. I.e., this is the minimum wait time required before an erase or programming process is being initiated after a read operation.

TWHD_COUNT[3:0]:

This will provide the minimum number of equivalent system clock cycles for which all SE, IFREN, XADDR and XE should be kept constant after the de assertion of NVSTR.



7.1.2.14 Timing Register 5

Flash Timing register 5

Timing Register 5, address 0x34				
Bit #	Type	Name	Comments	Default
23:0	R/W	Terase_count[23:0]	Counter value for determining Erase time.	24'h30_10B0 (180MHz) 24'h18_0858 (100MHz)
27:24	R/W	Tads_count[3:0]	Counter value for determining Address/data set up time.	4'h5 (180MHz) 4'h3 (100MHz)
31:28	R/W	Tadh_count[3:0]	Counter value for determining Address/data hold time.	4'h5 (180MHz) 4'h3 (100MHz)

TERASE_COUNT[23:0]:

This value provides the minimum number of equivalent system clock cycles for which the ERASE signal should be kept asserted after the assertion of NVSTR for an erase to take place.

TADS_COUNT[3:0]:

This will provide the minimum number of equivalent system clock cycles for which the Address and Data are to be stable before programming is enabled (selected) by asserting YE.

TADH_COUNT[3:0]:

This will provide the minimum number of equivalent system clock cycles for which the Address and data are to be kept stable after the YE is de-asserted.

7.1.2.15 Timing Register 6

Flash timing register 6

Timing Register 6 , address 0x38				
Bit #	Type	Name	Comments	Default
15:0	R/W	Trcv_count[15:0]	Counter value for determining Recovery time.	16'h840 (180MHz) 16'h420 (100MHz)



Timing Register 6 , address 0x38				
Bit #	Type	Name	Comments	Default
19:16	R/W	Tcps_count[3:0]	Counter value for determining Control to PROG/ERASE set-up time.	4'h1 for both freq.
23:20	R/W	Txyh_count[3:0]	Counter value for hold time for XE/YE	4'h1 for both freq.

TRCV_COUNT[15:0]:

This value provides the minimum number of equivalent system clock cycles for which the signal NVSTR has to be de-asserted till the next active state.

TCPS_COUNT[3:0]:

This value provides the minimum number of equivalent system clock cycles for which the control signals like address, select etc. are to be stable before the next active edge of PROG/ERASE.

TXYH_COUNT[3:0]:

This value provides the minimum number of equivalent system clock cycles for which XE/YE stays high when the output data for flash is a valid.

7.1.2.16 Timing Register 7

Flash Timing register 7

Timing Register 7, address 0x3C				
Bit #	Type	Name	Comments	Default
23:0	R/W	Tme_count[23:0]	Counter value for determining Mass erase time.	24'h30_10B0 (180MHz) 24'h18_0858 (100MHz)

TME_COUNT[23:0]:

This value provides the number of equivalent system clock cycles in mass erase case for which the ERASE signal should be asserted after the assertion of NVSTR for a mass erase to take place.



Table 26 Flash Timing Register Values for Different Frequencies

		Bit #	50MHz	100MHz	150MHz	180MHz	200MHz	220MHz
TIMING1	Tacc_count[3:0]	[3:0]	4'd5	4'd5	4'd7	4'd10	4'd11	4'd12
	Tpws_count[3:0]	[7:4]	4'd2	4'd2	4'd4	4'd4	4'd5	4'd6
	Tnws_count[3:0]	[11:8]	4'd3	4'd3	4'd4	4'd5	4'd6	4'd6
	Txys_count[3:0]	[15:12]	4'd2	4'd2	4'd3	4'd3	4'd4	4'd4
	Flash_TIMING1	[31:0]	0x2325	0x2325	0x3447	0x354A	0x465B	0x466C
TIMING2	Tnvs_count[15:0]	[15:0]	0x1A80	0x03500	0x04F8	0x06A0	0x075C	0x0818
	Tnvs_count[15:0]	[31:16]	0x010C	0x0218	0x0324	0x0430	0x04A8	0x051E
	Flash_TIMING2	[31:0]	0x010C1A80	0x02180350	0x032404F8	0x043006A0	0x04A8075C	0x051E0818
TIMING3	Tnvh1_count[15:0]	[15:0]	0x1488	0x2910	0x3D98	0x5520	0x5E96	0x680A
	Tprog_count[15:0]	[31:16]	0x0258	0x04F0	0x0768	0x09E0	0xAF9	0xC12
	Flash_TIMING3	[31:0]	0x02581488	0x04F02910	0x07683D98	0x09E05520	0xAF95E96	0xC12680A
TIMING4	Tpgs_count[15:0]	[15:0]	0x006C	0x00D8	0x0144	0x01B0	0x01E0	0x0210
	Tphg_count[4:0]	[20:16]	5'h3	5'h3	5'h4	5'h5	5'h5	5'h5
	Twpr_count[4:0]	[25:21]	5'h1	5'h1	5'h1	5'h1	5'h1	5'h1
	Twhd_count[4:0]	[30:26]	5'h1	5'h1	5'h1	5'h1	5'h1	5'h1
	Flash_TIMING4	[31:0]	0x0423006C	0x042300D8	0x04240144	0x042501B0	0x042501E0	0x04250210
TIMING5	Terase_count[23:0]	[23:0]	24'h0B_71B0	24'h18_0858	24'h24_0C84	24'h30_10B0	24'h35_67E0	24'h3A_BF10
	Tads_count[3:0]	[27:24]	4'h3	4'h3	4'h4	4'h5	4'h6	4'h6
	Tadh_count[3:0]	[31:28]	4'h3	4'h3	4'h4	4'h5	4'h6	4'h6
	Flash_TIMING5	[31:0]	0x330B71B0	0x33180858	0x44240C84	0x553010B0	0x663567E0	0x663ABF10
TIMING6	Trcv_count[15:0]	[15:0]	0x210	0x0420	0x0630	0x840	0x092B	0xA16
	Tcps_count[3:0]	[19:16]	4'h1	4'h1	4'h1	4'h1	4'h1	4'h1
	Txyh_count[3:0]	[23:20]	4'h1	4'h1	4'h1	4'h1	4'h1	4'h1
	Flash_TIMING6	[31:0]	0x00110210	0x00110420	0x00110630	0x00110840	0x0011092B	0x00110A16
TIMING7	Tme_count[23:0]	[23:0]	24'h0B_71B0	24'h18_0858	24'h24_0C84	24'h30_10B0	24'h35_67E0	24'h3A_BF10
	Flash_TIMING7	[31:0]	0x000B71B0	0x00180858	0x00240C84	0x003010B0	0x003567E0	0x003ABF10



7.1.2.17 Flash erase/program lock (FLASH_MEM_LOCK)

Bit #	Type	Name	Comments	Default
15:0	RW	FLASH_MEM_LOCK	<p>Write : This provide the key and lock feature for the flash program and erase commands. When the 0xF1A1 is written to this register flash is enabled for the above mentioned commands. The lock is automatically cleared when the given flash operation is done. If non 0xF1A1 is written flash erase or program is disabled.</p> <p>Read: Indicates the state of the lock transferred</p> <ul style="list-style-type: none"> 000 : No operation in progress 001 : flash_mem_lock is unlocked (indicates that the write happened to this register with signature 0xF1A1). write to FLASH_MEM_CMD is only allowed when flash_mem_lock==3'b001. 010 : Flash erase/program in progress. 011 : Flash erase/program is done 100 : Flash erase/program is disabled until next reset. 	2'h0
31:16	RO	Reserved		0

7.2 Timer

7.2.1 List of registers and offset details

Base Address : APB_TIMER_BASE

Only three timer exist in the PMIC instance.



Register	Offset	Memory Access	Description
TIMER1LOADCOUNT	0x0	RW	Value After Reset: 0x0 Name: Timer1 Load Count Register Size: 8-32 bits Read/Write Access: Read/Write
TIMER1CURRENTVAL	0x4	RO	Value After Reset: 0x0 Name: Timer1 Current Value Size: 8-32 bits Read/Write Access: Read
TIMER1CONTROLREG	0x8	RW	Value After Reset: 0x0 Name: Timer1 Control Register Size: 3 bits Address Offset: 8 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer1. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.
TIMER1EOI	0xC	RO	Value After Reset: 0x0 Name: Timer1 End-of-Interrupt Register Size: 1 bit Read/Write Access: Read
TIMER1INTSTAT	0x10	RO	Value After Reset: 0x0 Name: Timer1 Interrupt Status Register Size: 1 bit Read/Write Access: Read
TIMER2LOADCOUNT	0x14	RW	Value After Reset: 0x0 Name: Timer2 Load Count Register Size: 8-32 bits Read/Write Access: Read/Write
TIMER2CURRENTVAL	0x18	RO	Value After Reset: 0x0 Name: Timer2 Current Value Register Size: 8-32 bits Read/Write Access: Read



TIMER2CONTROLREG	0x1C	RW	Value After Reset: 0x0 Name: Timer2 Control Register Size: 3 bits Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer2. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.
TIMER2EOI	0x20	RO	Value After Reset: 0x0 Name: Timer2 End-of-Interrupt Register Size: 1 bit Read/Write Access: Read
TIMER2INTSTAT	0x24	RO	Value After Reset: 0x0 Name: Timer2 Interrupt Status Register Size: 1 bit Read/Write Access: Read
TIMER3LOADCOUNT	0x28	RW	Value After Reset: 0x0 Name: Timer1 Load Count Register Size: 8-32 bits Read/Write Access: Read/Write
TIMER3CURRENTVAL	0x2C	RO	Value After Reset: 0x0 Name: Timer3 Current Value Register Size: 8-32 bits Read/Write Access: Read
TIMER3CONTROLREG	0x30	RW	Value After Reset: 0x0 Name: Timer3 Control Register Size: 3 bits Address Offset: 48 Read/Write Access: Read/Write This register controls enabling, operating mode (free-running or defined-count), and interrupt mask of Timer3. You can program each Timer1ControlReg to enable or disable a specific timer and to control its mode of operation.
TIMER3EOI	0x34	RO	Value After Reset: 0x0 Name: Timer1 End-of-Interrupt Register Size: 1 bit Read/Write Access: Read



TIMER3INTSTAT	0x38	RO	Value After Reset: 0x0 Name: Timer3 Interrupt Status Register Size: 1 bit Read/Write Access: Read
TIMERSINTSTAT	0xA0	RO	Value After Reset: 0x0 Name: Timers Interrupt Status Register Size: 1-9 bits Read/Write Access: Read
TIMERSEOI	0xA4	RO	Value After Reset: 0x0 Name: Timers End-of-Interrupt Register Size: 1-9 bits Read/Write Access: Read
TIMERSRAWINTSTAT	0xA8	RO	Value After Reset: 0x0 Name: Timers Raw Interrupt Status Register Size: 1-9 bits Read/Write Access: Read
TIMERSCOMPVERSION	0xAC	RO	Value After Reset: 0x3231322A Name: Timers Component Version Register Size: 32 bits Read/Write Access: Read
TIMER1PROTLEVEL	0xD0	RW	Value After Reset: 0x2 Name: Timer1 protection level Register Size: 32 bits Read/Write Access: Read/Write
TIMER2PROTLEVEL	0xD4	RW	Value After Reset: 0x2 Name: Timer2 protection level Register Size: 32 bits Read/Write Access: Read/Write
TIMER3PROTLEVEL	0xD8	RW	Value After Reset: 0x2 Name: Timer3 protection level Register Size: 32 bits Read/Write Access: Read/Write

7.2.2 Register definition

7.2.2.1 TIMER1LOADCOUNT

Bit #	Type	Name	Comments	Default
31:0	RW	TIMER1LOADCOUNT	Value to be loaded into Timer1. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.	32'h0



7.2.2.2 TIMER1CURRENTVAL

Bit #	Type	Name	Comments	Default
31:0	RO	TIMER1CURRENTVAL	Current Value of Timer1. This register is supported only when timer_1_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.	32'h0

7.2.2.3 TIMER1CONTROLREG

Bit #	Type	Name	Comments	Default
0	RW	TIMER_ENABLE	Timer enable bit for Timer1	0
1	RW	TIMER_MODE	Timer mode for Timer1	0
2	RW	TIMER_INTERRUPT_MASK	Timer interrupt mask for Timer1	0
31:3	RO	RESERVED	Reserved for future use.	32'h0

TIMER_ENABLE:

0x1 (ENABLED): Timer 1 is enabled
 0x0 (DISABLE): Timer 1 is disabled

TIMER_MODE:

You must set the Timer1LoadCount register to all 1s before enabling the timer in free-running mode.
 0x1 (USER_DEFINED): User-Defined mode of operation
 0x0 (FREE_RUNNING): Free Running mode of operation

TIMER_INTERRUPT_MASK:

0x1 (MASKED): Timer 1 interrupt is masked
 0x0 (UNMASKED): Timer 1 interrupt is unmasked

7.2.2.4 TIMER1EOI

Bit #	Type	Name	Comments	Default
0	RO	TIMER1EOI	Reading from this register returns all zeroes (0) and clears the interrupt from Timer1.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0



7.2.2.5 TIMER1INTSTAT

Bit #	Type	Name	Comments	Default
0	RO	TIMER1INTSTATUS	Contains the interrupt status for Timer 1.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0

TIMER1INTSTATUS:

- 0x1 (ACTIVE): Timer 1 Interrupt is active
- 0x0 (INACTIVE): Timer 1 Interrupt is inactive

7.2.2.6 TIMER2LOADCOUNT

Bit #	Type	Name	Comments	Default
31:0	RW	TIMER2LOADCOUNT	Value to be loaded into Timer2. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.	32'h0

7.2.2.7 TIMER2CURRENTVAL

Bit #	Type	Name	Comments	Default
31:0	RO	TIMER2CURRENTVAL	Current Value of Timer2. This register is supported only when timer_2_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.	32'h0

7.2.2.8 TIMER2CONTROLREG

Bit #	Type	Name	Comments	Default
0	RW	TIMER_ENABLE	Timer enable bit for Timer2	0
1	RW	TIMER_MODE	Timer mode for Timer2	0
2	RW	TIMER_INTERRUPT_MASK	Timer interrupt mask for Timer2	0
31:3	RO	RESERVED	Reserved for future use.	32'h0

TIMER_ENABLE:

- 0x1 (ENABLED): Timer 2 is enabled



0x0 (DISABLE): Timer 2 is disabled

TIMER_MODE:

You must set the Timer2LoadCount register to all 1s before enabling the timer in free-running mode.

0x1 (USER_DEFINED): User-Defined mode of operation

0x0 (FREE_RUNNING): Free Running mode of operation

TIMER_INTERRUPT_MASK:

0x1 (MASKED): Timer 2 interrupt is masked

0x0 (UNMASKED): Timer 2 interrupt is unmasked

7.2.2.9 TIMER2EOI

Bit #	Type	Name	Comments	Default
0	RO	TIMER2EOI	Reading from this register returns all zeroes (0) and clears the interrupt from Timer2.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0

7.2.2.10 TIMER2INTSTAT

Bit #	Type	Name	Comments	Default
0	RO	TIMER2INTSTATUS	Contains the interrupt status for Timer 2.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0

TIMER2INTSTATUS:

0x1 (ACTIVE): Timer 2 Interrupt is active

0x0 (INACTIVE): Timer 2 Interrupt is inactive

7.2.2.11 TIMER3LOADCOUNT

Bit #	Type	Name	Comments	Default
31:0	RW	TIMER3LOADCOUNT	Value to be loaded into Timer3. This is the value from which counting commences. Any value written to this register is loaded into the associated timer.	32'h0

7.2.2.12 TIMER3CURRENTVAL



Bit #	Type	Name	Comments	Default
31:0	RO	TIMER2CURRENTVAL	Current Value of Timer3. This register is supported only when timer_3_clk is synchronous to pclk. Reading this register when using independent clocks results in an undefined value.	32'h0

7.2.2.13 TIMER3CONTROLREG

Bit #	Type	Name	Comments	Default
0	RW	TIMER_ENABLE	Timer enable bit for Timer3	0
1	RW	TIMER_MODE	Timer mode for Timer3	0
2	RW	TIMER_INTERRUPT_MASK	Timer interrupt mask for Timer3	0
31:3	RO	RESERVED	Reserved for future use.	32'h0

TIMER_ENABLE:

0x1 (ENABLED): Timer 3 is enabled
0x0 (DISABLE): Timer 3 is disabled

TIMER_MODE:

You must set the Timer3LoadCount register to all 1s before enabling the timer in free-running mode.

0x1 (USER_DEFINED): User-Defined mode of operation
0x0 (FREE_RUNNING): Free Running mode of operation

TIMER_INTERRUPT_MASK:

0x1 (MASKED): Timer 3 interrupt is masked
0x0 (UNMASKED): Timer 3 interrupt is unmasked

7.2.2.14 TIMER3EOI

Bit #	Type	Name	Comments	Default
0	RO	TIMER2EOI	Reading from this register returns all zeroes (0) and clears the interrupt from Timer3.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0

7.2.2.15 TIMER3INTSTAT

Bit #	Type	Name	Comments	Default
0	RO	TIMER2INTSTATUS	Contains the interrupt status for Timer 3.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0



TIMER2INTSTATUS:

- 0x1 (ACTIVE): Timer 2 Interrupt is active
- 0x0 (INACTIVE): Timer 2 Interrupt is inactive

7.2.2.16 TIMERSINTSTAT

Bit #	Type	Name	Comments	Default
2:0	RO	TIMERSINTSTATUS	Contains the interrupt status of all timers in the component.	3'h0
31:3	RO	RESERVED	Reserved for future use.	29'h0

TIMERSINTSTATUS:

If a bit of this register is 0, then the corresponding timer interrupt is not active and the corresponding interrupt could be on either the timer_intr bus or the timer_intr_n bus, depending on the interrupt polarity you have chosen. Similarly, if a bit of this register is 1, then the corresponding interrupt bit has been set in the relevant interrupt bus. In both cases, the status reported is the status after the interrupt mask has been applied. Reading from this register does not clear any active interrupts:

- 0 = either timer_intr or timer_intr_n is not active after masking
- 1 = either timer_intr or timer_intr_n is active after masking.

7.2.2.17 TIMERSEOI

Bit #	Type	Name	Comments	Default
2:0	RO	TIMERSEOI	Reading this register returns all zeroes (0) and clears all active interrupts.	3'h0
31:3	RO	RESERVED	Reserved for future use.	29'h0

7.2.2.18 TIMERSRAWINTSTAT

Bit #	Type	Name	Comments	Default
0	RO	TIMERSRAWINTSTAT	The register contains the unmasked interrupt status of all timers in the component.	0
31:1	RO	RESERVED	Reserved for future use.	31'h0

TIMERSRAWINTSTAT:

- 0 = either timer_intr or timer_intr_n is not active prior to masking



1 = either timer_intr or timer_intr_n is active prior to masking.

7.2.2.19 TIMERSCOMPVERSION

Bit #	Type	Name	Comments	Default
31:0	RO	TIMERSCOMPVERSION	Current revision number of the DW_apb_timers component.	32'h3231322A

7.2.2.20 TIMER_1_PROT_LEVEL

Bit #	Type	Name	Comments	Default
2:0	RW	TIMER_1_PROTLEVELFIELD	This field holds protection value of TIMER_1_PROT_LEVEL register.	3'h2
31:3	RO	RESERVED	Reserved for future use.	31'h0

7.2.2.21 TIMER_2_PROT_LEVEL

Bit #	Type	Name	Comments	Default
2:0	RW	TIMER_2_PROTLEVELFIELD	This field holds protection value of TIMER_2_PROT_LEVEL register.	3'h2
31:3	RO	RESERVED	Reserved for future use.	31'h0

7.2.2.22 TIMER_3_PROT_LEVEL

Bit #	Type	Name	Comments	Default
2:0	RW	TIMER_3_PROTLEVELFIELD	This field holds protection value of TIMER_3_PROT_LEVEL register.	3'h2
31:3	RO	RESERVED	Reserved for future use.	31'h0



7.3 I2C slave registers

7.3.1 List of registers and offset details

Base Address : APB_I2C_SLAVE0_BASE, APB_I2C_SLAVE1_BASE

Register	Offset	Memory Access	Description
CR1	0x000	R/W	Control Register 1
CR2	0x004	R/W	Control Register 2
FBCR1	0x008	R/W	FIFO Byte Count Register 1
FIFO	0x00C	R/W	FIFO Memory
ADR1	0x018	R/W	Address Register 1
ADR2	0x01C	R/W	Address Register 2
ISR	0x020	R/W	Interrupt Status Register
IMR	0x024	R/W	Interrupt Mask Register
IVR	0x028	RO	Interrupt Vector Register
FBCR2	0x02C	R/W	FIFO Byte Count Register 2
RSBCR1	0x030	R/W	Repeated Start Byte Count Register 1
RSBCR2	0x034	R/W	Repeated Start Byte Count Register 2
S-RSBCR1	0x038	R/W	Repeated Start Byte Count Register 1 (Slave)
S-RSBCR2	0x03C	R/W	Repeated Start Byte Count Register 2 (Slave)
RSSFIFO	0x040	R/W	Repeated Start Slave FIFO Memory (Slave)
ISR2	0x044	R/W	Interrupt Status Register 2
IMR2	0x048	R/W	Interrupt Mask Register 2
IVR2	0x04C	RO	Interrupt Vector Register 2
-	0x050 - 0x060	-	Reserved
SFR	0x064	R/W	Programmable SDA/SCL Spike Filter Rejection
HS-SFR	0x080	R/W	Hs-Mode Prog. SDA/SCL Spike Filter Rejection
	0x084 - 0x0D8		Reserved
S-MTR	0x0DC	R/W	MSH Timeout Release (Slave)
SDSR-I	0x090	RW	SDA Input Delay Select Register
SDSR-O	0x094	RW	SDA Output Delay Select Register
CIR1	0x0E0	RO	Core Identification Register 1
CIR2	0x0E4	RO	Core Identification Register 2
	0x0E8 - 0xFFFF	-	Reserved



7.3.2 Register definition

7.3.2.1 CR1 (Control Register 1)

Size: 8 bits

Offset: 0x0

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	IRT	R/W	I2C Reset: 0 – No reset. 1 – I2C Controller synchronous reset. While set to 1, the I2C Controller is held in reset. Thus, the user resets the I2C Controller by writing a 1 followed by writing a 0.
1	TRS	R/W	Transmitter / Receiver Select: 0 – I2C Controller set to Master-Receiver Mode. 1 – I2C Controller set to Master-Transmitter Mode Only valid when MSS = 0 (Master Mode) For MSS = 0 (Master Mode), the Transmit / Receive direction must be set before the transfer is initiated by control bit FTE in Control Register 2.
2	MSS	R/W	Master / Slave Select: 0 – I2C Controller set to Master Mode. 1 – I2C Controller set to Slave Mode MSS works with TRS in MSS Master Mode to set the Transmit or Receive direction
3	IEB	R/W	I2C Enable: 0 – Disables I2C Controller IP Core. The I2C Controller will not initiate a Master transaction nor respond to an external I2C Master. 1 – Enables I2C Controller IP Core. The I2C Controller can initiate a Master transaction as well as respond to an external I2C Master that initiates an I2C bus transaction with a valid slave address. For the I2C Controller programmed as a Slave, the Controller responds with appropriate Acknowledges and completes the transaction in either Slave-Transmitter or Slave-Receiver mode. IEB serves as an overriding enable / disable.
4	SAS		Slave Address Size: 0 – 7-bit Slave Address Size 1 – 10-bit Slave Address Size
[7:5]			Reserved

7.3.2.2 CR2 (Control Register 2)

Size: 8 bits



Offset: 0x004

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FRT	R/W	<p>FIFO Reset (synchronous):</p> <p>0 – No reset.</p> <p>1 – FIFO synchronous reset. While set to 1, the I2C Controller FIFO is held in reset. Thus, the user resets the I2C Controller FIFO by writing a 1 followed by writing a 0.</p> <p>Note that the FIFO address pointers are reset. The actual FIFO memory contents are not cleared. (This is to facilitate FIFO implementation in SRAM, at the user's discretion, which is more area and power efficient than registers, and do not contain a reset input capability.)</p> <p>Note Control Register 1, control bit IRT, resets all FIFO address pointers, as does the FIFO Reset (FRT) control bit.</p> <p>The purpose of the FRT control bit is to reset the FIFO for re-use while holding the I2C Bus, for data block transfers longer than the size of the FIFO. See control bit HBD for more information.</p>
1	FTE	R/W	Reserved
2	HBD	R/W	<p>Hold I2C Bus for more FIFO Data (DB-I2C-S):</p> <p>0 – Do Not Hold I2C bus for more FIFO data</p> <p>1 – Hold I2C bus for more FIFO data.</p> <p>Once transfer complete as indicated by register FBCR=0, after a ACK is sent but no STOP bit, if control bit HBD set, the FSM waits for the next FIFO block to transfer. Interrupt MHB sets informing the CPU to either write more data into the FIFO for the next transfer after Repeated Start, or simply clear MHB. Clearing MHD will force a STOP bit if the FIFO is empty or if the FIFO is not empty, a Repeated Start followed by the data transfer. Valid for I2C Master transactions.</p>
3	RSE	R/W	Reserved

4	RSF	R/W	Repeated Start FIFO (DB-I2C-M & DB-I2C-S): 0 – FIFO used for transfer after I2C Repeated Start 1 – RSS FIFO used for transfer after I2C Repeated Start The Slave-Receiver transaction after the Repeated Start (Sr) will write the incoming I2C bytes into the FIFO if RSF=0, or into RSS
5	BCE	R/W	Bus Clear Enable (DB-I2C-M & DB-I2C-S): 0 – Bus Clear Enable inactive 1 – Bus Clear Enable active DB-I2C-M: When BCE=1, when FTE set to 1 to initiate a I2C Master transfer, 9 zeros are transmitted to force a I2C Slave holding SDA at 0 to self-reset. Interrupt SDA Stuck at 0 (SS0) is asserted. DB-I2C-S: When BCE=1, after I2C Start, if 9 zeros received detected, then an internal Synchronous Reset is issued while interrupt SDA Stuck at 0 (SS0) asserted. See Bus Clear section for full programming information
6	-		Reserved
7	-		Reserved

7.3.2.3 FBCR1 (FIFO Byte Count Register 1)

Size: 8 bits

Offset: 0x008

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7: 0	FBCR[7:0]	R/W	<p>FIFO Byte Count Register 1 (lower 8-bits of register FBCR): Concatenates with FBCR2[3:0] to form FBCR[11:0].</p> <p>Number of byte transfers on I2C Bus . So, if <i>NumWords</i> is the Number of words to transfer, write <i>NumWords</i> to FBCR.</p> <p>Note the following for each transfer direction: Master-Transmitter Mode: FBCR contains the number of bytes written to the FIFO by the host processor and POPped by the control FSM for the I2C Bus transfer.</p> <p>(CPU Writes; I2C Controller FSM decrements) Master-Receiver Mode: FBCR contains the number of bytes the control FSM should read from the I2C Bus slave device and PUSH into the FIFO.</p> <p>(CPU Writes; I2C Controller FSM decrements) Slave-Transmitter Mode: FBCR contains the number of bytes written to the FIFO by the host processor and POPped by the control FSM for the I2C Bus transfer.</p> <p>(I2C Controller FSM increments; CPU Reads) Slave-Receiver Mode: FBCR contains the number of bytes received from the Slave and available for the host processor to read from the FIFO.</p> <p>(I2C Controller FSM increments; CPU Reads) For Master Operations, CPU writes FBCR with transfer byte count and I2C Controller decrements with each transfer. For Slave Operations, I2C Controller increments with each transfer and CPU reads FBCR to determine the number of bytes in FIFO to read.</p>

7.3.2.4 FIFO (FIFO memory)

Size: 8 bits

Offset: 0x00C

Memory Access: R/W



Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	[7:0]	R/W	Host Processor single address interface to FIFO. A write will PUSH a byte onto the FIFO memory while a read will POP a byte. For optional processor interfaces of 16- or 32-bits, please contact Digital Blocks for more information. If CR1.MSP Enabled, then the FIFO serves only as a TX FIFO for Master-Transmitter and Slave-Transmitter operations.

7.3.2.5 ADR1 (Address Register 1)

Size: 8 bits

Offset: 0x018

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
6:0	ADR1 [6:0]	R/W	<p>Slave Address Register 1: I2C Master Mode: The 7-bit Slave Address sent as the first 7-bits after a START condition. The R/W least significant bit sent is derived from TRS.</p> <p>I2C Slave Mode: After a START condition detected on the I2C Bus, if the following 7-bit Address equals ADR1[6:0], the DB-I2C-S responds with an appropriate Acknowledge, and based on the 8th R/W bit, enters Slave-Transmit or Slave-Receive mode for the follow-on data transfers.</p> <p>If the 7-bit Address equals 7'b1111_0XX, then a 10-bit address is detected. Incoming Address bits [1:0] are saved and concatenated with the next 8-bit address to form the 10-bit address from the I2C Master which is then compared to ADR2[1:0]:ADR1[7:0]. If they are equal, the DB-I2C-S responds with an appropriate Acknowledges and enters Slave-Transmit or Slave-Receive mode</p>
7	ADR1 [7]		<p>Address Register 1, Bit 7: Used for 10-bit Addressing. See ADR1[6:0] definition above and usage of ADR1[7]</p>

7.3.2.6 ADR2 (Address Register 1)

Size: 8 bits

Offset: 0x01C

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
1:0	ADR2 [1:0]	R/W	<p>Address Register 2, Bits 1:0:</p> <p>The most significant two-bits for comparison to an incoming 10-bit Slave Address from the I2C Master. Internal registers ADR2 [1:0] : ADR1 [7:0], concatenated, form the 10-bit address comparison for the DB-I2C-S to the incoming 10-bit Slave Address.</p>
7:2			Reserved

7.3.2.7 ISR (Interrupt Status Register)

Size: 9 bits

Offset: 0x020

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FUR	R/W	FIFO - Underrun: 0 – No Error. 1 – FIFO Underrun Error generates interrupt. Writing a 1 to this bit clears it.
1	FOR	R/W	FIFO - Overrun: 0 – No Error. 1 – FIFO Overrun Error generates interrupt. Writing a 1 to this bit clears it.
2	FER	R/W	FIFO Error – Underrun or Overrun: 0 – No Error. 1 – Any of FUR or FOR error bits set to active 1 generates FER interrupt. (Acts as a composite FIFO error interrupt.) Writing a 1 to this bit clears it.
3	RNK	R/W	Receive NACK (DB-I2C-M and DB-I2C-S): 0 – No Error. 1 – Receive NACK generates interrupt. For Master-Transmitter, NACK received when ACK expected after Address or Data. For Master-Receiver, NACK received when ACK expected after Address. For Slave-Transmitter, NACK received when ACK expected after Data. (At end of transfer, a NACK will be received from the external Master-Receiver signaling last byte in transfer. This is not an error. Contact Digital Blocks if more information is needed.) Writing a 1 to this bit clears it.
4	ALD	R/W	Reserved
5	FFE	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode): 0 – FIFO not Almost Full or Empty 1 – FIFO has reached parameterized Almost Full or Empty Value Default parameter setting is as follows: // FIFO Almost Full/Empty Threshold parameter FFE_THRESHOLD = 2; Writing a 1 to this bit clears it.

6	TCS	R/W	<p>Transfer Completed - I2C STOP Asserted (DB-I2C-M and DB-I2CS):</p> <p>0 – Current I2C Bus transfer (for Master Mode, invoked by control bit FTE in Control Register 2) not completed.</p> <p>1 – Current I2C Bus transfer completed.</p> <p>For Master Mode, TCS sets when FSM completes sending/receiving all FBCR number of bytes.</p> <p>For Slave-Receiver Mode, TCS sets when at least 1 byte is loaded into the FIFO and an I2C STOP is detected.</p> <p>For Slave-Transmitter Mode, TCS sets when an I2C STOP is detected.</p> <p>In all four I2C Modes, FBCR can be read for number of bytes transmitted / received.</p> <p>Writing a 1 to this bit clears it.</p>
7	HNK	R/W	<p>Hs-mode Receive NACK :</p> <p>0 – No Error.</p> <p>1 – Receive NACK in Hs-mode after Hs Master Code sent.</p> <p>For Master-Transmitter or Master-Receiver, in Hs-mode (HSCR.HME=1), after Hs Master Code sent, a NACK successfully received.</p> <p>HNK asserted will suppress interrupt RNK.</p> <p>Writing a 1 to this bit clears it</p>
8	Reserved	R/W	Reserved



7.3.2.8 IMR (Interrupt Mask Register)

Size: 9 bits

Offset: 0x024

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	FURM	R/W	FIFO – Underrun – Mask Enable/Disable: 0 – Disable FUR interrupt. 1 – Enable FUR interrupt.
1	FORM	R/W	FIFO – Overrun – Mask Enable/Disable: 0 – Disable FOR interrupt. 1 – Enable FOR interrupt.
2	FERM	R/W	FIFO Error – Underrun or Overrun – Mask Enable/Disable: 0 – Disable FER interrupt. 1 – Enable FER interrupt.
3	RNKM	R/W	Receive NACK – Mask Enable/Disable: 0 – Disable RNK interrupt. 1 – Enable RNK interrupt.
4	ALDM	R/W	Reserved
5	FFEM	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode) – Mask Enable/Disable: 0 – Disable FFE interrupt. 1 – Enable FFE interrupt.
6	TCSM	R/W	Transfer Completed - I2C STOP Asserted – Mask Enable/Disable: 0 – Disable TCS interrupt. 1 – Enable TCS interrupt.
7	RAKM	R/W	Receive ACK (DB-I2C-S) – Mask Enable/Disable: 0 – Disable RAK interrupt. 1 – Enable RAK interrupt.
8	Reserved		



7.3.2.9 IVR (Interrupt Vector Register)

Size: 9 bits

Offset: 0x028

Memory Access: RO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	FURV	R/W	FIFO – Underrun – Enabled Interrupt: Logical AND of FUR and FURM.
1	FORV	R/W	FIFO – Overrun – Enabled Interrupt: Logical AND of FOR and FORM.
2	FERV	R/W	FIFO Error – Underrun or Overrun – Enabled Interrupt: Logical AND of FER and FERM.
3	RNKV	R/W	Receive NACK – Enabled Interrupt: Logical AND of RNK and RNKM.
4	ALDV	R/W	Reserved
5	FFEV	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode) – Enabled Interrupt: Logical AND of FFE and FFEM.
6	TCSV	R/W	Transfer Completed - I2C STOP Asserted – Enabled Interrupt: Logical AND of TCS and TCSM.
7	RAKV	R/W	Receive ACK (DB-I2C-S) – Enabled Interrupt: Logical AND of RAK and RAKM
8	Reserved		

7.3.2.10 FBCR2 (FIFO Byte Count Register 2)

Size: 8 bits

Offset: 0x02C

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
3: 0	FBCR2[3:0]	R/W	FIFO Byte Count Register 2 (upper 4-bits of register FBCR): Concatenates with FBCR1[7:0] to form FBCR[11:0].

7.3.2.11 RSBCR1 (Repeated Start FIFO Byte Count Register 1)

Size: 8 bits

Offset: 0x030

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7: 0	RSBCR1 [7:0]	R/W	Repeated Start Byte Count Register 1 (lower 8-bits of register RSBCR): DB-I2C-S (Slave) For Slave-Transmitter or Slave-Receiver, RSBCR indicates number of bytes received on the I2C Bus AFTER a I2C Repeated Start and placed in the FIFO. RSBCR1 is for the FIFO in DB-I2C-M and DB-I2C-S

7.3.2.12 RSBCR2 (Repeated Start FIFO Byte Count Register 2)

Size: 8 bits

Offset: 0x034

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
3: 0	RSBCR2 [3:0]	R/W	Repeated Start Byte Count Register 2 (upper 4-bits of register RSBCR): Concatenates with RSBCR1[7:0] to form RSBCR[11:0]. RSBCR2 is for the FIFO in DB-I2C-M and DB-I2C-S
7:4			Reserved

7.3.2.13 S-RSBCR1 (RSS FIFO-Repeated Start FIFO Byte Count Register 1)

Size: 8 bits

Offset: 0x038

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7: 0	S-RSBCR1 [7:0]	R/W	<p>Repeated Start Byte Count Register 1 (lower 8-bits of register S-RSBCR):</p> <p>DB-I2C-S (Slave) For Slave-Transmitter or Slave-Receiver, S-RSBCR indicates number of bytes received on the I2C Bus AFTER a I2C Repeated Start and placed in the RSSFIFO.</p> <p>S-RSBCR1 is for the RSS FIFO in DB-I2C-S</p>

7.3.2.14 S-RSBCR2 (RSS FIFO-Repeated Start FIFO Byte Count Register 2)

Size: 8 bits

Offset: 0x03C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
3: 0	S-RSBCR2 [3:0]	R/W	<p>Repeated Start Byte Count Register 2 (upper 4-bits of register S-RSBCR):</p> <p>Concatenates with S-RSBCR1[7:0] to form S-RSBCR[11:0].</p> <p>S-RSBCR2 is for the RSSFIFO DB-I2C-S</p>
7:4			Reserved

7.3.2.15 RSSFIFO (Repeated Start Slave FIFO memory)

Size: 8 bits

Offset: 0x040

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7: 0	RSS [7:0]	R/W	Host Processor single address interface to Repeated Start FIFO. A write will PUSH a byte onto the FIFO memory while a read will POP a byte. CR1.RSF must be enabled for usage to direct the incoming I2C byte payload after the Repeated Start to be written into the RSS FIFO. If CR1.MSP Enabled, then the RSS FIFO serves as a RX FIFO for Master-Receiver and Slave-Receiver operations. (There does not need to be a Repeated Start in the I2C transfer.) For optional processor interfaces of 16- or 32-bits, please contact Digital Blocks for more information.

7.3.2.16 ISR2 (Interrupt Status Register2)

Size: 9 bits

Offset: 0x044

Memory Access: R/W

Value After Reset: 0x00



Bi ts	Na me	Mem ory Acces s	Description
0	RF UR	R/W	RSS FIFO - Underrun: (DB-I2C-MS & DB-I2C-S only) 0 – No Error. 1 – RSS FIFO Underrun Error generates interrupt. Writing a 1 to this bit clears it
1	RF OR	R/W	RSS FIFO - Overrun: (DB-I2C-MS & DB-I2C-S only) 0 – No Error. 1 – RSS FIFO Overrun Error generates interrupt. Writing a 1 to this bit clears it.
2	RFE R	R/W	RSS FIFO Error – Underrun or Overrun: (DB-I2C-MS & DB-I2C-S only) 0 – No Error. 1 – Any of FUR or FOR error bits set to active 1 generates FER interrupt. (Acts as a composite FIFO error interrupt.) Writing a 1 to this bit clears it.
3	RFF E	R/W	RSS FIFO Almost Full (receive mode) or Empty (transmit mode): (DB-I2C-MS & DB-I2C-S only) 0 – RSS FIFO not Almost Full or Empty 1 – RSS FIFO has reached parameterized Almost Full or Empty Value Default parameter setting is as follows: // RSS FIFO Almost Full/Empty Threshold parameter RS_FFE_THRESHOLD = 2; Writing a 1 to this bit clears it.
4	MS H	R/W	Master Slave Last Bit Hold (DB-I2C-M UNUSED) (DB-I2C-S) : 0 – Slave Not Completed Sending Tx Data & Not Holding I2C Bus 1 – Slave Completed Sending Tx Data & Holds I2C while CPU loads FIFO with more data. Slave-Transmitter holds I2C Bus by pulling SCL LOW, after the ACK of the last bit in the last byte transmitted when FIFO is empty. Interrupt MSH will set (to signal processor to re-load FIFO). Firmware has to reload the FIFO and then clear MSH interrupt in that order, following which Slave-Transmitter releases SCL, allowing transaction to continue to FIFO refilled data. Contact Digital Blocks for availability in DB-I2C-M.

5	RS D	R/W	Slave Repeated Start Detected: (DB-I2C-MS & DB-I2C-S only) 0 – Repeated Start (Sr) Not Detected 1 – Repeated Start (Sr) Detected after initial Slave ID validated Valid in DB-I2C-S (Slave-only). Writing a 1 to this bit clears it.
6	ST D	R/W	Slave Start Detected: (DB-I2C-MS & DB-I2C-S only) 0 – Start (S) Not Detected 1 – Start (S) Detected Valid in DB-I2C-S (Slave-only). Writing a 1 to this bit clears it.
7	SPD	R/W	Slave I2C STOP Detected (DB-I2C-MS & DB-I2C-S only): 0 – Stop (P) Not Detected 1 – Stop (P) Detected In I2C Slave, Stop (P) detected. SPD differs from ISR.TCS in that TCS sets when at least 1 byte is loaded into the FIFO; SPD sets when a physical Stop (P) is detected on the I2C Bus.
8	RS A	R/W	Receive Slave Address Match: 0 – Receive Slave Address that Matches NOT Received 1 – Receive Slave Address Matched
9	SS0	R/W	SDA Stuck at 0: (DB-I2C-S & DB-I2C-M only): 0 – SDA stuck at 0 (zero) not detected 1 – SDA stuck at 0 (zero) detected

7.3.2.17 IMR2 (Interrupt Mask Register2)

Size: 9 bits

Offset: 0x048

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	RFURM	R/W	RSS FIFO – Underrun – Mask Enable/Disable: (DB-I2C-MS & DB-I2C-S only) 0 – Disable FUR interrupt. 1 – Enable FUR interrupt.
1	RFORM	R/W	RSS FIFO – Overrun – Mask Enable/Disable: (DB-I2C-MS & DB-I2C-S only) 0 – Disable FOR interrupt. 1 – Enable FOR interrupt.
2	RFERM	R/W	RSS FIFO Error – Underrun or Overrun – Mask Enable/Disable: (DB-I2C-MS & DB-I2C-S only) 0 – Disable FER interrupt. 1 – Enable FER interrupt.
3	RFFEM	R/W	RSS FIFO Almost Full (receive mode) or Empty (transmit mode) – Mask Enable/Disable: (DB-I2C- MS & DB-I2C-S only) 0 – Disable FFE interrupt. 1 – Enable FFE interrupt.
4	MSHM	R/W	Master Slave Last Bit Hold Enable/Disable: 0 – Disable MSH interrupt. 1 – Enable MSH interrupt.
5	RSDM	R/W	Slave Repeated Start Detected - Mask Enable/Disable: (DB-I2C-MS & DB-I2C-S only) 0 – Disable RSD interrupt. 1 – Enable RSD interrupt.
6	STDM	R/W	Slave Start Detected - Mask Enable/Disable: (DB- I2C-MS & DB-I2C-S only) 0 – Disable STD interrupt. 1 – Enable STD interrupt.
7	SPDM	R/W	Slave I2C STOP Detected - Mask Enable/Disable (DB-I2C-MS & DB-I2C-S only): 0 – Disable SPD interrupt. 1 – Enable SPD interrupt.
8	RSAM	R/W	Receive Slave Address Match - Mask Enable/Disable: 0 – Disable RSA interrupt. 1 – Enable RSA interrupt.

9	SS0M	R/W	SDA Stuck at 0 - Mask Enable/Disable (DB-I2C-M only): 0 – Disable SS0 interrupt. 1 – Enable SS0 interrupt.
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7.3.2.18 IVR2 (Interrupt Vector Register2)

Size: 9 bits

Offset: 0x04C

Memory Access: RO

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	RFURV	R/W	RSS FIFO – Underrun – Enabled Interrupt: (DB-I2C-MS & DB-I2C-S) Logical AND of RFUR and RFURM.
1	RFORV	R/W	RSS FIFO – Overrun – Enabled Interrupt: (DB-I2C-MS & DB-I2C-S) Logical AND of RFOR and RFORM.
2	RFERV	R/W	RSS FIFO Error – Underrun or Overrun – Enabled Interrupt: (DB-I2C-MS & DB-I2C-S) Logical AND of RFER and RFERM.
3	RFFEV	R/W	RSS FIFO Almost Full (receive mode) or Empty (transmit mode) – Enabled Interrupt: (DB-I2C-MS & DB-I2C-S) Logical AND of RFFE and RFFEM.
4	MSHV	R/W	Master Slave Last Bit Hold – Enabled Interrupt: Logical AND of MSH and MSHM.
5	RSDV	R/W	Slave Repeated Start Detected - Enabled Interrupt: (DB-I2C-MS & DB-I2C-S only) Logical AND of RSD and RSDM.
6	STDV	R/W	Slave Start Detected - Enabled Interrupt: (DB-I2C-MS & DB-I2C-S only) Logical AND of STD and STDM.
7	SPDV	R/W	Slave I2C STOP Detected - Enabled Interrupt: (DB-I2C-MS & DB-I2C-S only) Logical AND of SPD and SPDM.
8	RSAV	R/W	Receive Slave Address Match - Enabled Interrupt: (DB-I2C-MS & DB I2C-S only) Logical AND of RSA and RSAM.
9	SS0V	R/W	SDA Stuck at 0 - Enabled Interrupt (DB-I2C-M only): Logical AND of SS0 and SS0M.

7.3.2.19 SFR (Spike Filter Rejection)

Size: 32 bits

Offset: 0x064

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	SFW	R/W	<p>Programmable SDA/SCL Spike Filter Width (DB-I2C-M & DB-I2C-S): 8-bit value that sets the width of the LOW spikes on SDAH/SCLH rejected. Each value indicates number of DB-I2C clock counts. Load with N – 1 value, with N the number of CLK cycles of the spike width rejection</p> <p>As an example, if the input bus fabric clock (e.g. PCLK / HCLK / ACLK/CLK) is 100 MHz, then set SFW = 5-1 = 4 in order to get the minimum 50 ns SDAH/SCLH LOW spike rejection.</p>
15:8			Reserved
31:16	SHW	R/W	<p>Programmable SCL HIGH Width (DB-I2C-S only): 16-bit value that indicates the width of the DB-I2C-S (Slave) incoming SCL HIGH pulse. While field SFW sets the LOW spike width rejection based on the DB-I2C clock, SHW indicates the SCL HIGH pulse length so that the rejection filter turns off when SCL really transitions to LOW. Each value indicates number of DB-I2C clock counts.</p> <p>If input SCL HIGH period is N DB-I2C clocks, then program SHW to N-2</p>

7.3.2.20 HS-SFR (Hs-Mode SDA/SCL Spike Filter Rejection)

Size: 8 bits

Offset: 0x80

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
7:0	HSFW[7:0]	R/W	<p>Programmable HS-Mode SDA/SCL Spike Filter Width (DB-I2C-S & DB-I2C-M): 8-bit value that sets the width of the LOW spikes on SDAH/SCLH rejected. Each value indicates number of DB-I2C clock counts. Load with N – 1 value, with N the number of CLK (bus clock APB / HCLK / ACLK) cycles of the spike width rejection As an example, if the input bus fabric clock (e.g. PCLK / HCLK / ACLK / Avalon CLK) is 100 MHz, then set HSFW = 5-1 = 4 in order to get the minimum 50 ns SDAH/SCLH LOW spike rejection.</p> <p>HSFW used during Hs-mode SCL/SDA cycles on the I2C bus, while SFR.SFW is used during Standard/Fast/Fast-mode Plus I2C SCL/SDA cycles.</p> <p>For DB-I2C-M, register HS-SCD2, field HSHP is set to the SCLH HIGH period, which informs the SCL rejection filter the pulse width of SCL the filter should reject spikes.</p> <p>For DB-I2C-S, register HS-SCD2, field HSHP can be used for the same purpose of setting the SCL width the filter should reject spikes. But, the width of the incoming SCL signal needs to be known.</p>

7.3.2.21 TX-FBCAR (TX FIFO Byte Count Actual register)

Bits	Name	Memory Access	Description
7:0	TX-FBCAR[7:0]	R/W	<p>TX-FIFO Byte Count Actual: Number of bytes in TX-FIFO.</p> <p>TX-FBCAR increments with each byte written by CPU to the TX FIFO and decrements with each byte read by I2C Control unit.</p> <p><i>TX-FBCAR shown at 8-bits for 256 byte FIFO implementation</i></p>



7.3.2.22 RX-FBCAR (RX FIFO Byte Count Actual register)

Bits	Name	Memory Access	Description
7:0	RX-FBCAR[7:0]	R/W	<p>RX-FIFO Byte Count Actual: Number of bytes in RX-FIFO. RX-FBCAR increments with each byte written by I2C Control unit to the RX-FIFO and decrements with each byte read by CPU.</p> <p><i>RX-FBCAR shown at 8-bits for 256 byte FIFO implementation</i></p>

7.3.2.23 TX-FAFETR (TX-FIFO Almost full or empty threshold register)

Size: 8 bits

Offset: 0x8C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	TX-FAFETR[7:0]	R/W	<p>TX FIFO Almost Full or Empty Threshold Register: Programmed threshold value, when TX-FAFETR equal to TX FIFO internal byte count, triggers interrupt FFE in ISR register. Thus, FFE triggered when TX-FAFETR = TX FIFO Byte Count Preset to 0xFF but on startup should be cleared as part of initialization</p>

7.3.2.24 Programmable Hs-Mode MSH Timeout Release (S-MTR)

Size: 8 bits

Offset: 0xDC

Memory Access: R/W

Value After Reset: 0x0A



Bits	Name	Memory Access	Description
7:0	MTR	R/W	<p>MSH Timeout Release</p> <p>8-bit value sets timeout from time of Interrupt MSH clear, as starting point, with first data bit on SDA, to rising edge of SCL.</p> <p>Valid range 1 – 255. Power up default is 6.</p> <p>Essential I2C timing parameter tSU; DAT Example calculation:</p> <p>For I2C Standard Mode (100 Kbps) with CLK = 22 MHz, set MTR = 6. This yields $45.45 \text{ ns} \times 6 = 272 \text{ ns}$, which exceeds tSU; DAT minimum value of 250 ns.</p>



7.3.2.25 SDSR-I (Programmable SDA Input Delay Select Register)

Size: 8 bits

Offset: 0x90

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
5:0	SDSR-I	R/W	Programmable SDA Input Delay Select Register SDA Input hold time can be extended to 0 to 63 AMBA Clocks Note that register SDSR-I is for SDA Input variable hold delay while SDSR-O is for SDA Output variable hold delay
7:6	Reserved		

7.3.2.26 SDSR-O (Programmable SDA Output Delay Select Register)

Size: 8 bits

Offset: 0x94

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
5:0	SDSR-O	R/W	Programmable SDA Output Delay Select Register SDA Output hold time can be extended to 0 to 63 AMBA Clocks Note that register SDSR-I is for SDA Input variable hold delay while SDSR-O is for SDA Output variable hold delay

7.3.2.27 CIR1 (Core Identification Register 1)

Size: 8 bits

Offset: 0xE0

Memory Access: RO



Value After Reset: 0x01

Bits	Name	Memory Access	Description
7:0	CIR_MN	RO	<p>Core Identification Register – Model Number:</p> <p>0x1 – Model Number DB-I2C-MS-APB Master/Slave, with APB interface, and FIFOs</p> <p>0x2 – Model Number DB-I2C-MS-AHB Master/Slave, with AHB interface, and FIFOs</p> <p>0x3 – Model Number DB-I2C-MS-AVLN Master/Slave, with Avalon interface, and FIFOs</p> <p>0x4 – Model Number DB-I2C-M-APB Master-only, with APB interface, and FIFOs</p> <p>0x5 – Model Number DB-I2C-M-AHB Master-only, with AHB interface, and FIFOs</p> <p>0x6 – Model Number DB-I2C-M-AVLN Master-only, with Avalon interface, and FIFOs</p> <p>0x7 – Model Number DB-I2C-S-APB Slave-only, with APB interface, and FIFOs</p> <p>0x8 – Model Number DB-I2C-S-AHB Slave-only, with AHB interface, and FIFOs</p> <p>0x9 – Model Number DB-I2C-S-AVLN Slave-only, with Avalon interface, and FIFOs</p> <p>0xA – Model Number DB-I2C-S-RA-AVLN Slave-only, with Register Array</p>

7.3.2.28 CIR2 (Core Identification Register 2)

Size: 8 bits

Offset: 0xE4

Memory Access: RO

Value After Reset: 0x28

Bits	Name	Memory Access	Description
4:0	CIR_REV	RO	Core Identification Register – Revision: 0x00 – Version 1.0.0 0x01 – Version 1.0.1 0x02 – Version 1.0.2 0x03 – Version 1.0.3 0x04 – Version 1.0.4 0x05 – Version 1.0.5 0x06 – Version 1.0.6 0x07 – Version 1.0.7 0x08 – Version 1.0.8
7:5	CIR_BW	RO	Core Identification Register – Bit Width (Processor Slave Bus): 0x2 – 32 Bits 0x1 – 16 Bits 0x0 – 8 Bits

7.4 I2C master registers

7.4.1 List of registers and offset details

Base Address : APB_I2C_MASTER0_BASE, APB_I2C_MASTER1_BASE

Register	Offset	Memory Access	Description
CR1	0x000	R/W	Control Register 1
CR2	0x004	R/W	Control Register 2
FBCR1	0x008	R/W	FIFO Byte Count Register 1
FIFO	0x00C	R/W	FIFO Memory
SCD1	0x010	R/W	SCL Clock Divider Register 1
SCD2	0x014	R/W	SCL Clock Divider Register 2
ADR1	0x018	R/W	Address Register 1
ADR2	0x01C	R/W	Address Register 2
ISR	0x020	R/W	Interrupt Status Register
IMR	0x024	R/W	Interrupt Mask Register
IVR	0x028	RO	Interrupt Vector Register
FBCR2	0x02C	R/W	FIFO Byte Count Register 2
ISR-2	0x44	R/W	Interrupt Status Register 2
IMR-2	0x48	R/W	Interrupt Mask Register 2
IVR-2	0x4C	R/W	Interrupt Vector Register 2
-	0x050 0x060	-	Reserved
SFR	0x064	R/W	Programmable SDA/SCL Spike Filter Rejection
HS-CR	0x074	R/W	Hs-Mode Control Register
HS-SCD1	0x078	R/W	Hs-Mode SCL Clock Divider Register 1
HS-SCD2	0x07C	R/W	Hs-Mode SCL Clock Divider Register 2
HS-SFR	0x080	R/W	Hs-Mode Prog. SDA/SCL Spike Filter Rejection
TX-FBCAR	0x084	RO	TX FIFO byte count actual register
RX-FBCAR	0x088	RO	RX FIFO byte count actual register
TX-FAFETR	0x08C	RW	TX FIFO Almost full/empty register
SDSR-I	0x090	RW	SDA Input Delay Select Register
SDSR-O	0x094	RW	SDA Output Delay Select Register
	0x098- 0x0D8		Reserved
CIR1	0x0E0	RO	Core Identification Register 1
CIR2	0x0E4	RO	Core Identification Register 2
	0x0E8 0xFFFF	-	Reserved



7.4.2 Register definition

7.4.2.1 CR1 (Control Register 1)

Size: 8 bits

Offset: 0x0

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	IRT	R/W	I2C Reset: 0 – No reset. 1 – I2C Controller synchronous reset. While set to 1, the I2C Controller is held in reset. Thus, the user resets the I2C Controller by writing a 1 followed by writing a 0.
1	TRS	R/W	Transmitter / Receiver Select: 0 – I2C Controller set to Master-Receiver Mode. 1 – I2C Controller set to Master-Transmitter Mode Only valid when MSS = 0 (Master Mode) For MSS = 0 (Master Mode), the Transmit / Receive direction must be set before the transfer is initiated by control bit FTE in Control Register 2.
2	MSS	R/W	Master / Slave Select: 0 – I2C Controller set to Master Mode. 1 – I2C Controller set to Slave Mode MSS works with TRS in MSS Master Mode to set the Transmit or Receive direction
3	IEB	R/W	I2C Enable: 0 – Disables I2C Controller IP Core. The I2C Controller will not initiate a Master transaction nor respond to an external I2C Master. 1 – Enables I2C Controller IP Core. The I2C Controller can initiate a Master transaction as well as respond to an external I2C Master that initiates an I2C bus transaction with a valid slave address. For the I2C Controller programmed as a Slave, the Controller responds with appropriate Acknowledges and completes the transaction in either Slave-Transmitter or Slave-Receiver mode. IEB serves as an overriding enable / disable.
4	SAS		Slave Address Size: 0 – 7-bit Slave Address Size 1 – 10-bit Slave Address Size
[7:5]	-		Reserved

7.4.2.2 CR2 (Control Register 2)

Size: 8 bits



Offset: 0x004

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FRT	R/W	<p>FIFO Reset (synchronous):</p> <p>0 – No reset.</p> <p>1 – FIFO synchronous reset. While set to 1, the I2C Controller FIFO is held in reset. Thus, the user resets the I2C Controller FIFO by writing a 1 followed by writing a 0.</p> <p>Note that the FIFO address pointers are reset. The actual FIFO memory contents are not cleared. (This is to facilitate FIFO implementation in SRAM, at the user's discretion, which is more area and power efficient than registers, and do not contain a reset input capability.)</p> <p>Note Control Register 1, control bit IRT, resets all FIFO address pointers, as does the FIFO Reset (FRT) control bit.</p> <p>The purpose of the FRT control bit is to reset the FIFO for re-use while holding the I2C Bus, for data block transfers longer than the size of the FIFO. See control bit HBD for more information.</p>
1	FTE	R/W	<p>FIFO Mode - Transfer Enable (DB-I2C-MS & DB-I2C-M):</p> <p>0 – Transfer on I2C Bus inactive.</p> <p>1 – Transfer on I2C Bus active. Setting FTE initiates the I2C Controller Finite State Machine (FSM) to conduct a I2C Master transfer.</p> <p>Note the Master / Slave Select (MSS) and Transmit / Receive (TRS) control bits in Control Register 1 must first be programmed before the transfer is initiated by FTE.</p> <p>FTE remains set during the transfer, and is reset by the Master control FSM upon the completion of the transfer.</p>



2	HBD	R/W	<p>Hold I2C Bus for more FIFO Data (DB-I2C-S):</p> <p>0 – Do Not Hold I2C bus for more FIFO data</p> <p>1 – Hold I2C bus for more FIFO data.</p> <p>Once transfer complete as indicated by register FBCR=0, after a ACK is sent but no STOP bit, if control bit HBD set, the FSM waits for the next FIFO block to transfer. Interrupt MHB sets informing the CPU to either write more data into the FIFO for the next transfer after Repeated Start, or simply clear MHB. Clearing MHD will force a STOP bit if the FIFO is empty or if the FIFO is not empty, a Repeated Start followed by the data transfer. Valid for I2C Master transactions.</p>
3	RSE	R/W	<p>Repeated Start Enable (DB-I2C-MS & DB-I2C-M):</p> <p>0 – No repeated Start I2C Bus transaction.</p> <p>1 – Repeated Start I2C Bus transaction</p> <p>Note that RSE must be set at the time FTE is set enabling an I2C Bus transfer. After Slave Address from register ADR1 is transmitted, and an ACK is received, bytes from the FIFO are transmitted according to the RSBCR. RSBCR decrements with each byte transmitted from the FIFO, and one RSBCR reaches zero, in place of a STOP, a Repeated START is asserted on the C Bus. At that point RSE is reset by the control FSM, and I2C transaction programmed by FTE and TRS occurs. TRS determines whether the transaction after the Repeated START is a Master-Transmitter or Master-Receiver. Note that the I2C transaction completes as any other, except that the Repeated Start replaces the START. If a Master-Transmitter, the DB-I2C-M will continue to send bytes from the FIFO according to FBCR.</p> <p>RSE remains set during the transfer, and is reset by the control FSM upon the completion of the transfer prior to the Repeated START on the I2C Bus.</p>



4	RSF	R/W	<p>Repeated Start FIFO (DB-I2C-M & DB-I2C-S): 0 – FIFO used for transfer after I2C Repeated Start 1 – RSS FIFO used for transfer after I2C Repeated Start The Slave-Receiver transaction after the Repeated Start (Sr) will write the incoming I2C bytes into the FIFO if RSF=0, or into RSS</p>
5	BCE	R/W	<p>Bus Clear Enable (DB-I2C-M & DB-I2C-S): 0 – Bus Clear Enable inactive 1 – Bus Clear Enable active DB-I2C-M: When BCE=1, when FTE set to 1 to initiate a I2C Master transfer, 9 zeros are transmitted to force a I2C Slave holding SDA at 0 to self-reset. Interrupt SDA Stuck at 0 (SS0) is asserted.</p> <p>DB-I2C-S: When BCE=1, after I2C Start, if 9 zeros received detected, then an internal Synchronous Reset is issued while interrupt SDA Stuck at 0 (SS0) asserted.</p> <p>See Bus Clear section for full programming information</p>
6	BCSE		<p>Bus Clear SDA Enable (DB-I2C-M): 0 – SDA left in tri-state when Bus Clear Enable active 1 – SDA forced to 0 when Bus Clear Enable active</p> <p>When DB-I2C-M issues a Bus Clear, when BCE=1, BCSE can be used to leave SDA in tristate by DB-I2C-M or to force a 0. Note when left in tristate (BCSE=0), presumably the SDA stuck at 0 provides the 0s during the 9 SCL clocks. When SDA forced to 0, the full programming information in the Bus Clear section must be followed</p>



7	RSCO		Repeated Start (Sr) Continuous Operation (DB-I2C-M): 0 – Continuous Sr Operation Disabled 1 – Continuous Sr Operation Enabled See section “Repeated Start (Sr) – Continuous Back-to-Back Transfers” for description.
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7.4.2.3 FBCR1 (FIFO Byte Count Register 1)

Size: 8 bits

Offset: 0x008

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7: 0	FBCR[7:0]	R/W	<p>FIFO Byte Count Register 1 (lower 8-bits of register FBCR): Concatenates with FBCR2[3:0] to form FBCR[11:0].</p> <p>Number of byte transfers on I2C Bus . So, if <i>NumWords</i> is the Number of words to transfer, write <i>NumWords</i> to FBCR.</p> <p>Note the following for each transfer direction: Master-Transmitter Mode: FBCR contains the number of bytes written to the FIFO by the host processor and POPped by the control FSM for the I2C Bus transfer.</p> <p>(CPU Writes; I2C Controller FSM decrements) Master-Receiver Mode: FBCR contains the number of bytes the control FSM should read from the I2C Bus slave device and PUSH into the FIFO.</p> <p>(CPU Writes; I2C Controller FSM decrements) Slave-Transmitter Mode: FBCR contains the number of bytes written to the FIFO by the host processor and POPped by the control FSM for the I2C Bus transfer.</p> <p>(I2C Controller FSM increments; CPU Reads) Slave-Receiver Mode: FBCR contains the number of bytes received from the Slave and available for the host processor to read from the FIFO.</p> <p>(I2C Controller FSM increments; CPU Reads) For Master Operations, CPU writes FBCR with transfer byte count and I2C Controller decrements with each transfer. For Slave Operations, I2C Controller increments with each transfer and CPU reads FBCR to determine the number of bytes in FIFO to read.</p>





7.4.2.4 FIFO (FIFO memory)

Size: 8 bits

Offset: 0x00C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	[7:0]	R/W	Host Processor single address interface to FIFO. A write will PUSH a byte onto the FIFO memory while a read will POP a byte. For optional processor interfaces of 16- or 32-bits, please contact Digital Blocks for more information. If CR1.MSP Enabled, then the FIFO serves only as a TX FIFO for Master-Transmitter and Slave-Transmitter operations.

7.4.2.5 SCD1 (SCL Clock Divider Register 1)

Size: 8 bits

Offset: 0x010

Memory Access: R/W

Value After Reset: 0x01

Bits	Name	Memory Access	Description
7:0	SCD1[7:0]	R/W	SCL Clock Divider Register 1 The frequency of I2C Bus SCL divided down from the primary clock input from the Host Processor

7.4.2.6 SCD2 (SCL Clock Divider Register 2)

Size: 8 bits

Offset: 0x014

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
2:0	SCD2[2:0]	R/W	SCL Clock Divider Register 2 The frequency of I2C Bus SCL divided down from the primary clock input from the Host Processor
6:3			Reserved
7	SHT	R/W	Fast/Standard/Fast Plus Start/Stop Setup/Hold & Tlow Time Control: 0 – F/S Speeds Setup/Hold Time is $\frac{1}{4}$ SCL Period & Tlow spec for Fast (400KHz) 1 – F/S Speeds Setup/Hold Time is $\frac{1}{2}$ SCL Period and Tlow spec for Standard (100KHz) and Fast Plus (1MHz) Set SHT=0 for Fast Speed (400 KHz) – 1/4 SCK Clock Period Setup/Hold Time and SCL Tlow min requirement of 1.3us for Fast Mode Set SHT=1 for Standard Speed (100 KHz) & Fast Mode Plus – 1/2 SCK Clock Period Setup/Hold Time and SCL Tlow min requirements for Standard and Fast Plus

Note : SCD 1,2 are concatenated into one 11-bit word (with SCD2[2:0] the most significant three bits). Program SCD2:SCD1 to value N-1 (one less than the desired value).

7.4.2.7 ADR1 (Address Register 1)

Size: 8 bits

Offset: 0x018

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
6:0	ADR1 [6:0]	R/W	<p>Slave Address Register 1: I2C Master Mode: The 7-bit Slave Address sent as the first 7-bits after a START condition. The R/W least significant bit sent is derived from TRS.</p> <p>I2C Slave Mode: After a START condition detected on the I2C Bus, if the following 7-bit Address equals ADR1[6:0], the DB-I2C-S responds with an appropriate Acknowledge, and based on the 8th R/W bit, enters Slave-Transmit or Slave-Receive mode for the follow-on data transfers.</p> <p>If the 7-bit Address equals 7'b1111_0XX, then a 10-bit address is detected. Incoming Address bits [1:0] are saved and concatenated with the next 8-bit address to form the 10-bit address from the I2C Master which is then compared to ADR2[1:0]: ADR1[7:0]. If they are equal, the DB-I2C-S responds with an appropriate Acknowledges and enters Slave-Transmit or Slave-Receive mode</p>
7	ADR1 [7]		Reserved

7.4.2.8 ADR2 (Address Register 2)

Size: 8 bits

Offset: 0x01C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
1:0	ADR2 [1:0]	R/W	<p>Address Register 2, Bits 1:0: I2C Master Mode: The most significant two-bits for an outgoing 10-bit Slave Address from the DB-I2C-M</p>
7:2			Reserved

7.4.2.9 ISR (Interrupt Status Register)

Size: 8 bits

Offset: 0x020



Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FUR	R/W	FIFO - Underrun: 0 – No Error. 1 – FIFO Underrun Error generates interrupt. Writing a 1 to this bit clears it.
1	FOR	R/W	FIFO - Overrun: 0 – No Error. 1 – FIFO Overrun Error generates interrupt. Writing a 1 to this bit clears it.
2	FER	R/W	FIFO Error – Underrun or Overrun: 0 – No Error. 1 – Any of FUR or FOR error bits set to active 1 generates FER interrupt. (Acts as a composite FIFO error interrupt.) Writing a 1 to this bit clears it.
3	RNK	R/W	Receive NACK (DB-I2C-S and DB-I2C-M): 0 – No Error. 1 – Receive NACK generates interrupt. For Master-Transmitter, NACK received when ACK expected after Address or Data. For Master-Receiver, NACK received when ACK expected after Address. For Slave-Transmitter, NACK received when ACK expected after Data. Writing a 1 to this bit clears it.
4	ALD	R/W	Arbitration Loss Detected (DB-I2C-MS & DB-I2C-M): 0 – No Error. 1 – Arbitration loss detected. More than one I2C Master Controller on the same I2C Bus, and this controller loss arbitration. Writing a 1 to this bit clears it.
5	FFE	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode): 0 – FIFO not Almost Full or Empty 1 – FIFO has reached parameterized Almost Full or Empty Value Default parameter setting is as follows: // FIFO Almost Full/Empty Threshold parameter FFE_THRESHOLD = 2; Writing a 1 to this bit clears it.



6	TCS	R/W	<p>Transfer Completed - I2C STOP Asserted:</p> <p>0 – Current I2C Bus transfer (for Master Mode, invoked by control bit FTE in Control Register 2) not completed.</p> <p>1 – Current I2C Bus transfer completed.</p> <p>For Master Mode, TCS sets when FSM completes sending/receiving all FBCR number of bytes.</p> <p>For Slave-Receiver Mode, TCS sets when at least 1 byte is loaded into the FIFO and an I2C STOP is detected.</p> <p>For Slave-Transmitter Mode, TCS sets when an I2C STOP is detected.</p> <p>In all four I2C Modes, FBCR can be read for number of bytes transmitted / received.</p> <p>Writing a 1 to this bit clears it.</p>
7	RAK	R/W	<p>Receive ACK (DB-I2C-S):</p> <p>0 – No ACK Received.</p> <p>1 – Receive ACK generates interrupt.</p> <p>Set with each ACK received.</p> <p>Writing a 1 to this bit clears it</p>
8	HNK	R/W	<p>Hs-mode Receive NACK (DB-I2C-M):</p> <p>0 – No Error.</p> <p>1 – Receive NACK in Hs-mode after Hs Master Code sent.</p> <p>For Master-Transmitter or Master-Receiver, in Hs-mode (HSCR).</p> <p>HME=1), after Hs Master Code sent, a NACK successfully received.</p> <p>HNK asserted will suppress interrupt RNK.</p> <p>Writing a 1 to this bit clears it.</p>

7.4.2.10 IMR (Interrupt Mask Register)

Size: 8 bits

Offset: 0x024

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FURM	R/W	FIFO – Underrun – Mask Enable/Disable: 0 – Disable FUR interrupt. 1 – Enable FUR interrupt.
1	FORM	R/W	FIFO – Overrun – Mask Enable/Disable: 0 – Disable FOR interrupt. 1 – Enable FOR interrupt.
2	FERM	R/W	FIFO Error – Underrun or Overrun – Mask Enable/Disable: 0 – Disable FER interrupt. 1 – Enable FER interrupt.
3	RNKM	R/W	Receive NACK – Mask Enable/Disable: 0 – Disable RNK interrupt. 1 – Enable RNK interrupt.
4	ALDM	R/W	Arbitration Loss Detected – Mask Enable/Disable: 0 – Disable ALD interrupt. 1 – Enable ALD interrupt.
5	FFEM	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode) – Mask Enable/Disable: 0 – Disable FFE interrupt. 1 – Enable FFE interrupt.
6	TCSM	R/W	Transfer Completed - I2C STOP Asserted – Mask Enable/Disable: 0 – Disable TCS interrupt. 1 – Enable TCS interrupt.
7	RAKM	R/W	Receive ACK (DB-I2C-S) – Mask Enable/Disable: 0 – Disable RAK interrupt. 1 – Enable RAK interrupt.
8	HNKM	R/W	Hs-mode Receive NACK – Mask Enable/Disable: 0 – Disable HNK interrupt. 1 – Enable HNK interrupt

7.4.2.11 IVR (Interrupt Vector Register)

Size: 8 bits

Offset: 0x028

Memory Access: RO

Value After Reset: 0x00



Bits	Name	Memory Access	Description
0	FURV	R/W	FIFO – Underrun – Enabled Interrupt: Logical AND of FUR and FURM.
1	FORV	R/W	FIFO – Overrun – Enabled Interrupt: Logical AND of FOR and FORM.
2	FERV	R/W	FIFO Error – Underrun or Overrun – Enabled Interrupt: Logical AND of FER and FERM.
3	RNKV	R/W	Receive NACK – Enabled Interrupt: Logical AND of RNK and RNKM.
4	ALDV	R/W	Arbitration Loss Detected – Enabled Interrupt: Logical AND of ALD and ALDM.
5	FFEV	R/W	FIFO Almost Full (receive mode) or Empty (transmit mode) – Enabled Interrupt: Logical AND of FFE and FFEM.
6	TCSV	R/W	Transfer Completed – I2C STOP Asserted – Enabled Interrupt: Logical AND of TCS and TCSM.
7	RAKV	R/W	Receive ACK (DB-I2C-S) – Enabled Interrupt: Logical AND of RAK and RAKM
8	HNKV	R/W	Hs-mode Receive NACK – Enabled Interrupt: Logical AND of HNK and HNKM.

7.4.2.12 FBCR2 (FIFO Byte Count Register 2)

Size: 8 bits

Offset: 0x02C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
3: 0	FBCR2[3:0]	R/W	FIFO Byte Count Register 2 (upper 4-bits of register FBCR): Concatenates with FBCR1[7:0] to form FBCR[11:0].

7.4.2.13 ISR-2 (Interrupt Status Register-2)

Size: 8 bits

Offset: 0x044



Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
[3:0]	Reserved		Not applicable for Master



4	MSH	R/W	<p>Master Slave FIFO Hold (DB-I2C-M & DB-I2C-S) : Master-Transmitter Mode (DB-I2C-M): 0 – Master Not Completed Sending Tx Data & Not Holding I2C Bus Digital Blocks, Inc. DB-I2C CONFIDENTIAL I2C Controller – Master/Slave DB-I2C-TRM-V1.0.8 84 9/14/2021 1 – Master Completed Sending Tx Data & Holds I2C while CPU loads FIFO with more data.</p> <p><u>Slave-Transmitter Mode (DB-I2C-S):</u> 0 – Slave Not Completed Sending Tx Data & Not Holding I2C Bus 1 – Slave Completed Sending Tx Data & Holds I2C while CPU loads FIFO with more data.</p> <p>When CR2.HBD=1, Master-Transmitter or Slave-Transmitter holds I2C Bus by pulling SCL LOW (for Master-Transmitter , after the received ACK from external Slave of received byte, and the Master FIFO transmitting is empty; and for Slave-Transmitter Mode, after the sent ACK of either the Slave Address validated or ACK from external Master of received byte and the FIFO is empty. Interrupt MSH will simultaneously set (to signal processor to re-load FIFO) when SCL pulled low. After FIFO re-loaded, processor clears MSH interrupt, and Master-Transmitter or Slave-Transmitter releases SCL, allowing transaction to continue using FIFO refilled data.</p> <p>This can continue indefinitely until for Master-Transmitter, after re-loading FIFO, clears CR2.HBD, allowing transfer to terminate after all bytes sent; and for Slave-Transmitter , external I2C Master issues NACK. The FIFO is reset flushing potentially unused bytes. Writing a 1 to this bit clears it.</p>
[8:5]	Reserved		Not applicable for Master

9	SS0	R/W	SDA Stuck at 0: (DB-I2C-S & DB-I2C-M only): 0 – SDA stuck at 0 (zero) not detected 1 – SDA stuck at 0 (zero) detected
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7.4.2.14 IMR-2 (Interrupt Mask Register-2)

Size: 8 bits

Offset: 0x048

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
[3:0]	Reserved	R/W	Not applicable for Master
4	MSHM	R/W	Master Slave FIFO Hold: (DB-I2C-MS & DB-I2C-M only) 0 – Disable MSH interrupt. 1 – Enable MSH interrupt.
[8:5]	Reserved		Not applicable for Master
9	SS0M	R/W	SDA Stuck at 0 - Mask Enable/Disable (DB-I2C-M only): 0 – Disable SS0 interrupt. 1 – Enable SS0 interrupt.

7.4.2.15 IVR-2 (Interrupt Vector Register-2)

Size: 8 bits

Offset: 0x04C

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
[3:0]	Reserved	R/W	Not applicable for Master
4	MSHV	R/W	Master Slave FIFO Hold – Enabled Interrupt: (DB-I2C-MS & DB-I2C-M only) Logical AND of MSH and MSHM.
[8:5]	Reserved	R/W	Not applicable for Master
9	SS0V	R/W	SDA Stuck at 0 - Enabled Interrupt (DB-I2C-M only): Logical AND of SS0 and SS0M.

7.4.2.16 SFR (SDA/SCL Spike Filter Rejection)

Size: 32 bits

Offset: 0x064

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
7:0	SFW	R/W	<p>Programmable SDA/SCL Spike Filter Width (DB-I2C-M & DB-I2C-S): 8-bit value that sets the width of the LOW spikes on SDAH/SCLH rejected. Each value indicates number of DB-I2C clock counts. Load with N – 1 value, with N the number of CLK cycles of the spike width rejection</p> <p>As an example, if the input bus fabric clock (e.g. PCLK / HCLK / ACLK/CLK) is 100 MHz, then set SFW = 5-1 = 4 in order to get the minimum 50 ns SDAH/SCLH LOW spike rejection.</p>
15:8			Reserved
31:16	SHW	R/W	<p>Programmable SCL HIGH Width (DB-I2C-S only): 16-bit value that indicates the width of the DB-I2C-S (Slave) incoming SCL HIGH pulse. While field SFW sets the LOW spike width rejection based on the DB-I2C clock, SHW indicates the SCL HIGH pulse length so that the rejection filter turns off when SCL really transitions to LOW. Each value indicates number of DB-I2C clock counts.</p> <p>If input SCL HIGH period is N DB-I2C clocks, then program SHW to N+1</p>

7.4.2.17 HS-CR (Hs-Mode Control Register)

Size: 8 bits

Offset: 0x074

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
2:0	HMC	R/W	<p>Hs-Mode Master Code Number (DB-I2C-MS, DB-I2C-M): 3-bit Hs-Mode Master Code Number that forms the lower 3-bits of the 8-bit Hs Master Code $8b0000_1XXX$ (where XXX = HMC[2:0]) Valid for DB-I2C Master when HME = 1, forming the lower 3-bit field of the first byte Hs-mode Master Code, signaling to the external I2C Slave that the following transaction will be a Hs-Mode 3.4 Mbit/s transfer.</p> <p>Each Hs-Mode I2C Master has its own unique master code, used for arbitration and synchronization, with up to eight Hs-mode masters present on one I2C-bus system.</p>
6:3		R/W	Reserved
7	HME	R/W	<p>Hs-Mode Enable (DB-I2C-MS, DB-I2C-M): 0 – Hs-Mode Disabled. 1 – Hs-Mode Enabled. When HME = 1, then all Master I2C transactions will be Hs-mode transfers, at the 3.4 Mbit/s rate.</p>

7.4.2.18 HS-SCD1 (HS-SCL Clock Divider Register 1)

Size: 8 bits

Offset: 0x078

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	HSLP[7:0]	R/W	<p>HS-mode - SCL LOW Period: In I2C Master Hs-mode (when register HS-CR, bit HME = 1), field HSLP[7:0] programs the SCL LOW period, in number of the primary clock input cycles.</p> <p>To meet Hs-mode timing, $HSLP \times Input\ Clock\ Period$ should equal 160 ns minimum.</p> <p>Note that ($HS-SCD1.HSLP + HS-SCD2.HSHP - 1$) $\times Input\ Clock\ Period$ must equal the Hs-mode 3.4 MHz clock period of 294 ns minimum.</p>



7.4.2.19 HS-SCD2 (HS-SCL Clock Divider Register 2)

Size: 8 bits

Offset: 0x07C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	HSHP[7:0]	R/W	<p>HS-mode - SCL HIGH Period: In I2C Master Hs-mode (when register HS-CR, bit HME = 1), field HSHP[7:0] programs the SCL HIGH period, in number of the primary clock input cycles.</p> <p>To meet Hs-mode timing, <i>HSHP x Input Clock Period</i> should equal 60 ns minimum.</p> <p>Note that (<i>HS-SCD1.HSLP + HS-SCD2.HSHP - 1</i>) <i>x Input Clock Period</i> must equal the Hs-mode 3.4 MHz clock period of 294 ns minimum.</p> <p>Set SCL HIGH (hs_scd2_reg) to value N-1 (one less than the desired value).</p>

7.4.2.20 HS-SFR (Hs-Mode SDA/SCL Spike Filter Rejection)

Size: 8 bits

Offset: 0x80

Memory Access: R/W

Value After Reset: 0x00



Bits	Name	Memory Access	Description
7:0	HSFW[7:0]	R/W	<p>Programmable HS-Mode SDA/SCL Spike Filter Width (DB-I2C-S & DB-I2C-M): 8-bit value that sets the width of the LOW spikes on SDAH/SCLH rejected. Each value indicates number of DB-I2C clock counts. Load with N – 1 value, with N the number of CLK (bus clock APB / HCLK / ACLK) cycles of the spike width rejection As an example, if the input bus fabric clock (e.g. PCLK / HCLK / ACLK / Avalon CLK) is 100 MHz, then set HSFW = 5-1 = 4 in order to get the minimum 50 ns SDAH/SCLH LOW spike rejection.</p> <p>HSFW used during Hs-mode SCL/SDA cycles on the I2C bus, while SFR.SFW is used during Standard/Fast/Fast-mode Plus I2C SCL/SDA cycles.</p> <p>For DB-I2C-M, register HS-SCD2, field HSHP is set to the SCLH HIGH period, which informs the SCL rejection filter the pulse width of SCL the filter should reject spikes.</p> <p>For DB-I2C-S, register HS-SCD2, field HSHP can be used for the same purpose of setting the SCL width the filter should reject spikes. But, the width of the incoming SCL signal needs to be known.</p>

7.4.2.21 TX-FBCAR (TX FIFO Byte Count Actual register)

Bits	Name	Memory Access	Description
7:0	TX-FBCAR[7:0]	R/W	<p>TX-FIFO Byte Count Actual: Number of bytes in TX-FIFO.</p> <p>TX-FBCAR increments with each byte written by CPU to the TX FIFO and decrements with each byte read by I2C Control unit.</p> <p><i>TX-FBCAR shown at 8-bits for 256 byte FIFO implementation</i></p>



7.4.2.22 RX-FBCAR (RX FIFO Byte Count Actual register)

Bits	Name	Memory Access	Description
7:0	RX-FBCAR[7:0]	R/W	<p>RX-FIFO Byte Count Actual: Number of bytes in RX-FIFO. RX-FBCAR increments with each byte written by I2C Control unit to the RX-FIFO and decrements with each byte read by CPU.</p> <p><i>RX-FBCAR shown at 8-bits for 256-byte FIFO implementation</i></p>

7.4.2.23 TX-FAFETR (TX-FIFO Almost full or empty threshold register)

Size: 8 bits

Offset: 0x8C

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	TX-FAFETR[7:0]	R/W	<p>TX FIFO Almost Full or Empty Threshold Register: Programmed threshold value, when TX-FAFETR equal to TX FIFO internal byte count, triggers interrupt FFE in ISR register. Thus, FFE triggered when TX-FAFETR = TX FIFO Byte Count Preset to 0xFF but on startup should be cleared as part of initialization</p>

7.4.2.24 SDSR-I (Programmable SDA Input Delay Select Register)

Size: 8 bits

Offset: 0x90

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
5:0	SDSR-I	R/W	<p>Programmable SDA Input Delay Select Register SDA Input hold time can be extended to 0 to 63 AMBA Clocks</p> <p>Note that register SDSR-I is for SDA Input variable hold delay while SDSR-O is for SDA Output variable hold delay</p>
7:6	Reserved		

7.4.2.25 SDSR-O (Programmable SDA Output Delay Select Register)

Size: 8 bits

Offset: 0x94

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
5:0	SDSR-O	R/W	<p>Programmable SDA Output Delay Select Register SDA Output hold time can be extended to 0 to 63 AMBA Clocks</p> <p>Note that register SDSR-I is for SDA Input variable hold delay while SDSR-O is for SDA Output variable hold delay</p>

7.4.2.26 CIR1 (Core Identification Register 1)

Size: 8 bits

Offset: 0xE0

Memory Access: RO

Value After Reset: 0x04

Bits	Name	Memory Access	Description
7:0	CIR_MN	RO	<p>Core Identification Register – Model Number: 0x1 – Model Number DB-I2C-MS-APB Master/Slave, with APB interface, and FIFOs</p> <p>0x2 – Model Number DB-I2C-MS-AHB Master/Slave, with AHB interface, and FIFOs</p> <p>0x3 – Model Number DB-I2C-MS-AVLN Master/Slave, with Avalon interface, and FIFOs</p> <p>0x4 – Model Number DB-I2C-M-APB Master-only, with APB interface, and FIFOs</p> <p>0x5 – Model Number DB-I2C-M-AHB Master-only, with AHB interface, and FIFOs</p> <p>0x6 – Model Number DB-I2C-M-AVLN Master-only, with Avalon interface, and FIFOs</p> <p>0x7 – Model Number DB-I2C-S-APB Slave-only, with APB interface, and FIFOs</p> <p>0x8 – Model Number DB-I2C-S-AHB Slave-only, with AHB interface, and FIFOs</p> <p>0x9 – Model Number DB-I2C-S-AVLN Slave-only, with Avalon interface, and FIFOs</p> <p>0xA – Model Number DB-I2C-S-RA-AVLN Slave-only, with Register Array</p>

7.4.2.27 CIR2 (Core Identification Register 2)

Size: 8 bits

Offset: 0XE4

Memory Access: RO

Value After Reset: 0x48

Bits	Name	Memory Access	Description
4:0	CIR_REV	RO	Core Identification Register – Revision: 0x00 – Version 1.0.0 0x01 – Version 1.0.1 0x02 – Version 1.0.2 0x03 – Version 1.0.3 0x04 – Version 1.0.4 0x05 – Version 1.0.5 0x06 – Version 1.0.6 0x07 – Version 1.0.7 0x08 – Version 1.0.8
7:5	CIR_BW	RO	Core Identification Register – Bit Width (Processor Slave Bus): 0x2 – 32 Bits 0x1 – 16 Bits 0x0 – 8 Bits



7.5 SPI Master/Slave registers

7.5.1 List of registers and offset details

Register	Offset	Memory Access	Description
CR1	0x000	R/W	Control Register 1
CR2	0x004	R/W	Control Register 2
-	0x008	-	Reserved
TX-FIFO	0x00C	WO	Transmit FIFO Memory
TX-RX FBCR	0x010	R/W	TX-RX FIFO Byte Count Register
TX-FBCAR	0x014	RO	TX FIFO Byte Count Actual Register
TX-FAETR	0x018	R/W	TX FIFO Almost Empty Threshold Register
RX-FIFO	0x01C	RO	Receive FIFO Memory
-	0x020	-	Reserved
RX-FBCAR	0x024	RO	RX FIFO Byte Count Actual Register
RX-FAFTR	0x028	R/W	RX FIFO Almost Full Threshold Register
SCDR	0x02C	R/W	SCK Clock Divider Register
ISR	0x030	R/W	Interrupt Status Register
IMR	0x034	R/W	Interrupt Mask Register
IVR	0x038	RO	Interrupt Vector Register
-	0x03C – 0x044	-	Reserved
TX-FSRBCAR	0x48	RO	TX-FIFO & Output Serial Register Byte Count Actual
CIR1	0x0E0	RO	Core Identification Register 1
CIR2	0x0E4	RO	Core Identification Register 2
-	0x0E8 – 0xFFFF	-	Reserved

7.5.2 Register definition

7.5.2.1 CR1 (Control Register 1)

Size: 8 bits

Offset: 0x000



Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	SCR	R/W	<p>SPI Controller Reset: SCR will ASYNCHRONOUS reset all SCK clock domain logic, the Interrupt Controller, and the TX/RX FIFOs, both SCK and AMBA Clock domains.</p> <p>Note that AMBA domain power-up reset signal db_spi_slv_presetn will reset SCR to 0. Software upon initialization of the DB-SPI should initially set SCR to 1.</p> <p>Values:</p> <p>0 – SPI Controller ASYNCHRONOUS reset. While set to 0, the SPI Controller is held in reset. Thus, the user resets the SPI Controller by writing a 0 followed by writing a 1.</p> <p>1 – No reset.</p>
1	SCE	R/W	<p>SPI Controller Enable:</p> <p>Values:</p> <p>0 – Disables SPI Controller IP Core. The SPI Controller will not initiate a Master transaction nor respond to an external SPI Master.</p> <p>1 – Enables SPI Controller IP Core. The SPI Controller can initiate a Master transaction (CR1.MSS=0) or respond as a SPI Slave (CR1.MSS=1) to an external SPI Master.</p> <p>SCE serves as an overriding enable / disable</p>
2	MSS	R/W	<p>Master / Slave Select (DB-SPI-MS only):</p> <p>Values:</p> <p>0 – SPI Controller set to Master Mode.</p> <p>1 – SPI Controller set to Slave Mode</p> <p>MSS cleared to 0 (Master Mode) as well as SCE set to 1 for SPI Controller to initiate as SPI Master with external SPI Slave Write/Read transfers. Transfers invoked when CR2.MTE set to 1</p> <p>MSS set to 1 (Slave Mode) as well as SCE set to 1 for SPI Controller to respond as SPI Slave to external SPI Master Write/Read transfers</p>



Bits	Name	Memory Access	Description
3	CPH	R/W	SPI Clock Phase: 0 – Sampling of data occurs at odd edges (1,3,5, ...) of SCK 1 – Sampling of data occurs at even edges (2,4,6, ...) of SCK
4	CPO	R/W	SPI Clock Polarity: CPO selects the polarity of the inactive state of SCK. 0 – SCK held low in the inactive state. 1 – SCK held high in the inactive.
7:5	-	RO	Reserved bits and read as zero (0).



7.5.2.2 CR2 (Control Register 2)

Size: 8 bits

Offset: 0x004

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
1:0	SSO	R/W	<p>Slave Select Output Selection (DB-SPI-M only): DB-SPI outputs SS[7:0]serves as SPI Master output Slave Select 00 – SS0 – Slave Select 0 01 – SS1 10 – SS2 11 – SS3 – Slave Select 3 Note: In SPI Master mode, the processor software sets-up CR2.SSO as chip select for a transfer to particular SPI Slave, which is conditioned by the DB-SPI-M control unit driving the actual SS_n output.</p>
2	SWD	R/W	<p>SPI Write Disable: 0 – Disable Transmit logic 1 – Enable Transmit logic When disabled, TX-FIFO and TX Shift Register inhibited from popping data from TX_FIFO and transmitting to external SPI Slave. Used for half-duplex communications, with SPI Read only transfer. Valid only in DB-SPI-S (Slave Function).</p>



Bits	Name	Memory Access	Description
3	SRD	R/W	<p>SPI Read Disable (DB-SPI-M only): 0 – Disable Receive logic 1 – Enable Receive logic</p> <p>When disabled, RX-FIFO, RX Shift Register, and RX Control inhibited from accepting data input and storing in the RX-FIFO</p> <p>Used for half-duplex communications, with SPI Write only transfer.</p>
4	SRI	R/W	<p>SPI Read First Byte Ignore (DB-SPI-M only): 0 – Accept and Write into RX-FIFO starting with FIRST Byte in SPI Read 1 – Accept and Write into RX-FIFO starting with SECOND Byte in SPI Read</p> <p>SPI Master reads typical first write a command to the SPI Slave to be followed by SPI Read Data starting on the 9th SPI SCK</p> <p>SRI=1 enables ignoring of the FIRST data byte read making it simpler for the CPU when reading the RX-FIFO.</p> <p>Note that CR2.SRD must equal 1</p>
5	MLB	R/W	<p>Most or Least Significant Bit First Transmitted/Received: 0 – Data Transmitted/Received most significant bit first (MSB first). 1 – Data Transmitted/Received least significant bit first (LSB first).</p>
6	MTE	R/W	<p>Master Transfer Enable: 0 – SPI Master transfer inactive. 1 – SPI Master transfer on SPI Bus active.</p> <p>Setting MTE initiates the SPI Control to conduct a SPI Master transfer</p> <p>MTE set by CPU indicating SPI master configured and data transferred should be initiated. Once MTE invokes the transfer, and the transfer, completes, MTE self-clears.</p>
7	-	RO	Reserved bits and read as zero (0).



7.5.2.3 TX-FIFO (TX FIFO MEMORY)

Size: 8 bits

Offset: 0x00C

Memory Access: WO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	TXFIFO	WO	Host Processor single address interface to TX-FIFO. A write will PUSH a byte onto the FIFO memory.

7.5.2.4 TX-RX FBCR (TX RX-FIFO Byte Count Register)

Size: 8 bits

Offset: 0x010

Memory Access: WO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	TX_RX_FBCR	WO	TX- RX -FIFO Byte Count Register: Used by Master-Receive when Master Transmitter inactive. That is, in half duplex mode, when SPI Master RX-FIFO receives burst without TX-FIFO filled by CPU and sending data on MO output. TX-RX-FBCR is set with the number of bytes the SPI Master Receive should read from the external SPI Slave. TX-RX-FBCR used when CR2.SWD=0 (SPI Master-Receive only).

7.5.2.5 TX-FBCAR (TX FIFO Byte Count Actual Register)

Size: 8 bits

Offset: 0x014

Memory Access: RO

Value After Reset: 0x00



Bits	Name	Memory Access	Description
7:0	TX_FBCAR	RO	TX-FIFO Byte Count Actual: Number of bytes in TX-FIFO. TX-FBCAR increments (in AMBA clock domain) with each byte written by CPU to the TX-FIFO and decrements (in SCK clock domain) with each byte read by SPI Control unit

7.5.2.6 TX-FAETR (TX FIFO Almost Empty Threshold Register)

Size: 9 bits

Offset: 0x018

Memory Access: R/W

Value After Reset: 0x1FF

Bits	Name	Memory Access	Description
8:0	TX_FAETR	R/W	TX FIFO Almost Empty Threshold Register: Programmed threshold value, when TX-FAETR greater than or equal to TX FIFO internal byte count, triggers interrupt TFE in ISR register. Thus, TFE triggered when TX-FAFTR => TX FIFO Byte Count Preset to 0xFF in order to match RX-FAFTR (but TFE will still set on startup and need to be cleared as part of initialization).

7.5.2.7 RX-FIFO (RX FIFO MEMORY)

Size: 8 bits

Offset: 0x01C

Memory Access: RO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	RXFIFO	RO	Host Processor single address interface to RX-FIFO. A read will POP a byte.



7.5.2.8 RX-FBCAR (RX FIFO Byte Count Actual Register)

Size: 8 bits

Offset: 0x024

Memory Access: RO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	RXFBCAR	RO	<p>RX-FIFO Byte Count Actual: Number of bytes in RX-FIFO.</p> <p>RX-FBCAR increments (in SCK clock domain) with each byte written by SPI Control unit to the RX-FIFO and decrements (in AMBA clock domain) with each byte read by CPU.</p> <p>RX-FBCAR shown at 8-bits for 256-byte FIFO implementation.</p>

7.5.2.9 RX-FAFTR (RX FIFO Almost Full Threshold Register)

Size: 9 bits

Offset: 0x028

Memory Access: R/W

Value After Reset: 0x1FF

Bits	Name	Memory Access	Description
8:0	RXFATR	R/W	<p>RX FIFO Almost Full Threshold Register: Programmed threshold value, when RX FIFO internal byte count greater than or equal to RX-FAFTR, triggers interrupt RFF in ISR register.</p> <p>Thus, RFF triggered when RX FIFO Byte Count => RX-FAFTR</p> <p>Preset to 0xFF in order not to latch RFF interrupt on reset.</p> <p>RX-FAFTR shown at 8-bits for 256-byte FIFO implementation</p>

7.5.2.10 SCDR (SCK Clock Divider Register)

Size: 10 bits

Offset: 0x02C

Memory Access: R/W

Value After Reset: 0x000



Bits	Name	Memory Access	Description
8:0	SCD	R/W	SCK Clock Divider Register (DB-SPI-M only): The frequency of SPI Master SCK output divided down from the AMBA Slave clock input. $SCK = \text{AMBA Slave clock} / (\text{SCD} + 2)$ Valid SCD values are 9'h000 – 9'h1FE. User should program with even values (thus, Valid when SCS = 1). SCK value maximum is (AMBA Slave clock) / 2.
9	SCS	R/W	SCK Clock Source: 0 – SCK Clock Source in DB-SPI-M is SPI_M_CLK_EXT external clock 1 – SCK Clock Source in DB-SPI-M is output of clock divider programmed by SCDR field SCD, with AMBA Slave the clock source Enabled Clock Divider, with AMBA Slave the clock source, and controls clock mux in DB-SPI-M

7.5.2.11 ISR (Interrupt Status Register)

Size: 8 bits

Offset: 0x030

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	TFU	R/W	Transmit (TX) FIFO - Underrun: 0 – No Error. 1 – TX FIFO Underrun Error generates interrupt. Writing a 1 to this bit clears it. TFU originates in SCK clock domain and synchronized via 2 FFs to AMBA clock domain
1	TFO	R/W	Transmit (TX) FIFO - Overrun: 0 – No Error. 1 – TX FIFO Overrun Error generates interrupt. Writing a 1 to this bit clears it.
2	RFU	R/W	Receive (RX) FIFO - Underrun: 0 – No Error. 1 – RX FIFO Underrun Error generates interrupt. Writing a 1 to this bit clears it.



Bits	Name	Memory Access	Description
3	RFO	R/W	<p>Receive (RX) FIFO - Overrun: 0 – No Error. 1 – RX FIFO Overrun Error generates interrupt. Writing a 1 to this bit clears it.</p> <p>RFO originates in SCK clock domain and synchronized via 2 FFs to AMBA clock domain.</p>
4	TFE	R/W	<p>Transmit (TX) FIFO Almost Empty: 0 – FIFO not Almost Empty 1 – FIFO has reached Almost Empty Value set by register TX FIFO Almost Empty Threshold Register (TX-FAETR)</p> <p>Note that TFE is a greater than or equal to threshold detect – that is, when the number of bytes in the TX FIFO are \geq to register TX-FAETR value, interrupt TFE asserts.</p> <p>Writing a 1 to this bit clears it.</p>
5	RFF	R/W	<p>Receive (RX) FIFO Almost Full: 0 – FIFO not Almost Full 1 – FIFO has reached Almost Full Value set by register RX FIFO Almost Full Threshold Register (RX-FAFTR)</p> <p>RFF is a greater than or equal to threshold detect – that is, when the number of bytes in the RX FIFO are \geq to register RX-FAFTR value, interrupt RFF asserts.</p> <p>Writing a 1 to this bit clears it.</p>
6	MTC	R/W	<p>SPI Master Transmit/Receive Transfer Completed: 0 – Current SPI Master transfer not completed. 1 – Current SPI Master transfer completed.</p> <p>For SPI Master, MTC sets when SPI Master Control completes sending all bytes in the TX-FIFO (as signaled by the TX-FIFO empty signal) and SSn de-asserts.</p> <p>Writing a 1 to this bit clears it.</p>
7	STC	R/W	<p>SPI Slave Transmit/Receive Transfer Completed: 0 – DB-SPI does Not detect a SPI Slave transfer completed. 1 – DB-SPI detects a SPI Slave transfer completed.</p> <p>For SPI Slave, STC sets by the SPI Slave Control with the detection of SSn input de-asserting.</p> <p>Writing a 1 to this bit clears it.</p>



7.5.2.12 IMR (Interrupt Mask Register)

Size: 8 bits

Offset: 0x034

Memory Access: R/W

Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	TFUM	R/W	Transmit (TX) FIFO – Underrun – Mask Enable/Disable: 0 – Disable TFUR interrupt. 1 – Enable TFUR interrupt.
1	TFOM	R/W	Transmit (TX) FIFO – Overrun – Mask Enable/Disable: 0 – Disable TFOR interrupt. 1 – Enable TFOR interrupt.
2	RFUM	R/W	Receive (RX) FIFO – Underrun – Mask Enable/Disable: 0 – Disable RFUR interrupt. 1 – Enable RFUR interrupt.
3	RFOM	R/W	Receive (RX) FIFO – Overrun – Mask Enable/Disable: 0 – Disable RFOR interrupt. 1 – Enable RFOR interrupt.
4	TFEM	R/W	Transmit (TX) FIFO Almost Empty – Mask Enable/Disable: 0 – Disable TFE interrupt. 1 – Enable TFE interrupt.
5	RFFM	R/W	Receive (RX) FIFO Almost Full – Mask Enable/Disable: 0 – Disable RFF interrupt. 1 – Enable RFF interrupt.
6	MTCM	R/W	SPI Master Transmit/Receive Transfer Completed – Mask Enable/Disable: 0 – Disable MTC interrupt. 1 – Enable MTC interrupt.
7	STCM	R/W	SPI Slave Transmit/Receive Transfer Completed – Mask Enable/Disable: 0 – Disable SRC interrupt. 1 – Enable SRC interrupt.

7.5.2.13 IVR (Interrupt Vector Register)

Size: 8 bits

Offset: 0x038

Memory Access: RO



Value After Reset: 0x00

Bits	Name	Memory Access	Description
0	TFUV	RO	Transmit (TX) FIFO – Underrun – Enabled Interrupt: Logical AND of TFU and TFUM.
1	TFOV	RO	Transmit (TX) FIFO – Overrun – Enabled Interrupt: Logical AND of TFO and TFOM.
2	RFUV	RO	Receive (RX) FIFO – Underrun – Enabled Interrupt: Logical AND of RFU and RFUM.
3	RFOV	RO	Receive (RX) FIFO – Overrun – Enabled Interrupt: Logical AND of RFO and RFOM.
4	TFEV	RO	Transmit (TX) FIFO Almost Empty – Enabled Interrupt: Logical AND of TFE and TFEM.
5	RFFV	RO	Receive (RX) FIFO Almost Full – Enabled Interrupt: Logical AND of RFF and RFFM.
6	MTCV	RO	SPI Master Transmit/Receive Transfer Completed – Enabled Interrupt: Logical AND of MTC and MTCM.
7	STCV	RO	SPI Slave Transmit/Receive Transfer Completed – Enabled Interrupt: Logical AND of STC and STCM.

7.5.2.14 TX-FSRBCAR (TX FIFO & Output Serial Reg Byte Count Actual Register)

Size: 8 bits

Offset: 0x048

Memory Access: RO

Value After Reset: 0x00

Bits	Name	Memory Access	Description
7:0	TXFSRB CAR	RO	TX-FIFO & Output Serial Register Byte Count Actual: Number of bytes in TX-FIFO & Serial Output Register. When a byte is read from the TX-FIFO to send on the SPI data bus, TX- FSRBCAR counter



Bits	Name	Memory Access	Description
			includes the bytes in the TX-FIFO and if there is 1 byte in the output serial register being transmitted.

7.5.2.15 CIR1 (Core Identification Register 1)

Size: 8 bits

Offset: 0x0E0

Memory Access: RO

Value After Reset: 0x01

Bits	Name	Memory Access	Description
7:0	CIR_MN	RO	<p>Core Identification Register – Model Number: 0x1 – Model Number DB-SPI-MS-APB Master/Slave, with APB interface, and 2 FIFOs 0x2 – Model Number DB-SPI-MS-AHB Master/Slave, with AHB interface, and 2 FIFOs 0x3 – Model Number DB-SPI-MS-AVNL Master/Slave, with Avalon interface, and 2 FIFOs 0x4 – Model Number DB-SPI-M-APB Master-only, with APB interface, and 2 FIFOs 0x5 – Model Number DB-SPI-M-AHB Master-only, with AHB interface, and 2 FIFOs 0x6 – Model Number DB-SPI-M-AVNL Master-only, with Avalon interface, and 2 FIFOs 0x7 – Model Number DB-SPI-S-APB Slave-only, with APB interface, and 2 FIFOs 0x8 – Model Number DB-SPI-S-AHB Slave-only, with AHB interface, and 2 FIFOs 0x9 – Model Number DB-SPI-S-AVNL Slave-only, with Avalon interface, and 2 FIFOs </p>

7.5.2.16 CIR2 (Core Identification Register 2)

Size: 8 bits

Offset: 0x0E4

Memory Access: RO

Value After Reset: 0x01

Bits	Name	Memory Access	Description
4:0	CIR_REV	RO	Core Identification Register – Revision: 0x00 – Version 1.0.0 0x01 – Version 1.0.1 0x02 – Version 1.0.2
7:5	CIR_BW	RO	Core Identification Register – Bit Width (Processor Slave Bus): 0x2 – 32 Bits 0x1 – 16 Bits 0x0 – 8 Bits



7.6 I3C Master/Slave registers

7.6.1 List of registers and offset details



Register	Offset	Memory Access	Description
DEVICE_CTRL	0x0000	RW	Device Control Register
DEVICE_ADDR	0x0004	RW	Device Address Register
HW_CAPABILITY	0x0008	RO	Hardware Capability register
COMMAND_QUEUE_PORT	0x000C	WO	COMMAND_QUEUE_PORT
RESPONSE_QUEUE_PORT	0x0010	RO	RESPONSE_QUEUE_PORT
TX_DATA_PORT	0x0014	WO	Transmit Data Port Register
RX_DATA_PORT	0x0014	RO	Receive Data Port Register
IBI_QUEUE_STATUS	0x0018	RO	In-Band Interrupt Queue Status Register
QUEUE_THRESHOLD_CTRL	0x001C	RW	Queue Threshold Control Register
DATA_BUFFER_THRESHOLD_CTRL	0x0020	RW	Data Buffer Threshold Control Register
IBI_QUEUE_CTRL	0x0024	RW	IBI Queue Control Register
IBI_MR_REQ_REJECT	0x002C	RW	IBI MR Request Rejection Control Register
IBI_SIR_REQ_REJECT	0x0030	RW	IBI SIR Request Rejection Control Register
RESET_CTRL	0x0034	RW	Reset Control Register
SLV_EVENT_STATUS	0x0038	RW	Slave Event Status Register
INTR_STATUS	0x003C	RW	Interrupt Status Register
INTR_STATUS_ENABLE	0x0040	RW	Interrupt Status Enable Register
INTR_SIGNAL_ENABLE	0x0044	RW	Interrupt Signal Enable Register
INTR_FORCE	0x0048	WO	Interrupt Force Enable Register
QUEUE_STATUS_LEVEL	0x004C	RO	Queue Status Level Register
DATA_BUFFER_STATUS_LEVEL	0x0050	RO	Data Buffer Status Level Register
PRESENT_STATE	0x0054	RO	Present State Register
CCC_DEVICE_STATUS	0x0058	RO	Device Operating Status Register
DEVICE_ADDRESS_TABLE_POINTER	0x005C	RO	Pointer for Device Address Table Registers
DEV_CHAR_TABLE_POINTER	0x0060	RO	Pointer for Device Characteristics Table



VENDOR_SPECIF IC_REG_POINTE R	0x006C	RO	Pointer for Vendor specific Registers
SLV_MIPI_ID_VA LUE	0x0070	RW	Provisional ID Register
SLV_PID_VALUE	0x0074	RW	Provisional ID Register
SLV_CHAR_CTR L	0x0078	RW	I3C Slave Characteristic Register
SLV_MAX_LEN	0x007C	RO	I3C Max Write/Read Length Register
MAX_READ_TUR NAROUND	0x0080	RO	MXDS Maximum Read Turnaround Time Register
MAX_DATA_SPE ED	0x0084	RO	MXDS Maximum Data Speed Register
SLV_INTR_REQ	0x008C	RW	Slave Interrupt Request Register
DEVICE_CTRL_E XTENDED	0x00B0	RW	Device Control Extended Register
SCL_I3C_OD_TIM ING	0x00B4	RW	SCL I3C Open Drain Timing Register
SCL_I3C_PP_TIMI NG	0x00B8	RW	SCL I3C Push Pull Timing Register
SCL_I2C_FM_TIM ING	0x00BC	RW	SCL I2C Fast Mode Timing Register
SCL_I2C_FMP_TI MING	0x00C0	RW	SCL I2C Fast Mode Plus Timing Register
SCL_EXT_LCNT_ TIMING	0x00C8	RW	SCL Extended Low Count Timing Register
SCL_EXT_TERM N_LCNT_TIMING	0x00CC	RW	SCL Termination Bit Low count Timing Register
SDA_HOLD_SWI TCH_DLY_TIMIN G	0x00D0	RW	SDA Hold and Mode Switch Delay Timing Register
BUS_FREE_AVAI L_TIMING	0x00D4	RW	Bus Free Timing Register
BUS_IDLE_TIMIN G	0x00D8	RW	Bus Idle Timing Register
SCL_LOW_MST_ EXT_TIMEOUT	0x00DC	RW	SCL_LOW_MST_TIMEOUT
I3C_VER_ID	0x00E0	RO	DWC_mipi_i3c Version ID Register
I3C_VER_TYPE	0x00E4	RO	DWC_mipi_i3c Version Type Register
QUEUE_SIZE_CA PABILITY	0x00E8	RO	DWC_mipi_i3c Queue Size Capability Register



DEV_CHAR_TAB LE1_LOC1	0x0200	RW	Device Characteristic Table Location-1 of Device1 This register is used in master mode of... operation
DEV_CHAR_TAB LE1_LOC2	0x0204	RW	Device Characteristic Table Location-2 of Device1 This register is used in master mode of... operation
DEV_CHAR_TAB LE1_LOC3	0x0208	RW	Device Characteristic Table Location-3 of Device1 This register is used in master mode of... operation
DEV_CHAR_TAB LE1_LOC4	0x020C	RW	Device Characteristic Table Location-4 of Device1 This register is used in master mode of... operation
DEV_CHAR_TAB LE2_LOC1	0x0210	RW	Device Characteristic Table Location-1 of Device2 This register is used in master mode of operation
DEV_CHAR_TAB LE2_LOC2	0x0214	RW	Device Characteristic Table Location-2 of Device2 This register is used in master mode of operation
DEV_CHAR_TAB LE2_LOC3	0x0218	RW	Device Characteristic Table Location-3 of Device2 This register is used in master mode of operation
DEV_CHAR_TAB LE2_LOC4	0x021C	RW	Device Characteristic Table Location-4 of Device2 This register is used in master mode of operation
DEV_CHAR_TAB LE3_LOC1	0x0220	RW	Device Characteristic Table Location-1 of Device3 This register is used in master mode of operation
DEV_CHAR_TAB LE3_LOC2	0x0224	RW	Device Characteristic Table Location-2 of Device3 This register is used in master mode of operation
DEV_CHAR_TAB LE3_LOC3	0x0228	RW	Device Characteristic Table Location-3 of Device3 This register is used in master mode of operation
DEV_CHAR_TAB LE3_LOC4	0x022C	RW	Device Characteristic Table Location-4 of Device3 This register is used in master mode of operation
DEV_CHAR_TAB LE4_LOC1	0x0230	RW	Device Characteristic Table Location-1 of Device4 This register is used in master mode of operation



DEV_CHAR_TAB LE4_LOC2	0x0234	RW	Device Characteristic Table Location-2 of Device4 This register is used in master mode of operation
DEV_CHAR_TAB LE4_LOC3	0x0238	RW	Device Characteristic Table Location-3 of Device4 This register is used in master mode of operation
DEV_CHAR_TAB LE4_LOC4	0x023C	RW	Device Characteristic Table Location-4 of Device4 This register is used in master mode of operation
DEV_CHAR_TAB LE5_LOC1	0x0240	RW	Device Characteristic Table Location-1 of Device5 This register is used in master mode of operation
DEV_CHAR_TAB LE5_LOC2	0x0244	RW	Device Characteristic Table Location-2 of Device5 This register is used in master mode of operation
DEV_CHAR_TAB LE5_LOC3	0x0248	RW	Device Characteristic Table Location-3 of Device5 This register is used in master mode of operation
DEV_CHAR_TAB LE5_LOC4	0x024C	RW	Device Characteristic Table Location-4 of Device5 This register is used in master mode of operation
DEV_CHAR_TAB LE6_LOC1	0x0250	RW	Device Characteristic Table Location-1 of Device6 This register is used in master mode of operation
DEV_CHAR_TAB LE6_LOC2	0x0254	RW	Device Characteristic Table Location-2 of Device6 This register is used in master mode of operation
DEV_CHAR_TAB LE6_LOC3	0x0258	RW	Device Characteristic Table Location-3 of Device6 This register is used in master mode of operation
DEV_CHAR_TAB LE6_LOC4	0x025C	RW	Device Characteristic Table Location-4 of Device6 This register is used in master mode of operation
DEV_CHAR_TAB LE7_LOC1	0x0260	RW	Device Characteristic Table Location-1 of Device7 This register is used in master mode of operation
DEV_CHAR_TAB LE7_LOC2	0x0264	RW	Device Characteristic Table Location-2 of Device7 This register is used in master mode of operation
DEV_CHAR_TAB LE7_LOC3	0x0268	RW	Device Characteristic Table Location-3 of Device7 This register is used in master mode of operation



DEV_CHAR_TAB LE7_LOC4	0x026C	RW	Device Characteristic Table Location-4 of Device7 This register is used in master mode of operation
DEV_CHAR_TAB LE8_LOC1	0x0270	RW	Device Characteristic Table Location-1 of Device8 This register is used in master mode of operation
DEV_CHAR_TAB LE8_LOC2	0x0274	RW	Device Characteristic Table Location-2 of Device8 This register is used in master mode of operation
DEV_CHAR_TAB LE8_LOC3	0x0278	RW	Device Characteristic Table Location-3 of Device8 This register is used in master mode of operation
DEV_CHAR_TAB LE8_LOC4	0x027C	RW	Device Characteristic Table Location-4 of Device8 This register is used in master mode of operation
DEV_CHAR_TAB LE9_LOC1	0x0280	RW	Device Characteristic Table Location-1 of Device9 This register is used in master mode of operation
DEV_CHAR_TAB LE9_LOC2	0x0284	RW	Device Characteristic Table Location-2 of Device9 This register is used in master mode of operation
DEV_CHAR_TAB LE9_LOC3	0x0288	RW	Device Characteristic Table Location-3 of Device9 This register is used in master mode of operation
DEV_CHAR_TAB LE9_LOC4	0x028C	RW	Device Characteristic Table Location-4 of Device9 This register is used in master mode of operation
DEV_CHAR_TAB LE10_LOC1	0x0290	RW	Device Characteristic Table Location-1 of Device10 This register is used in master mode of operation
DEV_CHAR_TAB LE10_LOC2	0x0294	RW	Device Characteristic Table Location-2 of Device10 This register is used in master mode of operation
DEV_CHAR_TAB LE10_LOC3	0x0298	RW	Device Characteristic Table Location-3 of Device10 This register is used in master mode of operation
DEV_CHAR_TAB LE10_LOC4	0x029C	RW	Device Characteristic Table Location-4 of Device10 This register is used in master mode of operation
DEV_CHAR_TAB LE11_LOC1	0x02A0	RW	Device Characteristic Table Location-1 of Device11 This register is used in master mode of operation

DEV_CHAR_TAB LE11_LOC2	0x02A4	RW	Device Characteristic Table Location-2 of Device11 This register is used in master mode of operation
DEV_CHAR_TAB LE11_LOC3	0x02A8	RW	Device Characteristic Table Location-3 of Device11 This register is used in master mode of operation
DEV_CHAR_TAB LE11_LOC4	0x02AC	RW	Device Characteristic Table Location-4 of Device11 This register is used in master mode of operation
DEV_ADDR_TAB LE_LOC1	0x02C0	RW	Device Address Table Location of Device1
DEV_ADDR_TAB LE_LOC2	0x02C4	RW	Device Address Table Location of Device2
DEV_ADDR_TAB LE_LOC3	0x02C8	RW	Device Address Table Location of Device3
DEV_ADDR_TAB LE_LOC4	0x02CC	RW	Device Address Table Location of Device4
DEV_ADDR_TAB LE_LOC5	0x02D0	RW	Device Address Table Location of Device5
DEV_ADDR_TAB LE_LOC6	0x02D4	RW	Device Address Table Location of Device6
DEV_ADDR_TAB LE_LOC7	0x02D8	RW	Device Address Table Location of Device7
DEV_ADDR_TAB LE_LOC8	0x02DC	RW	Device Address Table Location of Device8
DEV_ADDR_TAB LE_LOC9	0x02E0	RW	Device Address Table Location of Device9
DEV_ADDR_TAB LE_LOC10	0x02E4	RW	Device Address Table Location of Device10
DEV_ADDR_TAB LE_LOC11	0x02E8	RW	Device Address Table Location of Device11



7.6.2 Register definition

7.6.2.1 DEVICE_CTRL

Size: 32 bits

Offset: 0x0000

Bits	Name	Memory Access	Description
8:0	IBA_INCLUDE	RW	I3C Broadcast Address include This bit is used in Master mode of operation. This bit is used to include DWC_mipi_i3c broadcast address (0x7E) for private transfer. Note: If DWC_mipi_i3c broadcast address is not included for the private transfers, In-band Interrupts (IBI) driven from Slaves might not win address arbitration. Hence, the IBIs get delayed. Values:0x0 (NOT_INCLUDED): I3C Broadcast Address is not included for Private Transfers0x1 (INCLUDED): I3C Broadcast Address is included for Private Transfers Value After Reset: 0x0
6:1	Reserved_1_6	RO	Reserved Field: Yes
7	I2C_SLAVE_PRESENT	RW	I2C Slave Present This bit is used in master mode of operation. This bit indicates whether any Legacy I2C devices are present in the system. In HDR mode, this field is used to select TSL over TSP in a mixed bus configuration.Values:0x0 (DISABLED): I2C Slave not present0x1 (ENABLED): I2C Slave present Value After Reset: 0x0
8	HOT_JOIN_CTRL	RW	Hot-Join ACK/NACK Control This bit is used in master mode of operation. This bit acts as a global control to ACK/NACK the Hot-Join request from the devices. The DWC_mipi_i3c Master ACK/NACKs the Hot-Join request from other devices connected on the DWC_mipi_i3c bus, based on



Bits	Name	Memory Access	Description
			programming of this bit.0: ACK the Hot-join request.1: NACK and send broadcast CCC to disable Hot-Join.Values:0x0 (DISABLED): Ack Hot-Join requests0x1 (ENABLED): Nack and auto-disable Hot-Join request Value After Reset: 0x0
23:9	Reserved_9_23	RO	Reserved Field: Yes
25:24	IDLE_CNT_MULTIPLIER	RW	Idle Count Multiplier This bit is used in Slave mode of operation. After power-on reset, the Slave controller is enabled only after it sees both SDA and SCL lines idle for a specified time. This idle time is calculated by multiplying IDLE_CNT_MULTIPLIER with BUS_AVAILABLE_TIME field in the BUS_FREE_AVAIL_TIMING register. - 00 - BUS_AVAILABLE_TIME * 1 - 01 - BUS_AVAILABLE_TIME * 2 - 10 - BUS_AVAILABLE_TIME * 4 - 11 - BUS_AVAILABLE_TIME * 8 Value After Reset: 0x0
26	Reserved_26_26	RO	Reserved Field: Yes
27	ADAPTIVE_I2C_I3C	RW	This field is used in Slave mode of operation. Note that when mode_i2c strap is driven to '0', the Slave controller operates in Adaptive Mode. Setting of this bit is NOT required to put the controller in Adaptive Mode. It is only used to enable some features of the Slave controller to adapt to "Adaptive I2C/I3C mode" of operation. This bit is cleared automatically if the controller determines the mode as I3C. Effect on Hot-Join: If this bit is programmed to 1'b1, the controller initiates a Hot-Join request only after it has switched to I3C mode of operation. If this bit is not set, the



Bits	Name	Memory Access	Description
			controller initiates a Hot-Join without determining the bus mode assuming itself to be on DWC_mipi_i3c bus. This bit should be set only if the Slave application does not know to which bus the device is connected to. Value After Reset: 0x0 Volatile: true
28	Reserved_28_28	RO	Reserved Field: Yes
29	ABORT	RW	DWC_mipi_i3c Abort This bit is used in Master mode of operation. This bit allows the controller to relinquish the DWC_mipi_i3c bus before completing the issued transfer. In response to an ABORT request, the controller issues the STOP condition after the complete data byte is transferred or received. This bit is auto-cleared once the transfer is aborted and the controller issues a 'Transfer Abort' interrupt. Value After Reset: 0x0 Volatile: true
30	RESUME	RW	DWC_mipi_i3c Resume This bit is used to resume the controller after it goes to the halt state. In the Master mode of operation, the controller goes to the halt state (as indicated in PRESENT_STATE Register) due to any type of error in the transfer (the type of error is indicated by ERR_STATUS field in the RESPONSE_QUEUE_PORT register). After the controller goes to the halt state, the application must write 1'b1 to this bit to resume the controller. This bit is auto-cleared once the controller resumes the transfers by initiating the next command. In the Slave mode of operation, the controller goes to the halt state due to following conditions: Any type of error in the transfer



Bits	Name	Memory Access	Description
			<p>(the type of error is indicated by ERR_STATUS field in the RESPONSE_QUEUE_PORT register) MRL Register updated by the master through SETMRL CCC. After the controller goes to the halt state, the application must take necessary action to handle the error condition and then write 1'b1 to this bit to resume the controller. This bit is auto cleared once the controller is ready to accept new transfers.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
31	ENABLE	RW	<p>Controls whether DWC_mipi_i3c is enabled.1: Enables the DWC_mipi_i3c controller.0: Disables the DWC_mipi_i3c controller. In Master mode of operation, software can disable DWC_mipi_i3c while it is active. However, the controller may not get disabled immediately and is 'Disabled' after commands in the Command queue (if any) are executed leading to a STOP condition on the bus and Master FSM is in IDLE state (as indicated by PRESENT_STATE Register). In Slave mode of operation, software can disable DWC_mipi_i3c while it is active. However, the disable happens after the ongoing transfer is completed on the I3C bus. Software can read back 1'b0 from this field once disabling of DWC_mipi_i3c is completed. After power on reset, the software can enable I3C slave controller by programming this bit to 1'b1. However, the I3C bus interface of the controller, responds to transfer on the bus only after it observes Bus Available condition for BUS_AVAILABLE_TIME*IDLE_CNT_MULTPLI</p>



Bits	Name	Memory Access	Description
			<p>ER counts of pclk period. The successful completion of Enable/Disable of the controller depends on availability of SCL to the controller at the time of performing this operation, and hence may not happen instantly.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>

7.6.2.2 DEVICE_ADDR

Size: 32 bits

Offset: 0x0004

Bits	Name	Memory Access	Description
6:0	STATIC_ADDR	RW	<p>Device Static Address.</p> <p>In slave mode of operation this field reflects the value of static_addr input port. The controller uses this address to respond to SETDASA CCC Command to get the Dynamic Address if static address is valid (static_addr_en port is set to 1).</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
14:7	Reserved_7_14	RO	Reserved Field: Yes
15	STATIC_ADDR_VALID	RW	<p>Static Address Valid.</p> <p>In slave mode of operation this bit reflects the value of static_addr_en input port. The input port static_addr_en is expected to be driven to 1 only if the device supports I2C or I3C Static Address.</p> <p>Values:</p>



Bits	Name	Memory Access	Description
			0x0 (INVALID): Static Address is invalid 0x1 (VALID): Static Address is valid Value After Reset: 0x0 Volatile: true
22:16	DYNAMIC_ADDR	RW	Device Dynamic Address. This field is used to program the Device Dynamic Address. The Controller uses this address for I3C transfers. In Main Master mode, the user/application has to program the Dynamic Address through the Slave interface as it self-assigns its Dynamic Address. In all other modes, the Main Master assigns this address during ENTDA or SETDASA mechanism. The Main Master assigns this address during ENTDA or SETDASA mechanism. Value After Reset: 0x0 Volatile: true
30:23	Reserved_23_30	RO	Reserved Field: Yes
31	DYNAMIC_ADDR_VALID	RW	Dynamic Address Valid This bit is used to control whether the DYNAMIC_ADDR is valid or not. In I3C Main Master mode, the user sets this bit to 1 as it self-assigns its dynamic address. In all other operation modes, the Controller sets this bit to 1 when Main Master assigns the Dynamic address during ENTDA or SETDASA mechanism. In I3C Slave Mode the Controller sets this bit to 1 when Main Master assigns the Dynamic address during ENTDA or SETDASA mechanism. Values: 0x0 (INVALID): Dynamic Address is invalid

Bits	Name	Memory Access	Description
			0x1 (VALID): Dynamic Address is valid Value After Reset: 0x0 Volatile: true

7.6.2.3 HW_CAPABILITY

Size: 32 bits

Offset: 0x0008

Bits	Name	Memory Access	Description
2:0	DEVICE_ROLE_CONFIG	RO	Reflects the IC_DEVICE_ROLE Configurable Parameter. Specifies the configured role of DWC_mipi_i3c controller 1: Master Only 2: Programmable Master-Slave 3: Secondary Master4: Slave Only Value After Reset: 0x3
3	HDR_DDR_EN	RO	Reflects the IC_SPEED_HDR_DDR Configurable Parameter. Specifies the Controllers capability to perform HDR-DDR transfers. 0: HDR-DDR not supported 1: HDR-DDR supported Value After Reset: 0x1
4	HDR_TS_EN	RO	Reflects the IC_SPEED_HDR_TS Configurable Parameter. Specifies the Controllers capability to perform HDR-TS transfers.0: HDR-TS not supported1: HDR-TS supported Value After Reset: 0x0
10:5	CLOCK_PERIOD	RO	Reflects the IC_CLK_PERIOD Configurable Parameter Value After Reset: 0x5



Bits	Name	Memory Access	Description
16:11	HDR_TX_CLOCK_PERIOD	RO	Reflects the IC_HDR_TX_CLK_PERIOD Configurable Parameter. Value After Reset: 0x28
17	DMA_EN	RO	Reflects the IC_HAS_DMA Configurable Parameter. Specifies whether controller is configured to have DMA handshaking interface. Value After Reset: 0x0
18	SLV_HJ_CAP	RO	Reflects the IC_SLV_HJ Configurable Parameter. Specifies slave's capability to initiate Hot-join request. Value After Reset: 0x1
19	SLV_IBI_CAP	RO	Reflects the IC_SLV_IBI Configurable Parameter. Specifies slave's capability to initiate slave interrupt requests. Value After Reset: 0x1
31:20	Reserved_20_31	RO	Reserved Field: Yes

7.6.2.4 COMMAND_QUEUE_PORT

Size: 32 bits

Offset: 0x000C

Bits	Name	Memory Access	Description
31:0	COMMAND	WO	32 bit command Value After Reset: 0x0

7.6.2.5 RESPONSE_QUEUE_PORT

Size: 32 bits

Offset: 0x0010



Bits	Name	Memory Access	Description
31:0	RESPONSE	RO	32 bit Response Value After Reset: 0x0

7.6.2.6 TX_DATA_PORT

Size: 32 bits

Offset: 0x0014

Bits	Name	Memory Access	Description
31:0	TX_DATA_PORT	WO	<p>Transmit Data Port</p> <p>The Transmit Data port is mapped to the Tx-Data Buffer. The transmit data should always be packed as 4-byte aligned data words and written to the Transmit Data Port register. If the Command length is not aligned to 4-bytes, then the additional bytes are ignored. The register is to provide a single bi-directional data port for both transmit and receive buffers.</p> <p>Therefore, writing into that port pushes data into transmit buffer and reading fetches data from receive buffer.</p> <p>Value After Reset: 0x0</p>



7.6.2.7 RX_DATA_PORT

Size: 32 bits

Offset: 0x0014

Bits	Name	Memory Access	Description
31:0	RX_DATA_PORT	RO	<p>Receive Data Port.</p> <p>The Receive data port is mapped to the Rx-Data Buffer. The Receive data is always packed in 4-byte aligned data words and stored in the Rx-Data Buffer. If the command length is not aligned to the 4-bytes, then the additional data bytes have to be ignored.</p> <p>Value After Reset: 0x0</p>

7.6.2.8 IBI_QUEUE_STATUS

Size: 32 bits

Offset: 0x0018

Bits	Name	Memory Access	Description
37:0	IID DATA_LENGTH	RO	<p>Interrupt ID (or IID)</p> <p>This indicates the highest priority pending interrupt which can be one of the following types specified in Values. For information on several levels into which the interrupt priorities are split into, see the 'Interrupts' section in the DW_apb_uart Databook.</p> <p>Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.</p> <p>Values:</p> <p>0x0 (MODEM_STATUS): modem status</p>



Bits	Name	Memory Access	Description
			<p>0x1 (NO_INTERRUPT_PENDING): no interrupt pending</p> <p>0x2 (THR_EMPTY): THR empty</p> <p>0x4 (RECEIVED_DATA_AVAILABLE): received data available</p> <p>0x6 (RECEIVER_LINE_STATUS): receiver line status</p> <p>0x7 (BUSY_DETECT): busy detect</p> <p>0xc (CHARACTER_TIMEOUT): character timeout</p> <p>In-Band Interrupt data length. This field represents the length of data received along with the IBI, in bytes. Value After Reset: 0x0</p>
5:4 15:8	RSVD_IIR_5to4 IBI_ID	RO	<p>Reserved</p> <p>IBI Identifier. The byte received after START which includes the address and the R/W bit. Device address and R/W bit in case of Slave Interrupt or Master Request. Hot-Join ID and R/W bit in case of Hot-Join IBI. Value After Reset: 0x0</p>
7:6 27:16	FIFOSE Reserved_16_27	RO	<p>FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.</p> <p>Values:</p> <p>0x0 (DISABLED): FIFOs are disabled</p> <p>0x3 (ENABLED): FIFOs are enabled</p> <p>Reserved Field: Yes</p>
31:828	RSVD_FCR_31to8 IBI_STS	RO	<p>Reserved</p> <p>IBI Received Status. Defines the master response for IBI received.4'b0xxx: Responded with ACK4'b1xxx: Responded with NACK Others: Reserved Value After Reset: 0x0</p>



7.6.2.9 QUEUE_THLD_CTRL

Size: 32 bits

Offset: 0x000C

Bits	Name	Memory Access	Description
7:0	CMD_EMPTY_BUF_THLD	RW	Command Buffer Empty Threshold Value. Controls the number of empty locations (or greater) in the Command Queue that trigger CMD_QUEUE_READY_STAT interrupt. The valid range is 0 to IC_CMD_BUF_DEPTH-1. The software programs only valid values. Value of N ranging from 1 to IC_CMD_BUF_DEPTH-1 sets the threshold to N empty locations and a value of 0 sets the threshold to indicate that the queue is completely empty. Value After Reset: 0x1
15:8	RESP_BUF_THLD	RW	Response Buffer Threshold Value. Controls the number of entries (or greater) in the Response Queue that trigger the RESP_READY_STAT_INTR interrupt. The valid range is 0 to IC_RESP_BUF_DEPTH-1. The software programs only valid values. A value of 0 sets the threshold for 1 entry, and a value of N sets the threshold for N+1 entries. Value After Reset: 0x1
23:16	Reserved_16_23	RO	Reserved Field: Yes
31:24	IBI_STATUS_THLD	RW	In-Band Interrupt Status Threshold Value. Every In Band Interrupt received (with or without Payload) by I3C controller generates an IBI status.



Bits	Name	Memory Access	Description
			<p>This field controls the number of IBI status entries (or greater) in the IBI queue that trigger the IBI_THLD_STAT interrupt. The valid range is 0 to IC_IBI_BUF_DEPTH-1. The software programs only valid values. A value of 0 sets the threshold for 1 entry, and a value of N sets the threshold for N+1 entries.</p> <p>NOTE: The valid value is only 0 if IBI with payload is selected in the configuration. Each IBI status entry can represent the complete (IBI payload byte size \leq 4*IBI_DATA_THLD) IBI payload or a segment (IBI payload byte size $>$ 4*IBI_DATA_THLD) of the IBI payload.</p> <p>Value After Reset: 0x1</p>

7.6.2.10 DATA_BUFFER_THLD_CTRL

Size: 32 bits

Offset: 0x0020

Bits	Name	Memory Access	Description
2:0	TX_EMPTY_BUF_THLD	RW	<p>Transmit Buffer Threshold Value</p> <p>This field controls the number of empty locations (or above) in the Transmit FIFO that trigger the TX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold is set to IC_TX_BUF_DEPTH.</p>



Bits	Name	Memory Access	Description
			The supported values for TX_BUF_THLD are 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 Value After Reset: 0x1
7:3	Reserved_3_7	RO	Reserved Field: Yes
10:8	RX_BUF_THLD	RW	Receive Buffer Threshold Value<ct:cfc:1:IC_MASTER_MODE==1> This field controls the number of entries (or above) in the Receive FIFO that trigger the RX_THLD_STAT interrupt. If the programmed value is greater than the buffer depth, then threshold is set to IC_RX_BUF_DEPTH. The supported values for RX_BUF_THLD are 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 Value After Reset: 0x1
15:11	Reserved_11_15	RO	Reserved Field: Yes
18:16	TX_START_THLD	RW	Transfer Start Threshold Value In master mode of operation when the controller is set up to initiate a write transfer, it waits until either one of the following conditions are met before it initiates the write transfer on the I3C Interface. Data length (as



Bits	Name	Memory Access	Description
			<p>specified in the command) number of locations are filled in the Transmit FIFOThreshold number of entries (or more) are available in the Transmit FIFO</p> <p>In slave mode of operation the slave controller ACK's a read request from Master only if either one of the following conditions are met:</p> <ul style="list-style-type: none"> Data length (as specified in the command) number of locations are filled in the Transmit FIFO Threshold number of entries (or more) are available in the Transmit FIFO <p>The supported values for TX_START_THLD are:</p> <ul style="list-style-type: none"> 000: 1 001: 4 010: 8 011: 16 100: 32 101: 64 <p>Value After Reset: 0x1</p>
23:19	Reserved_19_23	RO	Reserved Field: Yes
26:24	RX_START_THLD	RW	<p>Receive Start Threshold Value</p> <p>In master mode of operation when the controller is set up to initiate a read transfer, it waits until either one of the conditions are met before it initiates the read transfer on the I3C Interface.</p> <p>Data length (as specified in the command) number of locations are empty in the Receive FIFO.</p> <p>Threshold number of locations (or more) are empty in the Receive FIFO.</p> <p>In the slave mode of operation the</p>



Bits	Name	Memory Access	Description
			<p>slave controller ACK's a write request from Master only if threshold number of empty locations(or more) are available in its receive buffer.</p> <p>The supported values for RX_START_THLD are:</p> <ul style="list-style-type: none"> 000 – 1 001 – 4 010 – 8 011 – 16 100 – 32 101 – 64 <p>Value After Reset: 0x1</p>
31:27	Reserved_27_31	RO	Reserved Field: Yes

7.6.2.11 IBI_QUEUE_CTRL

Size: 32 bits

Offset: 0x0024

Bits	Name	Memory Access	Description
0	NOTIFY_HJ_REJECTED	RW	<p>Notify Rejected Hot-Join Control. This bit is used to suppress reporting to the application about Hot-Join request rejected (NACK and Auto Disable).</p> <p>0: Suppress passing the IBI Status to the IBI FIFO (hence not notifying the application) when a HJ Request is NACKed and auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL.</p> <p>1: Writes IBI Status to the IBI FIFO (hence notifying the application) when a HJ Request is NACKed and</p>



Bits	Name	Memory Access	Description
			auto-disabled based on the DEVICE_CTRL.HOT_JOIN_CTRL. Values:0x0 (DISABLED): Notify Hot-Join Rejected Disable0x1 (ENABLED): Notify Hot-Join Rejected Enable Value After Reset: 0x0
1	NOTIFY_MR_REJECTED	RW	Notify Rejected Master Request Control. This bit is used to suppress reporting to the application about Master request rejected. 0: Suppress passing the IBI Status to the IBI FIFO (hence not notifying the application) when a MR Request is NACKed and auto-disabled based on the IBI_MR_REQ_REJECT Register. 1: Writes IBI Status to the IBI FIFO (hence notifying the application) when a MR Request is NACKed and auto-disabled based on the IBI_MR_REQ_REJECT Register. Values: 0x0 (DISABLED): Notify Master Request Rejected Disable 0x1 (ENABLED): Notify Master Request Rejected Enable Value After Reset: 0x0
2	Reserved_2_2	RO	Reserved Field: Yes
3	NOTIFY_SIR_REJECTED	RW	Notify Rejected Slave Interrupt Request Control. This bit is used to suppress reporting to the application about SIR request rejected. 0: Suppress passing the IBI Status to the IBI FIFO (hence not notifying the application) when a Slave Interrupt



Bits	Name	Memory Access	Description
			<p>Request is NACKed and auto-disabled based on the IBI_SIR_REQ_REJECT Register.</p> <p>1: Writes IBI Status to the IBI FIFO (hence notifying the application) when a Slave Interrupt Request is NACKed and auto-disabled based on the IBI_SIR_REQ_REJECT Register.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Notify SIR Rejected Disable 0x1 (ENABLED): Notify SIR Rejected Enable <p>Value After Reset: 0x0</p>
31:4	Reserved_4_31	RO	Reserved Field: Yes

7.6.2.12 IBI_MR_REQ_REJECT

Size: 32 bits

Offset: 0x002C

Bits	Name	Memory Access	Description
31:0	MR_REQ_REJECT	RW	<p>In-band Master Request Reject.</p> <p>The control bits of this field determines if the controller ACK's incoming Master Request or NACKs and Disables it.</p> <p>A device specific policy can be established by appropriately programming this register.</p> <p>0: ACK Master Request</p> <p>1: NACK and send Directed DISEC CCC to disable the interrupting slave.</p> <p>Value After Reset: 0x0</p>



7.6.2.13 IBI_SIR_REQ_REJECT

Size: 32 bits

Offset: 0x0030

Bits	Name	Memory Access	Description
31:0	SIR_REQ_REJECT	RW	<p>In-band Slave Interrupt Request Reject The application of the DWC_mipi_i3c can decide whether to send ACK or NACK for a Slave Interrupt request received from any I3C device.</p> <p>A device-specific response control bit is provided to select the response option. Master ACK's/NACK's the Slave Interrupt Request based on programming of control bit, corresponding to the interrupting device.</p> <p>0 - ACK the SIR Request 1 - NACK and send directed auto disable CCC</p> <p>Value After Reset: 0x0</p>

7.6.2.14 RESET_CTRL

Size: 32 bits

Offset: 0x0034

Bits	Name	Memory Access	Description
7:0	SOFT_RST	RW	<p>Exists: (SIR_LP_RX == 1) and (SIR_MODE == 1).</p> <p>This register makes up the lower 8-bits of a 16-bit, read/write, Low Power Divisor Latch register that contains the baud rate divisor for the UART which must give a baud rate of 115.2K.</p> <p>This is required for SIR Low Power (minimum pulse width) detection at the receiver. The output low power baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the</p>



Bits	Name	Memory Access	Description
			<p>value of the baud rate divisor, as follows: Low power baud rate = (serial clock freq) / (16 * divisor) Therefore a divisor must be selected to give a baud rate of 115.2K. Value After Reset: 0x0 Exists: Always Core Software Reset. Write 1'b1 to this bit to exercise software reset. This resets all Buffers - Receive, Transmit, Command, and Response. This bit is cleared automatically once the core reset is complete. Value After Reset: 0x0 Volatile: true</p>
31:8 1	RSVD_LPDL_31to8 CMD_QUEUE_RST	RO RW	<p>Reserved Command Queue Software Reset. Write 1'b1 to this bit to exercise Command Queue reset. This bit is cleared automatically once the Command Queue reset is complete. Value After Reset: 0x0 Volatile: true</p>
2	RESP_QUEUE_RST	RW	<p>Response Queue Software Reset. Write 1'b1 to this bit to exercise Response Queue reset. This bit is cleared automatically once the Response Queue reset is complete. Value After Reset: 0x0 Volatile: true</p>
3	TX_FIFO_RST	RW	<p>Transmit Buffer Software Reset. Write 1'b1 to this bit to exercise Transmit Buffer reset. This bit is cleared automatically once the Transmit Buffer reset is completed. Value After Reset: 0x0 Volatile: true</p>
4	RX_FIFO_RST	RW	<p>Receive Buffer Software Reset. Write 1'b1 to this bit to exercise Receive Buffer reset. This bit is cleared</p>

Bits	Name	Memory Access	Description
			automatically once the Receive buffer reset is completed. Value After Reset: 0x0 Volatile: true
5	IBI_QUEUE_RST	RW	IBI Queue Software Reset. This bit is only used in master mode of operation. Write 1'b1 to this bit to exercise IBI Queue reset. This bit is cleared automatically once the IBI Queue reset is completed. Value After Reset: 0x0 Volatile: true
28:6	Reserved_6_28	RO	Reserved Field: Yes
30:29	BUS_RESET_TYPE	RW	Bus Reset type of bus reset triggered by BUS_RESET field. Values: 2'b00: EXIT: Exit Pattern 2'b11: SCL_LOW_RESET Pattern Others: Reserved Value After Reset: 0x0 Volatile: true
31	BUS_RESET	RW	Bus Reset. This bit is only used in master mode of operation. Write 1'b1 to this bit to exercise Bus Reset Pattern Generation based on Bus Reset Type selection. This bit is cleared automatically once the Bus Reset Pattern Generation is completed. Value After Reset: 0x0 Volatile: true



7.6.2.15 SLV_EVENT_STATUS

Size: 32 bits

Offset: 0x0038

Bits	Name	Memory Access	Description
0	SIR_EN	RO	<p>Slave Interrupt Request Enable.</p> <p>In Slave mode of operation, this bit reflects whether the controller can initiate the SIR on the I3C bus or not. Usually, this bit is set or cleared by the I3C Master through ENEC or DISEC CCC.</p> <p>Value After Reset: 0x1</p>
1	MR_EN	RO	<p>Master Request Enable. In Slave mode of operation, this bit reflects whether the controller can initiate the Master Request on the I3C bus or not. Usually, this bit is set or cleared by the I3C Master through ENEC or DISEC CCC.</p> <p>Value After Reset: 0x1</p> <p>Volatile: true</p>
2	Reserved_2_2	RO	Reserved Field: Yes
3	HJ_EN	RW	<p>Hot-Join Interrupt Enable</p> <p>This bit reflects whether the Hot-Join Request Interrupts are allowed on the I3C bus or not. The Slave application can choose to Disable HJ Capability of the Slave Controller (if selected) by setting this field to 0 before 'Enabling' the Controller. When done so, the Slave does not initiate Hot Join and takes part in Address Assignment without initiating Hot Join. If this field is NOT set to 0 by slave application, it can be set or cleared by the I3C Master through ENEC or DISEC CCCs. Once Disabled by software, CCCs do not have any effect on this field.</p> <p>Value After Reset: 0x1</p>

Bits	Name	Memory Access	Description
			Volatile: true
5:4	ACTIVITY_STATE	RO	<p>Activity State Status.</p> <p>ENTAS0 – 00</p> <p>ENTAS1 – 01</p> <p>ENTAS2 – 10</p> <p>ENTAS3 – 11</p> <p>This bit reflects the Activity State of slave set by the Master.</p> <p>Value After Reset: 0x0</p>
6	MRL_UPDATED	WC	<p>MRL Updated Status.</p> <p>This bit indicates a SETMRL CCC is received by the slave. The updated MRL value can be read from SLV_MAX_LEN register. This status can be cleared by writing 1'b1 to this field after reading the updated MRL.</p> <p>Value After Reset: 0x0</p>
7	MWL_UPDATED	WC	<p>MWL Updated Status.</p> <p>This bit indicates a SETMWL CCC is received by the slave. The updated MWL value can be read from SLV_MAX_LEN register. This status can be cleared by writing 1'b1 to this field after reading the updated MWL.</p> <p>Value After Reset: 0x0</p>
31:8	Reserved_8_31	RO	Reserved Field: Yes

7.6.2.16 INTR_STATUS

Size: 32 bits

Offset: 0x003C



Bits	Name	Memory Access	Description
0	TX_THLD_STS	RO	<p>Transmit Buffer Threshold Status This interrupt is generated when the number of empty locations in transmit buffer is greater than or equal to threshold value specified by TX_EMPTY_BUF_THLD field in DATA_BUFFER_THLD_CTRL register. This interrupt is cleared automatically when number of empty locations in transmit buffer is less than threshold value specified.</p> <p>Value After Reset: 0x0 Volatile: true</p>
1	RX_THLD_STS	RO	<p>Receive Buffer Threshold Status. This interrupt is generated when number of entries in receive buffer is greater than or equal to threshold value specified by RX_BUF_THLD field in DATA_BUFFER_THLD_CTRL register. This interrupt is cleared automatically when number of entries in receive buffer is less than threshold value specified.</p> <p>Value After Reset: 0x0 Volatile: true</p>
2	IBI_THLD_STS	RO	<p>IBI Buffer Threshold Status. This field is only used in master mode of operation This interrupt is generated when number of entries in IBI buffer is greater than or equal to threshold value specified by IBI_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt is cleared automatically when number of</p>



Bits	Name	Memory Access	Description
			entries in IBI buffer is less than threshold value specified. Value After Reset: 0x0 Volatile: true
3	CMD_QUEUE_READY_STS	RO	Command Queue Ready. This interrupt is generated when number of empty locations in command queue is greater than or equal to threshold value specified by CMD_EMPTY_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt is cleared automatically when number of empty locations in command buffer is less than threshold value specified. Value After Reset: 0x0 Volatile: true
4	RESP_READY_STS	RO	Response Queue Ready Status. This interrupt is generated when number of entries in response queue is greater than or equal to threshold value specified by RESP_BUF_THLD field in QUEUE_THLD_CTRL register. This interrupt is cleared automatically when number of entries in response buffer is less than threshold value specified. Value After Reset: 0x0 Volatile: true
5	TRANSFER_ABORT_STS	WC	Transfer Abort Status. This field is used only in master mode of operation. This interrupt is generated if transfer is aborted. This interrupt can be cleared by writing 1'b1. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Volatile: true
6	CCC_UPDATED_STS	WC	<p>CCC Table Updated Status. This field is used only in slave mode of operation. This interrupt is generated if any of the CCC registers are updated by I3C Master through CCC commands. This interrupt can be cleared by writing 1'b1.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
7	Reserved_7_7	RO	Reserved Field: Yes
8	DYN_ADDR_ASSGN_STS	WC	<p>Dynamic Address Assigned Status. This field is used only in slave mode of operation. This interrupt is generated if the device's Dynamic Address is assigned through SETDASA or ENTDAAC CCC. This bit can be cleared by writing 1'b1.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
9	TRANSFER_ERR_STS	WC	<p>Transfer Error Status. This interrupt is generated if any error occurs during transfer. The error type is specified in the response packet associated with the command (in ERR_STATUS field of RESPONSE_QUEUE_PORT register). This bit can be cleared by writing 1'b1.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>



Bits	Name	Memory Access	Description
10	DEFSLV_STS	WC	Define Slave CCC Received Status. This interrupt is generated if DEFSLV CCC is received. This bit can be cleared by writing 1'b1. Value After Reset: 0x0 Volatile: true
11	READ_REQ_RECV_STS	WC	Read Request Received. This field is used only in slave mode of operation. Read Request received from the current master when CMDQ is empty. This bit can be cleared by writing 1'b1. Value After Reset: 0x0 Volatile: true
12	IBI_UPDATED_STS	WC	IBI status is updated. This field is used only in slave mode of operation. It indicates that the IBI request initiated through SIR request register is addressed and status is updated. Value After Reset: 0x0 Volatile: true
13	BUSOWNER_UPDATED_STS	WC	This interrupt is set when the role of the controller changes from being a Master to Slave or vice versa. This bit can be cleared by writing 1'b1. Value After Reset: 0x0 Volatile: true
14	Reserved_14_14	RO	Reserved Field: Yes
15	BUS_RESET_DONE_STS	WC	Bus Reset Pattern Generation Done Status. This field is used only in Master mode of operation. This interrupt is generated when the SCL Low



Bits	Name	Memory Access	Description
			Timeout Bus Reset Pattern Generation is completed. This bit can be cleared by writing 1'b1. Value After Reset: 0x0 Volatile: true
31:16	Reserved_16_31	RO	Reserved Field: Yes

7.6.2.17 INTR_STATUS_EN

Size: 32 bits

Offset: 0x0040

Bits	Name	Memory Access	Description
0	TX_THLD_STS_EN	RW	Transmit Buffer Threshold Status Enable. Value After Reset: 0x0
1	RX_THLD_STS_EN	RW	Receive Buffer Threshold Status Enable Value After Reset: 0x0
2	IBI_THLD_STS_EN	RW	IBI Buffer Threshold Status Enable. This field is used only in master mode of operation. Value After Reset: 0x0
3	CMD_QUEUE_READY_STS_EN	RW	Command Queue Ready Status Enable Value After Reset: 0x0
4	RESP_READY_STS_EN	RW	Response Queue Ready Status Enable Value After Reset: 0x0
5	TRANSFER_ABORT_STS_EN	RW	Transfer Abort Status Enable. This field is used only in master mode of operation. Value After Reset: 0x0



Bits	Name	Memory Access	Description
6	CCC_UPDATED_STS_EN	RW	CCC Table Updated Status Enable. This field is used in slave mode of operation. Value After Reset: 0x0
7	Reserved_7_7	RO	Reserved Field: Yes
8	DYN_ADDR_ASSGN_STS_EN	RW	Dynamic Address Assigned Status Enable This field is used in slave mode of operation. Value After Reset: 0x0
9	TRANSFER_ERR_STS_EN	RW	Transfer Error Status Enable Value After Reset: 0x0
10	DEFSLV_STS_EN	RW	Define Slave CCC Received Status Enable Value After Reset: 0x0
11	READ_REQ_RECV_STS_EN	RW	Read Request Received Status Enable This field is used in slave mode of operation. Value After Reset: 0x0
12	IBI_UPDATED_STS_EN	RW	IBI Updated Status Enable This field is used in slave mode of operation. Value After Reset: 0x0
13	BUSOWNER_UPDATED_STS_EN	RW	Bus owner Updated Status Enable Value After Reset: 0x0
14	Reserved_14_14	RO	Reserved Field: Yes
15	BUS_RESET_DONE_STS_EN	RW	Bus Reset Pattern Generation Done Status Enable. This field is used only in Master mode of operation. Value After Reset: 0x0



Bits	Name	Memory Access	Description
31:16	Reserved_16_31	RO	Reserved Field: Yes



7.6.2.18 INTR_SIGNAL_EN

Size: 32 bits

Offset: 0x0044

Bits	Name	Memory Access	Description
0	TX_THLD_SIGNAL_EN	RW	Transmit Buffer Threshold Signal Enable Value After Reset: 0x0
1	RX_THLD_SIGNAL_EN	RW	Receive Buffer Threshold Signal Enable Value After Reset: 0x0
2	IBI_THLD_SIGNAL_EN	RW	IBI Buffer Threshold Signal Enable This field is used in master mode of operation. Value After Reset: 0x0
3	CMD_QUEUE_READY_SIGNAL_EN	RW	Command Queue Ready Signal Enable Value After Reset: 0x0
4	RESP_READY_SIGNAL_EN	RW	Response Queue Ready Signal Enable Value After Reset: 0x0
5	TRANSFER_ABORT_SIGNAL_EN	RW	Transfer Abort Signal Enable This field is used in master mode of operation. Value After Reset: 0x0
6	CCC_UPDATED_SIGNAL_EN	RW	CCC Table Updated Signal Enable This field is used in slave mode of operation. Value After Reset: 0x0
7	Reserved_7_7	RO	Reserved Field: Yes
8	DYN_ADDR_ASSGN_SIGNAL_EN	RW	Dynamic Address Assigned Signal Enable



Bits	Name	Memory Access	Description
			This field is used in slave mode of operation. Value After Reset: 0x0
9	TRANSFER_ERR_SIGNAL_EN	RW	Transfer Error Signal Enable Value After Reset: 0x0
10	DEFSLV_SIGNAL_EN	RW	Define Slave CCC Received Signal Enable Value After Reset: 0x0
11	READ_REQ_RECV_SIGNAL_EN	RW	Read Request Received Signal Enable This field is used in slave mode of operation. Value After Reset: 0x0
12	IBI_UPDATED_SIGNAL_EN	RW	IBI Updated Signal Enable This field is used in slave mode of operation. Value After Reset: 0x0
13	BUSOWNER_UPDATED_SIGNAL_EN	RW	Bus owner Updated Signal Enable Value After Reset: 0x0
14	Reserved_14_14	RO	Reserved Field: Yes
15	BUS_RESET_DONE_SIGNAL_EN	RW	Bus Reset Pattern Generation Done Signal Enable. This field is used only in Master mode of operation. Value After Reset: 0x0
31:16	Reserved_16_31	RO	Reserved Field: Yes

7.6.2.19 INTR_FORCE

Size: 32 bits

Offset: 0x0048



Bits	Name	Memory Access	Description
0	TX_THLD_FORCE_EN	WO	Transmit Buffer Threshold Force Enable Value After Reset: 0x0
1	RX_THLD_FORCE_EN	WO	Receive Buffer Threshold Force Enable Value After Reset: 0x0
2	IBI_THLD_FORCE_EN	WO	IBI Buffer Threshold Force Enable This field is used in master mode of operation. Value After Reset: 0x0
3	CMD_QUEUE_READY_FORCE_EN	WO	Command Queue Ready Force Enable Value After Reset: 0x0
4	RESP_READY_FORCE_EN	WO	Response Queue Ready Force Enable Value After Reset: 0x0
5	TRANSFER_ABORT_FORCE_EN	WO	Transfer Abort Force Enable This field is used in master mode of operation. Value After Reset: 0x0
6	CCC_UPDATED_FORCE_EN	WO	CCC Table Updated Force Enable This field is used in slave mode of operation. Value After Reset: 0x0
7	Reserved_7_7	RO	Reserved Field: Yes
8	DYN_ADDR_ASSGN_FORCE_EN	WO	Dynamic Address Assigned Force Enable This field is used in slave mode of operation. Value After Reset: 0x0



Bits	Name	Memory Access	Description
9	TRANSFER_ERR_FORCE_EN	WO	Transfer Error Force Enable Value After Reset: 0x0
10	DEFSLV_FORCE_EN	WO	Define Slave CCC Received Force Enable Value After Reset: 0x0
11	READ_REQ_FORCE_EN	WO	Read Request Received Force Enable This field is used in slave mode of operation. Value After Reset: 0x0
12	IBI_UPDATED_FORCE_EN	WO	IBI Updated Force Enable This field is used in slave mode of operation. Value After Reset: 0x0
13	BUSOWNER_UPDATED_FORCE_EN	WO	Bus owner Updated Force Enable Value After Reset: 0x0
14	Reserved_14_14	RO	Reserved Field: Yes
15	BUS_RESET_DONE_FORCE_EN	WO	Bus Reset Pattern Generation Done Force Enable. This field is used only in Master mode of operation. Value After Reset: 0x0
31:16	Reserved_16_31	RO	Reserved Field: Yes



7.6.2.20 QUEUE_STATUS_LEVEL

Size: 32 bits

Offset: 0x004C

Bits	Name	Memory Access	Description
7:0	CMD_QUEUE_EMPTY_LOC	RO	Command Queue Empty Locations. Contains the number of empty locations in the command Buffer. Value After Reset: 0x10
15:8	RESP_BUF_BLR	RO	Response Buffer Level Value. Contains the number of valid data entries in the response Buffer. Value After Reset: 0x0
23:16	IBI_BUF_BLR	RO	IBI Buffer Level Value. When IC_HAS_IBI_DATA =0, Contains the number of Valid IBI Status entries in the IBI Buffer. When IC_HAS_IBI_DATA=1, Contains the number of valid IBI Data entries in the IBI Data Buffer. This field is used in master mode of operation. Value After Reset: 0x0
28:24	IBI_STS_CNT	RO	IBI Buffer Status Count. When IC_HAS_IBI_DATA =0, this field is reserved and always returns 0. When IC_HAS_IBI_DATA=1, Contains the number of valid IBI Status entries in the IBI Status Buffer. This field is used in master mode of operation. Value After Reset: 0x0
31:29	Reserved_29_31	RO	Reserved Field: Yes



7.6.2.21 DATA_BUFFER_STATUS_LEVEL

Size: 32 bits

Offset: 0x0050

Bits	Name	Memory Access	Description
7:0	TX_BUF_EMPTY_LOC	RO	Transmit Buffer Empty Level Value. Contains the number of empty locations in the transmit Buffer. Value After Reset: 0x40
15:8	Reserved_8_15	RO	Reserved Field: Yes
23:16	RX_BUF_BLR	RO	Receive Buffer Level Value. Contains the number of valid data entries in the receive Buffer. Value After Reset: 0x0
31:24	Reserved_24_31	RO	Reserved Field: Yes

7.6.2.22 PRESENT_STATE

Size: 32 bits

Offset:0x0054

Bits	Name	Memory Access	Description
0	SCL_LINE_SIGNAL_LEVEL	RO	This bit is used to check the SCL line level to recover from errors and for debugging. This bit reflects the value of synchronized scl_in_a signal. This is valid in Master mode only Value After Reset: 0x1 Volatile: true
1	SDA_LINE_SIGNAL_LEVEL	RO	This bit is used to check the SDA line level to recover from errors and for debugging. This bit reflects the value of synchronized sda_in_a signal. This is valid in Master mode only.



Bits	Name	Memory Access	Description
			Value After Reset: 0x1 Volatile: true
2	CURRENT_MASTER	RO	This Bit is used to check whether the Master is Current Master or not. The Current Master is the Master that owns the SCL line. If this bit is set to 0, the Master is not Current Master and requires to request and the ownership before initiating any transfer on the line. If this bit is set to 1, the Master is the Current Master and can initiate the transfers on the line. 0: Master is not Current Master 1: Master is Current Master Values: 0x0 (NOT_BUS_OWNER): Master is not a Current Master 0x1 (BUS_OWNER): Master is Current Master Value After Reset: 0x0 Volatile: true
7:3	Reserved_3_7	RO	Reserved Field: Yes
13:8	CM_TFR_STS	RO	Transfer Type Status Indicates the type of transfer currently executing by the DWC_mipi_i3c controller. In Master mode of operation: 6'h0: IDLE (Controller is in Idle state, waiting for commands from application or Slave initiated In-band Interrupt) 6'h1: Broadcast CCC Write Transfer. 6'h2: Directed CCC Write Transfer. 6'h3: Directed CCC Read Transfer. 6'h4: ENTDAA Address Assignment Transfer.



Bits	Name	Memory Access	Description
			<p>6'h5: SETDASA Address Assignment Transfer.</p> <p>6'h6: Private I3C SDR Write Transfer.</p> <p>6'h7: Private I3C SDR Read Transfer.</p> <p>6'h8: Private I2C SDR Write Transfer.</p> <p>6'h9: Private I2C SDR Read Transfer.</p> <p>6'hA: Private HDR Ternary Symbol(TS) Write Transfer.</p> <p>6'hB: Private HDR Ternary Symbol(TS) Read Transfer.</p> <p>6'hC: Private HDR Double-Data Rate(DDR) Write Transfer.</p> <p>6'hD: Private HDR Double-Data Rate(DDR) Read Transfer.</p> <p>6'hE: Servicing In-Band Interrupt Transfer.</p> <p>6'hF: Halt state (Controller is in Halt State, waiting for the application to resume through DEVICE_CTRL Register)</p> <p>In Slave mode of operation:</p> <p>4'h0: IDLE (Controller is in Idle state)</p> <p>4'h1: Hot-Join transfer state</p> <p>4'h2: IBI transfer state</p> <p>4'h3: Master write transfer ongoing</p> <p>4'h4: Read data prefetch state</p> <p>4'h5: Master read transfer ongoing</p> <p>4'h6: Slave controller in Halt State waiting for resume from application</p> <p>Value After Reset: 0x0</p>
15:14	Reserved_14_15	RO	Reserved Field: Yes
21:16	CM_TFR_ST_STS	RO	Current Master Transfer State Status. Indicates the state of current transfer currently executing by the DWC_mipi_i3c controller. This is valid in Master mode only.



Bits	Name	Memory Access	Description
			<p>6'h0: IDLE (Controller is Idle state, waiting for commands from application or Slave initiated In-band Interrupt)</p> <p>6'h1: START Generation State.</p> <p>6'h2: RESTART Generation State.</p> <p>6'h3: STOP Generation State.</p> <p>6'h4: START Hold Generation for the Slave Initiated START State.</p> <p>6'h5: Broadcast Write Address Header(7'h7E,W) Generation State.</p> <p>6'h6: Broadcast Read Address Header(7'h7E,R) Generation State.</p> <p>6'h7: Dynamic Address Assignment State.</p> <p>6'h8: Slave Address Generation State.</p> <p>6'hB: CCC Byte Generation State.</p> <p>6'hc: HDR Command Generation State.</p> <p>6'hD: Write Data Transfer State.</p> <p>6'hE: Read Data Transfer State.</p> <p>6'hF: In-Band Interrupt(SIR) Read Data State.</p> <p>6'h10: In-Band Interrupt Auto-Disable State</p> <p>6'h11: HDR-DDR CRC Data Generation/Receive State.</p> <p>6'h12: Clock Extension State.</p> <p>6'h13: Halt State.</p> <p>Value After Reset: 0x0</p>
23:22	Reserved_22_23	RO	Reserved Field: Yes
27:24	CMD_TID	RO	<p>This field reflects the Transaction-ID of the current executing command.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
28	MASTER_IDLE	RO	<p>This field reflects whether the Master Controller is in Idle state or not. This bit is set when all the Queues(Command , Response, IBI) and Buffers(Transmit and Receive) are empty along with the Master State machine is in Idle state.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (MST_NOT_IDLE): Master Controller is not in IDLE State 0x1 (MST_IDLE): Master Controller is in IDLE State. <p>Value After Reset: 0x1 Volatile: true</p>
31:29	Reserved_29_31	RO	Reserved Field: Yes

7.6.2.23 CCC_DEVICE_STATUS

Size: 32 bits

Offset: 0x0058

Bits	Name	Memory Access	Description
3:0	PENDING_INTR	RO	<p>Pending Interrupt This field reflects the value driven on pending_int input port. Value After Reset: 0x0 Volatile: true</p>
4	Reserved_4_4	RO	Reserved Field: Yes
5	PROTOCOL_ERR	RO	<p>Protocol Error This bit is set when the slave controller encounters a Parity/CRC error during write data transfer. Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
			Volatile: true
7:6	ACTIVITY_MODE	RO	Activity Mode This field reflects the input port signal act_mode. Value After Reset: 0x0 Volatile: true
8	UNDERFLOW_ERR	RO	Underflow error Under Flow Error during private master read transfer. This bit is set if slave controller terminates a read transfer because of unavailability of data in the transmit buffer. This is cleared only after master reads the Device Status through GETSTATUS CCC. Value After Reset: 0x0 Volatile: true
9	SLAVE_BUSY	RO	Slave Busy This bit is set if any change is made by the current master in to MRL register or occurrence of any error. It is cleared after slave application resumes the slave operation by writing 1'b1 in RESUME field of Device Control Register. Value After Reset: 0x0 Volatile: true
10	OVERFLOW_ERR	RO	Overflow Error Overflow error condition detected during master write transfer. This is cleared only after master reads the Device Status through GETSTATUS CCC. Value After Reset: 0x0 Volatile: true
11	DATA_NOT_READY	RO	Data not ready This bit is set when private read request from Master is NACKED because of any

Bits	Name	Memory Access	Description
			<p>of the following conditions Command FIFO Empty. Transmit FIFO threshold is not met. Response FIFO Full. This is cleared when the Master issues GET_STATUS CCC or upon successful completion of the subsequent read transfer.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
12	BUFFER_NOT_AVAIL	RO	<p>Buffer not available</p> <p>This bit is set when private write request from Master is NACKED because of RX buffer not having RX_BUF_THLD number of empty locations or Response buffer is full. In SDR mode of operation this is cleared when the Master issues GET_STATUS CCC or upon space becoming available in the buffer and the successful completion of the next write transfer. In HDR mode of operation it is cleared only when Master issues GET_STATUS CCC.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
13	FRAME_ERROR	RO	<p>Frame Error This bit is set when private write request from Master has frame error in HDR-DDR/HDR-TSP/TSL mode.</p> <p>This is cleared only after Master reads the device status through GETSTATUS_CCC.</p> <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
31:14	Reserved_14_31	RO	Reserved Field: Yes



7.6.2.24 DEVICE_ADDR_TABLE_POINTER

Size: 32 bits

Offset: 0x005C

Bits	Name	Memory Access	Description
15:0	P_DEV_ADDR_TABLE_START_ADDR	RO	Start Address of Device Address Table. Value After Reset: 0x2c0
31:16	DEV_ADDR_TABLE_DEPTH	RO	Depth of Device Address Table Value After Reset: 0xb

7.6.2.25 DEV_CHAR_TABLE_POINTER

Size: 32 bits

Offset: 0x0060

Bits	Name	Memory Access	Description
11:0	P_DEV_CHAR_TABLE_START_ADDR	RO	Start Address of Device Characteristics Table. Value After Reset: 0x200
18:12	DEV_CHAR_TABLE_DEPTH	RO	Depth of Device Characteristics Table Value After Reset: 0x2c
22:19	PRESENT_DEV_CHAR_TABLE_INDX	RW	Current index of Device Characteristics Table. This field returns the current location of Device Characteristics Table index. Initially, this index points to 0. Once the complete characteristics information of a Slave device is written into Device Characteristics Table during ENTDA, this index increments by 1. The first winning device information is stored in

Bits	Name	Memory Access	Description
			<p>Device Characteristics Table index 0, the second winning device information in index 1, and so on. If required, this index can be used to override the location, where characteristic information of Slave devices on the I3C bus are written during ENTDAA. Hence, this field is useful only if the device is Current Master. During DEFSLV CCC, the index always starts from 0. In Non-current Master, this field is always read-only.</p> <p>Value After Reset: 0x0</p>
31:23	Reserved_23_31	RO	Reserved Field: Yes

7.6.2.26 VENDOR_SPECIFIC_REG_POINTER

Size: 32 bits

Offset: 0x006C

Bits	Name	Memory Access	Description
15:0	P_VENDOR_REG_START_ADDR	RO	<p>Start Address of Vendor specific registers.</p> <p>Value After Reset: 0xb0</p>
31:16	Reserved_16_31	RO	Reserved Field: Yes



7.6.2.27 SLV_MIPI_ID_VALUE

Size: 32 bits

Offset: 0x0070

Bits	Name	Memory Access	Description
0	SLV_PROV_ID_SEL	RW	Specifies the Provisional ID Type Selector (PID[32]). (1'b1: Random Value, 1'b0: Vendor Fixed Value) Value After Reset: 0x0
15:1	SLV_MIPI_MFG_ID	RW	Specifies the MIPI Manufacturer ID. (PID[47:33]). Value After Reset: 0x0
31:16	Reserved_16_31	RO	Reserved Field: Yes

7.6.2.28 SLV_PID_VALUE

Size: 32 bits

Offset: 0x0074

Bits	Name	Memory Access	Description
11:0	SLV_PID_DCR	RW	Specifies the additional 12-bit ID of DWC_mipi_i3c device (PID[11:0]). After reset, assigned to external input slv_pid Value After Reset: 0x0
15:12	SLV_INST_ID	RW	This field is used to program the instance ID of the Slave. The reset value of this register is taken from input port 'inst_id'. Value After Reset: 0x0
31:16	SLV_PART_ID	RW	Specifies the additional 12-bit ID of DWC_mipi_i3c device (PID[11:0]). Value After Reset: 0x0

7.6.2.29 SLV_CHAR_CTRL

Size: 32 bits



Offset: 0x0078

Bits	Name	Memory Access	Description
0	MAX_DATA_SPEED_LIMIT	RW	<p>Max Data Speed Limitation field in Bus Characteristic Register (BCR[0]). Specifies whether or not DWC_mipi_i3c has maximum data speed limitation. If this bit is set to 0, controller NACK's the GETMXDS CCC sent by Master. If this bit is set to 1, controller returns the data in MAX_DATA_SPEED and MAX_READ_TURNAROUND register in response the GETMXDS CCC sent by Master. The field is Reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset.</p> <p>Value After Reset: 0x0</p>
1	IBI_REQUEST_CAPABLE	RO	<p>IBI Request Capable field in Bus Characteristic Register (BCR[1]). This bit is set if configuration parameter IC_SLV_IBI is set to 1. Value After Reset: 0x1</p>
2	IBI_PAYLOAD	RO	<p>IBI Payload field in Bus Characteristic Register (BCR[2]). This bit is set if configuration parameter IC_SLV_IBI_DATA is set to 1. Value After Reset: 0x0</p>
3	OFFLINE_CAPABLE	RO	<p>Offline Capable field in Bus Characteristic Register (BCR[3]). This bit is set if configuration parameter IC_SLV_OFFLINE_CAP is set to 1. Value After Reset: 0x0</p>
4	BRIDGE_IDENTIFIER	RO	<p>Bridge Identifier field in Bus Characteristic Register (BCR[4]). This bit is set if configuration parameter IC_SLV_BRIDGE is set to 1. Value After Reset: 0x0</p>

Bits	Name	Memory Access	Description
5	HDR_CAPABLE	RW	SDR Only or SDR and HDR Capable field in Bus Characteristic Register (BCR[5]). This bit is set if any of the configuration parameter IC_SPEED_HDR_TS or IC_SPEED_HDR_DDR is set to 1. It is to be noted that the programming this field to 0 does not Disable the HDR Feature itself. This bit can be modified by the application if it does not want to advertise Slaves HDR capability to Master. The field is Reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset. Value After Reset: 0x1
7:6	DEVICE_ROLE	RW	Device Role field in Bus Characteristic Register (BCR[7:6]). This field is set to 1 by default if configuration parameter IC_DEVICE_ROLE is set to 3(Secondary Master). The application is not expected to change the role once configured. But if the application chooses to operate the secondary master configuration (IC_DEVICE_ROLE==3) as "Slave Only" through programming, then the Device Role can be overwritten as Slave (BCR[7:6] = 2'b00). The field is Reset to its default value upon HW/SW Reset. SW must program the values again after issuing reset. Value After Reset: 0x1
15:8	DCR	RW	I3C Device Characteristic Value. Value After Reset: 0x0



Bits	Name	Memory Access	Description
23:16	HDR_CAP	RO	I3C Device HDR Capability Register Value. HDR_CAP[2] - HDR Mode 2 (IC_SPEED_HDR_TS) HDR_CAP[1] - HDR Mode 1 (IC_SPEED_HDR_TS) HDR_CAP[1] - HDR Mode 0 (IC_SPEED_HDR_DDR) Others – Reserved Value After Reset: 0x1
31:24	Reserved_24_31	RO	Reserved Field: Yes

7.6.2.30 SLV_MAX_LEN

Size: 32 bits

Offset: 0x007C

Bits	Name	Memory Access	Description
15:0	MWL	RO	I3C Device Max Write Length Value After Reset: 0xffff
31:16	MRL	RO	I3C Device Max Read Length. Value After Reset: 0xffff

7.6.2.31 MAX_READ_TURNAROUND

Size: 32 bits

Offset: 0x0080

Bits	Name	Memory Access	Description
23:0	MXDS_MAX_RD_TURN	RO	Specifies the maximum read turnaround time (in microseconds (us)) of DWC_mipi_i3c Slave. Value After Reset: 0x64



Bits	Name	Memory Access	Description
31:24	Reserved_24_31	RO	Reserved Field: Yes

7.6.2.32 MAX_DATA_SPEED

Size: 32 bits

Offset: 0x0084

Bits	Name	Memory Access	Description
2:0	MXDS_MAX_WR_SPEED	RW	Specifies the Maximum Sustained Data Rate for non-CCC messages sent by Master Device to DWC_mipi_i3c Slave device 0: 12.5MHz 1: 8MHz 2: 6MHz 3: 4MHz 4: 2MHz 5-7: Reserved/User Defined Value After Reset: 0x0
7:3	Reserved_3_7	RO	Reserved Field: Yes
10:8	MXDS_MAX_RD_SPEED	RW	Specifies the Maximum Sustained Data Rate for non-CCC messages sent by DWC_mipi_i3c Slave Device to Master Device 0: 12.5MHz 1: 8MHz 2: 6MHz 3: 4MHz 4: 2MHz 5-7: Reserved/User Defined Value After Reset: 0x0
15:11	Reserved_11_15	RO	Reserved Field: Yes



18:16	MXDS_CLK_DATA_TURN	RW	Specifies the clock to data turnaround time (Tsco parameter) of DWC_mipi_i3c Slave device 0: 8ns 1: 9ns 2: 10ns 3: 11ns 4: 12ns 5-7: Reserved/user Defined Value After Reset: 0x0
31:19	Reserved_19_31	RO	Reserved Field: Yes

7.6.2.33 SLV_INTR_REQ

Size: 32 bits

Offset: 0x008C

Bits	Name	Memory Access	Description
0	SIR	RW	Slave Interrupt Request When set, the slave controller attempts to issue the SIR on the I3C bus. Once issued and when the current master accepts (ACK) or if the controller is unable to issue the SIR, then the controller clears this bit automatically and updates the IBI_STS field. If the NACK response is received for the SIR, the controller reattempts the SIR upon detecting the next START condition from the master or after the Bus Available Time. Once set, the application cannot clear this bit. Value After Reset: 0x0 Volatile: true
2:1	SIR_CTRL	RW	Slave Interrupt Request Control 2'b00: Send the Assigned Dynamic Address 2'b01: Reserved 2'b10: Reserved



Bits	Name	Memory Access	Description
			2'b11: Reserved Value After Reset: 0x0
3	MR	RW	<p>Master Request</p> <p>When set, the controller attempts to issue the MR on the I3C bus. Once issued and when the current master accepts (ACK) or if the controller is unable to issue the MR, then the controller clears this bit automatically and updates the IBI_STS field. If NACK response is received for the MR, the controller reattempts the MR upon detecting the next START condition from the master or after the Bus Available time. This bit is available only in the secondary master configuration. For other configurations, this bit is reserved and returns 0 when read. Once set, the application cannot clear this bit.</p> <p>Value After Reset: 0x0 Volatile: true</p>
7:4	Reserved_4_7	RO	Reserved Field: Yes
9:8	IBI_STS	RO	<p>IBI Completion Status</p> <p>This field is common for SIR and MR</p> <p>2'b00: Reserved</p> <p>2'b01: IBI accepted by the Master (ACK response received)</p> <p>2'b10: Reserved</p> <p>2'b11: IBI Not Attempted</p> <p>The controller does not attempt to issue the IBI and generates the IBI Completion Status as 2'b11 if one of the following condition is true.</p> <ol style="list-style-type: none"> 1. Master has not assigned the Dynamic Address.



Bits	Name	Memory Access	Description
			2. Master has cleared the assigned Dynamic Address (through RSTDAA CCC). 3. Master has disabled the IBI event (through DISEC CCC). 4. The controller has switched the role to Master (applicable only for secondary master configuration). Value After Reset: 0x0
31:10	Reserved_10_31	RO	Reserved Field: Yes

7.6.2.34 DEVICE_CTRL_EXTENDED

Size: 32 bits

Offset:0x00B0

Bits	Name	Memory Access	Description
1:0	DEV_OPERATION_MODE	RW	This bit is used to select the Device Operation Mode before the controller is enabled. This field is written only when the DWC_mipi_i3c is disabled. 0: Master 1: Slave 2: Reserved 3: Reserved The controller automatically updates this field once the role change happens in secondary master mode. Values: 0x0 (MASTER): Master 0x1 (SLAVE): Slave Value After Reset: 0x0 Volatile: true
2	Reserved_2_2	RO	Reserved Field: Yes

Bits	Name	Memory Access	Description
3	REQMST_ACK_CTRL	RW	In Slave mode of operation, this bit serves as a control to ACK/NACK GETACCMST CCC from current master. 0: ACK GETACCMST CCC 1: NACK GETACCMST CCC Values: 0x0 (ACK): ACK 0x1 (NACK): NACK Value After Reset: 0x0
31:4	Reserved_4_31	RO	Reserved Field: Yes

7.6.2.35 SCL_I3C_OD_TIMING

Size: 32 bits

Offset: 0x00B4

Bits	Name	Memory Access	Description
7:0	I3C_OD_LCNT	RW	I3C Open Drain Low Count. SCL Open-drain low count for I3C transfers targeted to I3C devices. Value After Reset: 0x10
15:8	Reserved_8_15	RO	Reserved Field: Yes
23:16	I3C_OD_HCNT	RW	I3C Open Drain High Count. SCL open-drain High count (I3C) for I3C transfers targeted to I3C devices. Value After Reset: 0xa
31:24	Reserved_24_31	RO	Reserved Field: Yes



7.6.2.36 SCL_I3C_PP_TIMING

Size: 32 bits

Offset: 0x00B8

Bits	Name	Memory Access	Description
7:0	I3C_PP_LCNT	RW	I3C Push Pull Low Count. SCL Push-pull low count for I3C transfers targeted to I3C devices. Value After Reset: 0xa
15:8	Reserved_8_15	RO	Reserved Field: Yes
23:16	I3C_PP_HCNT	RW	I3C Push Pull High Count. SCL push-pull High count for I3C transfers targeted to I3C devices. Value After Reset: 0xa

7.6.2.37 SCL_I2C_FM_TIMING

Size: 32 bits

Offset: 0x00BC

Bits	Name	Memory Access	Description
15:0	I2C_FM_LCNT	RW	I2C Fast Mode Low Count The SCL open-drain low count timing for I2C fast mode transfers. Value After Reset: 0x10
31:16	I2C_FM_HCNT	RW	I2C Fast Mode High Count The SCL open-drain high count timing for I2C fast mode transfers. Value After Reset: 0x10



7.6.2.38 SCL_I2C_FMP_TIMING

Size: 32 bits

Offset: 0x00C0

Bits	Name	Memory Access	Description
15:0	I2C_FMP_LCNT	RW	I2C Fast Mode Plus Low Count The SCL open-drain low count timing for I2C fast mode plus transfers. Value After Reset: 0x10
23:16	I2C_FMP_HCNT	RW	I2C Fast Mode Plus High Count The SCL open-drain high count timing for I2C fast mode plus transfers. Value After Reset: 0x10
31:24	Reserved_24_31	RO	Reserved Field: Yes

7.6.2.39 SCL_EXT_LCNT_TIMING

Size: 32 bits

Offset: 0x00C8

Bits	Name	Memory Access	Description
7:0	I3C_EXT_LCNT_1	RW	I3C Extended Low Count Register 1 SDR1 uses this register field for data transfer. Value After Reset: 0x20
15:8	I3C_EXT_LCNT_2	RW	I3C Extended Low Count Register 2 SDR2 uses this register field for data transfer. Value After Reset: 0x20
23:16	I3C_EXT_LCNT_3	RW	I3C Extended Low Count Register 3 SDR3 uses this register field for data transfer. Value After Reset: 0x20



Bits	Name	Memory Access	Description
31:24	I3C_EXT_LCNT_4	RW	I3C Extended Low Count Register 4 SDR4 uses this register field for data transfer. Value After Reset: 0x20

7.6.2.40 SCL_EXT_TERMN_LCNT_TIMING

Size: 32 bits

Offset: 0x00CC

Bits	Name	Memory Access	Description
3:0	I3C_EXT_TERMN_LCNT	RW	I3C Read Termination Bit Low count. Extended I3C Read Termination Bit low count for I3C Read transfers. Effective Termination-Bit Low Period is derived based on the SDR speed as shown below SDR0 speed: I3C_PP_LCNT + I3C_EXT_TERMN_LCNT SDR1 speed: I3C_EXT_LCNT_1 + I3C_EXT_TERMN_LCNT SDR2 speed: I3C_EXT_LCNT_2 + I3C_EXT_TERMN_LCNT SDR3 speed: I3C_EXT_LCNT_3 + I3C_EXT_TERMN_LCNT SDR4 speed: I3C_EXT_LCNT_4 + I3C_EXT_TERMN_LCNT Value After Reset: 0x0
31:4	Reserved_4_31	RO	Reserved Field: Yes

7.6.2.41 SDA_HOLD_SWITCH_DLY_TIMING

Size: 32 bits

Offset: 0x00D0



Bits	Name	Memory Access	Description
15:0	Reserved_0_15	RO	Reserved Field: Yes
18:16	SDA_TX_HOLD	RW	This field controls the hold time (in term of the core clock period) of the transmit data (SDA) with respect to the SCL edge in FM+ SDR and DDR speed mode of operations. This field is not applicable for the ternary speed modes. The valid values are 1 to 7. Others are Reserved. Value After Reset: 0x1
31:19	Reserved_19_31	RO	Reserved Field: Yes

7.6.2.42 BUS_FREE_AVAIL_TIMING

Size: 32 bits

Offset: 0x00D4

Bits	Name	Memory Access	Description
15:0	BUS_FREE_TIME	RW	This register field is used only in Master mode of operation I3C Bus Free Count Value. In Pure Bus System, this field represents tCAS parameter. In Mixed Bus system, this field is expected to be programmed to tLOW of I2C Timing. Value After Reset: 0x20
31:16	BUS_AVAILABLE_TIME	RW	This register field is used only in Slave mode of operation Bus Available Count Value. This field is used by the Slave/Non-current Master to initiate an IBI after STOP condition. Value After Reset: 0x20



7.6.2.43 BUS_IDLE_TIMING

Size: 32 bits

Offset: 0x00D8

Bits	Name	Memory Access	Description
19:0	BUS_IDLE_TIME	RW	Bus Idle Count Value. This field is used by the controller in Slave or Non-Current Master mode to initiate Hot-Join request if the dynamic address is not valid. Value After Reset: 0x20
31:20	Reserved_20_31	RO	Reserved Field: Yes

7.6.2.44 SCL_LOW_MST_EXT_TIMEOUT

Size: 32 bits

Offset: 0x00DC

Bits	Name	Memory Access	Description
25:0	SCL_LOW_MST_TIMEOUT_COUNT	RW	This count defines the number of core clock periods to count for generation of the SCL Low Bus Reset Pattern. Value After Reset: 0x3567e0
31:26	Reserved_26_31	RO	Reserved Field: Yes

7.6.2.45 I3C_VER_ID

Size: 32 bits

Offset: 0x00E0



Bits	Name	Memory Access	Description
31:0	I3C_VER_ID	RO	<p>Current release number This field indicates the Synopsys DesignWare Cores DWC_mipi_i3c current release number that is read by an application. For example, release number "1.00a" is represented in ASCII as 0x313030. Lower 8 bits read from this register can be ignored by the application. An application reading this register along with the I3C_VER_TYPE register, gathers details of the current release.</p> <p>Value After Reset: 0x3130302a</p>

7.6.2.46 I3C_VER_TYPE

Size: 32 bits

Offset: 0x00E4

Bits	Name	Memory Access	Description
31:0	I3C_VER_TYPE	RO	<p>Current release type This field indicates the Synopsys DesignWare Cores DWC_mipi_i3c current release type that is read by an application. For example, release type "ga" is represented in ASCII as 0x6761 and "ea" is represented as 0x6561. Lower 16 bits read from this register can be ignored by the application if release type is "ga". If release type is "ea" the lower 16 bits represents the "ea" release version. An application reading this register along with the I3C_VER_ID register, gathers details of the current release.</p> <p>Value After Reset: 0x6c633033</p>

7.6.2.47 QUEUE_SIZE_CAPABILITY

Size: 32 bits

Offset: 0x00E8

Bits	Name	Memory Access	Description
3:0	TX_BUF_SIZE	RO	<p>Transmit Data Buffer Size This field reflects the configured Transmit Buffer size (in DWORDS) in Encoded Values.</p> <p>Values:</p> <ul style="list-style-type: none"> - 0x0: 2 DWORDS - 0x1: 4 DWORDS - 0x2: 8 DWORDS - 0x3: 16 DWORDS - 0x4: 32 DWORDS - 0x5: 64 DWORDS <p>Value After Reset: 0x5</p>
7:4	RX_BUF_SIZE	RO	<p>Receive Data Buffer Size This field reflects the configured Receive Buffer size (in DWORDS) in Encoded Values.</p> <p>Values:</p> <ul style="list-style-type: none"> - 0x0: 2 DWORDS - 0x1: 4 DWORDS - 0x2: 8 DWORDS - 0x3: 16 DWORDS - 0x4: 32 DWORDS - 0x5: 64 DWORDS <p>Value After Reset: 0x5</p>
11:8	CMD_BUF_SIZE	RO	<p>Command Queue Size This field reflects the configured Command Queue size (in DWORDS) in Encoded Values.</p> <p>Values:-</p> <ul style="list-style-type: none"> 0x0: 2 DWORDS 0x1: 4 DWORDS 0x2: 8 DWORDS 0x3: 16 DWORDS <p>Value After Reset: 0x3</p>
15:12	RESP_BUF_SIZE	RO	Response Queue Size



			<p>This field reflects the configured Response Queue size (in DWORDS) in Encoded Values.</p> <p>Values:</p> <ul style="list-style-type: none"> - 0x0: 2 DWORDS - 0x1: 4 DWORDS - 0x2: 8 DWORDS - 0x3: 16 DWORDS <p>Value After Reset: 0x2</p>
19:16	IBI_BUF_SIZE	RO	<p>IBI Queue Size</p> <p>This field reflects the configured IBI Queue size (in DWORDS) in Encoded Values.</p> <p>Values:</p> <ul style="list-style-type: none"> - 0x0: 2 DWORDS - 0x1: 4 DWORDS - 0x2: 8 DWORDS - 0x3: 16 DWORDS <p>Value After Reset: 0x3</p>
31:20	Reserved_20_31	RO	Reserved Field: Yes

7.6.2.48 DEV_CHAR_TABLE1_LOC1

Size: 32 bits

Offset: 0x0200

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	<p>The LSB 32-bit value of Provisional-ID</p> <p>Value After Reset: 0x0</p> <p>Testable: untestable</p> <p>Volatile: true</p>

7.6.2.49 DEV_CHAR_TABLE1_LOC2

Size: 32 bits

Offset: 0x0204



Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.50 DEV_CHAR_TABLE1_LOC3

Size: 32 bits

Offset: 0x0208

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.51 DEV_CHAR_TABLE1_LOC4

Size: 32 bits

Offset: 0x020C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true



Bits	Name	Memory Access	Description
31:8	Reserved_8_31	RW	Reserved Field: Yes

[7.6.2.52 DEV_CHAR_TABLE2_LOC1](#)

Size: 32 bits

Offset: 0x0210

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true

[7.6.2.53 DEV_CHAR_TABLE2_LOC2](#)

Size: 32 bits

Offset: 0x0214

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.54 DEV_CHAR_TABLE2_LOC3](#)

Size: 32 bits

Offset: 0x0218

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.55 DEV_CHAR_TABLE2_LOC4

Size: 32 bits

Offset: 0x021C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.56 DEV_CHAR_TABLE3_LOC1

Size: 32 bits

Offset: 0x0220

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true



[7.6.2.57 DEV_CHAR_TABLE3_LOC2](#)

Size: 32 bits

Offset: 0x0224

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.58 DEV_CHAR_TABLE3_LOC3](#)

Size: 32 bits

Offset: 0x0228

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.59 DEV_CHAR_TABLE3_LOC4](#)

Size: 32 bits

Offset: 0x022C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

[7.6.2.60 DEV_CHAR_TABLE4_LOC1](#)

Size: 32 bits

Offset: 0x0230

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true

[7.6.2.61 DEV_CHAR_TABLE4_LOC2](#)

Size: 32 bits

Offset: 0x0234

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.62 DEV_CHAR_TABLE4_LOC3](#)

Size: 32 bits

Offset: 0x0238



Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.63 DEV_CHAR_TABLE4_LOC4

Size: 32 bits

Offset: 0x023C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.64 DEV_CHAR_TABLE5_LOC1

Size: 32 bits

Offset: 0x0240

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true



[7.6.2.65 DEV_CHAR_TABLE5_LOC2](#)

Size: 32 bits

Offset: 0x0244

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.66 DEV_CHAR_TABLE5_LOC3](#)

Size: 32 bits

Offset: 0x0248

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.67 DEV_CHAR_TABLE5_LOC4](#)

Size: 32 bits

Offset: 0x024C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.68 DEV_CHAR_TABLE6_LOC1

Size: 32 bits

Offset: 0x0250

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true

7.6.2.69 DEV_CHAR_TABLE6_LOC2

Size: 32 bits

Offset: 0x0254

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.70 DEV_CHAR_TABLE6_LOC3

Size: 32 bits

Offset: 0x0258



Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.71 DEV_CHAR_TABLE6_LOC4

Size: 32 bits

Offset: 0x025C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.72 DEV_CHAR_TABLE7_LOC1

Size: 32 bits

Offset: 0x0260

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true



[7.6.2.73 DEV_CHAR_TABLE7_LOC2](#)

Size: 32 bits

Offset: 0x0264

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.74 DEV_CHAR_TABLE7_LOC3](#)

Size: 32 bits

Offset: 0x0268

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.75 DEV_CHAR_TABLE7_LOC4](#)

Size: 32 bits

Offset: 0x026C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.76 DEV_CHAR_TABLE8_LOC1

Size: 32 bits

Offset: 0x0270

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true

7.6.2.77 DEV_CHAR_TABLE8_LOC2

Size: 32 bits

Offset: 0x0274

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.78 DEV_CHAR_TABLE8_LOC3

Size: 32 bits

Offset: 0x0278



Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.79 DEV_CHAR_TABLE8_LOC4

Size: 32 bits

Offset: 0x027C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.80 DEV_CHAR_TABLE9_LOC1

Size: 32 bits

Offset: 0x0280

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true



[7.6.2.81 DEV_CHAR_TABLE9_LOC2](#)

Size: 32 bits

Offset: 0x0284

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.82 DEV_CHAR_TABLE9_LOC3](#)

Size: 32 bits

Offset: 0x0288

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.83 DEV_CHAR_TABLE9_LOC4](#)

Size: 32 bits

Offset: 0x028C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.84 DEV_CHAR_TABLE10_LOC1

Size: 32 bits

Offset: 0x0290

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true

7.6.2.85 DEV_CHAR_TABLE10_LOC2

Size: 32 bits

Offset: 0x0294

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.86 DEV_CHAR_TABLE10_LOC3

Size: 32 bits

Offset: 0x0298



Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

7.6.2.87 DEV_CHAR_TABLE10_LOC4

Size: 32 bits

Offset: 0x029C

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0 Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

7.6.2.88 DEV_CHAR_TABLE11_LOC1

Size: 32 bits

Offset: 0x02A0

Bits	Name	Memory Access	Description
31:0	LSB_PROVISIONAL_ID	RW	The LSB 32-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true



[7.6.2.89 DEV_CHAR_TABLE11_LOC2](#)

Size: 32 bits

Offset: 0x02A4

Bits	Name	Memory Access	Description
15:0	MSB_PROVISIONAL_ID	RW	The MSB 16-bit value of Provisional-ID Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.90 DEV_CHAR_TABLE11_LOC3](#)

Size: 32 bits

Offset: 0x02A8

Bits	Name	Memory Access	Description
7:0	DCR	RW	Device Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
15:8	BCR	RW	Bus Characteristic Value Value After Reset: 0x0 Testable: untestable Volatile: true
31:16	Reserved_16_31	RW	Reserved Field: Yes

[7.6.2.91 DEV_CHAR_TABLE11_LOC4](#)

Size: 32 bits

Offset: 0x02AC

Bits	Name	Memory Access	Description
7:0	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address assigned. Value After Reset: 0x0



Bits	Name	Memory Access	Description
			Testable: untestable Volatile: true
31:8	Reserved_8_31	RW	Reserved Field: Yes

[7.6.2.92 DEV_ADDR_TABLE_LOC1](#)

Size: 32 bits

Offset: 0x02C0

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes



Bits	Name	Memory Access	Description
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.93 DEV_ADDR_TABLE_LOC2

Size: 32 bits

Offset: 0x02C4

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes



Bits	Name	Memory Access	Description
23:16	DEV_DYNAMIC_ADDR	RW	<p>Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$</p> <p>Value After Reset: 0x0 Testable: untestable</p>
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	<p>This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master.</p> <p>Value After Reset: 0x0 Testable: untestable</p>
31	LEGACY_I2C_DEVICE	RW	<p>Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
			Testable: untestable

7.6.2.94 DEV_ADDR_TABLE_LOC3

Size: 32 bits

Offset: 0x02C8

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave



Bits	Name	Memory Access	Description
			does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.95 DEV_ADDR_TABLE_LOC4

Size: 32 bits

Offset: 0x02CC

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The



			MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment (~XOR(DEV_DYNAMIC_ADDR[22:16])) Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.96 DEV_ADDR_TABLE_LOC5

Size: 32 bits

Offset: 0x02D0



Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the



Bits	Name	Memory Access	Description
			slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.97 DEV_ADDR_TABLE_LOC6

Size: 32 bits

Offset: 0x02D4

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable



Bits	Name	Memory Access	Description
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.98 DEV_ADDR_TABLE_LOC7

Size: 32 bits

Offset: 0x02D8

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable



Bits	Name	Memory Access	Description
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	<p>Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment</p> $(\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ <p>Value After Reset: 0x0 Testable: untestable</p>
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	<p>This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master. Value After Reset: 0x0 Testable: untestable</p>



Bits	Name	Memory Access	Description
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.99 DEV_ADDR_TABLE_LOC8

Size: 32 bits

Offset: 0x02DC

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim \text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the



Bits	Name	Memory Access	Description
			<p>device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master.</p> <p>Value After Reset: 0x0 Testable: untestable</p>
31	LEGACY_I2C_DEVICE	RW	<p>Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.</p> <p>Value After Reset: 0x0 Testable: untestable</p>

7.6.2.100 DEV_ADDR_TABLE_LOC9

Size: 32 bits

Offset: 0x02E0

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	<p>Device Static Address. Value After Reset: 0x0 Testable: untestable</p>
15:7	Reserved_7_15	RW	Reserved Field: Yes



Bits	Name	Memory Access	Description
23:16	DEV_DYNAMIC_ADDR	RW	<p>Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim \text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$</p> <p>Value After Reset: 0x0 Testable: untestable</p>
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	<p>This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master.</p> <p>Value After Reset: 0x0 Testable: untestable</p>



Bits	Name	Memory Access	Description
31	LEGACY_I2C_DEVICE	RW	Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device. Value After Reset: 0x0 Testable: untestable

7.6.2.101

DEV_ADDR_TABLE_LOC10

Size: 32 bits

Offset: 0x02E4

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	Device Static Address. Value After Reset: 0x0 Testable: untestable
15:7	Reserved_7_15	RW	Reserved Field: Yes
23:16	DEV_DYNAMIC_ADDR	RW	Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment $(\sim \text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16]))$ Value After Reset: 0x0 Testable: untestable
28:24	Reserved_24_28	RW	Reserved Field: Yes



Bits	Name	Memory Access	Description
30:29	DEV_NACK_RETRY_CNT	RW	<p>This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master.</p> <p>Value After Reset: 0x0 Testable: untestable</p>
31	LEGACY_I2C_DEVICE	RW	<p>Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.</p> <p>Value After Reset: 0x0 Testable: untestable</p>

7.6.2.102

DEV_ADDR_TABLE_LOC11

Size: 32 bits

Offset: 0x02E8

Bits	Name	Memory Access	Description
6:0	DEV_STATIC_ADDR	RW	<p>Device Static Address. Value After Reset: 0x0 Testable: untestable</p>
15:7	Reserved_7_15	RW	Reserved Field: Yes

Bits	Name	Memory Access	Description
23:16	DEV_DYNAMIC_ADDR	RW	<p>Device Dynamic Address with parity. This field consists of Dynamic address and Parity Bit. The LSB bits [22:16] should consist of Dynamic Address field indicates the address to be assigned for the winning I3C device when using ENTDAA command. The MSB[23] bit is the odd parity of the 7-bit Dynamic address used for ENTDAA address assignment ($\sim\text{XOR}(\text{DEV_DYNAMIC_ADDR}[22:16])$)</p> <p>Value After Reset: 0x0</p> <p>Testable: untestable</p>
28:24	Reserved_24_28	RW	Reserved Field: Yes
30:29	DEV_NACK_RETRY_CNT	RW	<p>This field is used to set the Device NACK Retry count for the particular device. If the Device NACK's for the device address, the controller automatically retries the same device until this count expires. If the Slave does not ACK for the mentioned number of retries, then Controller generates an error response and move to the Halt state. This feature is used for Retry Model for the following features mentioned in the I3C Specification: Retry Model for Direct GET CCC Commands. The incoming SIR-IBI matches with the slave address initiated by the Master.</p> <p>Value After Reset: 0x0</p> <p>Testable: untestable</p>
31	LEGACY_I2C_DEVICE	RW	<p>Legacy I2C device or not. This bit should be set to 1 if the device is a legacy I2C device.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
			Testable: untestable



7.7 MDIO registers

7.7.1 List of registers and offset details

Register	Offset	Memory Access	Description
MDIO_Ctrl	0x0000	RW	MDIO link control
MDIO_Cfg	0x0020	RW	Configuration of MDIO hardware
MDIO_Addr_Data	0x0024	RW	MDIO address and data register
MDIO_Op_Ctr_I	0x0028	RW	MDIO operation and control register
MDIO_Interrupt_Status_Reg	0x0030	RW	MDIO interrupt status
MDIO_Interrupt_Enable_Reg	0x0034	RW	MDIO interrupt enable

7.7.2 Register definition

7.7.2.1 MDIO_Ctrl

Size: 32 bits

Offset: 0x0000

Bits	Name	Memory Access	Description
0	rmt	RW	MDIO busy status register When this bit is set, MDIO master is busy. When MDIO command is executed, this bit is set 0.
31:1	RESERVED	RO	Reserved

7.7.2.2 MDIO_Cfg

Size: 32 bits

Offset: 0x0020

Bits	Name	Memory Access	Description
9:0	mdcdiv	RW	<p>MDIO Clock Divisor</p> <p>This field contains the clock divisor for generating the MDC from pclk_i or pclk_i/32. The valid range is 2 to 510 (i.e. value of 0 is reserved) only even numbers are supported with bit [0] = 0 or ignored. The programmed divisor value is restricted to even numbers, so that duty cycle of MDC is 50%.</p> <p>Value after reset : 10'b 0001010000</p>
15:10	RESERVED	RO	Reserved
16	fm	RW	<p>Enable Fast mode</p> <p>When this bit is set, pclk_i is used for generating MDC.</p> <p>When this bit is reset, pclk_i is divided by 32 and then used to generate MDC.</p> <p>Note: When this bit is set, ensure that MDCCDIV field is programmed with appropriate non-zero value to avoid higher frequency clock (equal to pclk_i) being driven on MDC.</p> <p>Value after reset: 0x1</p>
17	mdioen	RW	<p>Enable MDIO</p> <p>When this bit is set, the MDIO Master is enabled for MDIO accesses.</p> <p>When this bit is reset, the MDIO Master do not</p>



Bits	Name	Memory Access	Description
			perform MDIO accesses, i.e. MDC and MDIO interface signals do not toggle. Value after reset:0x0
18	mdiocl	RW	MDIO Clause When this bit is set, Clause 45 frames are sent. When this bit is reset, Clause 22 frames are sent. Value after reset:0x0
19	pse	RW	Preamble Suppression Enable When this bit is set, the MDIO Master suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is reset, the MDIO frame always has 32 bits of preamble as defined in the IEEE specification. Value after reset:0x0
20	btt	RW	Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MDIO Master informs the completion of a read or write command at the end of frame transfer by de-asserting BUSY (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated



Bits	Name	Memory Access	Description
			<p>for the previous frame.</p> <p>When this bit is reset, then the read/write command completion (BUSY is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame.</p> <p>This bit must not be set when NTC=0. Value after reset:0x0</p>
23:21	ntc	RW	<p>Number of Trailing Clocks</p> <p>This field controls the number of trailing clock cycles generated on m_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. For example, programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.</p> <p>Value after reset:0x0</p>
27:24	RESERVED	RO	Reserved
28	ecif	RW	<p>Enable Capturing MDI on Falling Edge</p> <p>When this bit is set, the MDIO Master captures the MDIO Input (MDI) on the falling edge of MDIO Clock(MDC).</p> <p>When this bit is reset, the MDIO Master captures the</p>



Bits	Name	Memory Access	Description
			MDIO Input (MDI) on the rising edge of MDIO Clock(MDC). Value after reset:0x0
31:29	RESERVED	RO	Reserved

7.7.2.3 MDIO_Addr_Data

Size: 32 bits

Offset: 0x0024

Bits	Name	Memory Access	Description
15:0	data	RW	<p>PHY Write or Read Data</p> <p>This field contains data to be written or read from PHY.</p> <p>When Read or Post Read Increment Address operations are initiated, this field contains the valid data read from PHY when BUSY bit in MDIO_Op_Ctrl register is cleared.</p> <p>When Write operations are initiated, this field can be updated with new data only when BUSY bit in MDIO_Op_Ctrl register is cleared.</p> <p>Value after reset:0x0</p>
31:16	regad	RW	<p>PHY Register Address</p> <p>This field contains PHY Register Address (Clause 45 MDIO Address frame).</p> <p>Value after reset:0x0</p>

7.7.2.4 MDIO_Op_Ctrl

Size: 32 bits



Offset: 0x0028

Bits	Name	Memory Access	Description						
0	busy	RW	<p>MDIO Busy</p> <p>When this bit is set, MDIO Master initiates read, write, or post-increment read operation.</p> <p>DWC_mdio_mstr clears this bit when the operation is completed.</p> <p>During the MDIO transfer cycle, this bit remains high to indicate the cycle is in progress. When the Busy bit is high, do not modify any bits in MDIO_Addr_Data and MDIO_Op_Ctrl registers.</p> <p>When the read or post-increment read operation completes the MDIO_Addr_Data register contains the data read from PHY register for current MDIO transfer.</p> <p>Access restriction applies. Setting 1 sets. Self cleared. Setting 0 had no effect</p> <p>Value after reset:0x0</p>						
5:1	devad	RW	<p>MDIO DeviceAddress</p> <p>This field contains Device Address for Clause.</p> <p>Value after reset:0x0</p>						
7:6	RESERVED	RO	Reserved						
12:8	prtad	RW	<p>MDIO Port or PHY Address</p> <p>This field contains Port/PHY Address for Clause 45 or PHY address for Clause 22 frames.</p> <p>Value after reset:0x0</p>						
14:13	op	RW	<p>MDIO Operation Code</p> <p>Values:</p> <table> <tr> <td>00:</td> <td>Reserved</td> </tr> <tr> <td>01:</td> <td>Write</td> </tr> <tr> <td>10:</td> <td>Post Read Increment Address</td> </tr> </table>	00:	Reserved	01:	Write	10:	Post Read Increment Address
00:	Reserved								
01:	Write								
10:	Post Read Increment Address								



			<p>for Clause 45 PHY 11: Read</p> <p>When Clause 22 PHY is enabled, only Write and Read commands are valid, i.e. only bit [14] is valid, where bit[14] = 0 is Write and bit[14] =1 is Read</p> <p>Value after reset:0x0</p>
15	saadr	RW	<p>Skip Address Frame</p> <p>When this bit is set, the MDIO Master do not send Clause 45 address frames before read, write, or post-increment read data frames.</p> <p>When this bit is reset, the MDIO Master sends Clause 45 address frames read, write, or post increment read data frames.</p> <p>Value after reset:0x0</p>
31:16	RESERVED	RO	Reserved

7.7.2.5 MDIO_Interrupt_Status_Reg

Size: 32 bits

Offset: 0x0030

Bits	Name	Memory Access	Description
0	mtcis	RW	<p>MDIO Transaction Complete Interrupt Status.</p> <p>This bit indicates an interrupt event after the completion of MDIO transaction (BUSY bit in MDIO_Op_Ctrl register is cleared by MDIO Master). To reset this bit, the application must write 1 to this bit.</p> <p>Access restriction applies. Setting 1 clears. Setting 0 had no effect. Self-set to 1 on</p>



			internal event. Value after reset:0x0
31:1	RESERVED	RO	Reserved

7.7.2.6 MDIO Interrupt Enable Reg

Size: 32 bits

Offset: 0x0034

Bits	Name	Memory Access	Description
0	mtcie	RW	<p>MDIO Transaction Complete Interrupt Enable.</p> <p>When this bit is set, it enables the assertion of the interrupt when MTCIS bit is set in MDIO Interrupt_Status register.</p> <p>When this bit is reset, it disables the assertion of the interrupt when MTCIS bit is set in MDIO Interrupt_Status register.</p> <p>Value after reset:0x0</p>
31:1	RESERVED	RO	Reserved



7.8 UART registers

7.8.1 List of registers and offset details



Register	Offset	Memory Access	Description
RBR	0x000	RO	Receive Buffer Register
DLL	0x000	RW	Divisor Latch Low
THR	0x000	WO	Transmit Holding Register
DLH	0x004	RW	Divisor Latch High
IER	0x004	RW	Interrupt Enable Register
FCR	0x008	WO	FIFO Control Register (FCR)
IIR	0x008	RO	Interrupt Identification Register
LCR	0x00c	RW	Line Control Register
MCR	0x0010	RW	Modem Control Register
LSR	0x0014	RO	Line Status Register
MSR	0x0018	RO	Modem Status Register
SCR	0x001c	RW	Scratchpad Register
SRBR0	0x0030	RO	Shadow Receive Buffer Register
STHR0	0x0030	WO	Shadow Transmit Holding Register
SRBR1	0x0034	RO	Shadow Receive Buffer Register
STHR1	0x0034	WO	Shadow Transmit Holding Register
SRBR2	0x0038	RO	Shadow Receive Buffer Register
STHR2	0x0038	WO	Shadow Transmit Holding Register
SRBR3	0x003c	RO	Shadow Receive Buffer Register
STHR3	0x003c	WO	Shadow Transmit Holding Register
SRBR4	0x0040	RO	Shadow Receive Buffer Register
STHR4	0x0040	WO	Shadow Transmit Holding Register
SRBR5	0x0044	RO	Shadow Receive Buffer Register
STHR5	0x0044	WO	Shadow Transmit Holding Register
SRBR6	0x0048	RO	Shadow Receive Buffer Register
STHR6	0x0048	WO	Shadow Transmit Holding Register
SRBR7	0x004c	RO	Shadow Receive Buffer Register
STHR7	0x004c	WO	Shadow Transmit Holding Register
SRBR8	0x0050	RO	Shadow Receive Buffer Register
STHR8	0x0050	WO	Shadow Transmit Holding Register
SRBR9	0x0054	RO	Shadow Receive Buffer Register
STHR9	0x0054	WO	Shadow Transmit Holding Register
SRBR10	0x0058	RO	Shadow Receive Buffer Register
STHR10	0x0058	WO	Shadow Transmit Holding Register
SRBR11	0x005c	RO	Shadow Receive Buffer Register
STHR11	0x005c	WO	Shadow Transmit Holding Register
SRBR12	0x0060	RO	Shadow Receive Buffer Register
STHR12	0x0060	WO	Shadow Transmit Holding Register
SRBR13	0x0064	RO	Shadow Receive Buffer Register
STHR13	0x0064	WO	Shadow Transmit Holding Register
SRBR14	0x0068	RO	Shadow Receive Buffer Register



STHR14	0x0068	WO	Shadow Transmit Holding Register
SRBR15	0x006c	RO	Shadow Receive Buffer Register
STHR15	0x006c	WO	Shadow Transmit Holding Register
FAR	0x0070	RW	FIFO Access Register
TFR	0x0074	WO	Transmit FIFO Read
RFW	0x0078	WO	Receive FIFO Write
USR	0x007c	RO	UART Status register
TFL	0x0080	RO	Transmit FIFO Level
RFL	0x0084	RO	Transmit FIFO Level
SRR	0x0088	WO	Software Reset Register
SRTS	0x008c	RW	Shadow Request to Send
SBCR	0x0090	RW	Shadow Break Control Register
SDMAM	0x0094	RW	Shadow DMA Mode Register
SFE	0x0098	RW	Shadow FIFO Enable Register
SRT	0x009c	RW	Shadow RCVR Trigger Register
STET	0x00a0	RW	Shadow TX Empty Trigger Register
HTX	0x00a4	RW	Halt TX
DMASA	0x00a8	RO	DMA Software Acknowledge Register
DLF	0x00c0	RW	Divisor Latch Fraction Register
RAR	0x00c4	RW	Receive Address Register
TAR	0x00c8	RW	Transmit Address Register
LCR_EXT	0x00cc	RW	Line Extended Control Register
UART_PROT			
LEVEL	0x00d0	RW	UART Protection level register
REG_TIMEO			
UT_RST	0x00d4	RW	Register timeout counter reset value
CPR	0x00f4	RO	Component Parameter Register
UCV	0x00f8	RO	UART Component Version
CTR	0x00fc	RO	Component Type Register

7.8.2 Register definition

7.8.2.1 RBR (Receive Buffer Register)

Size: 32 bits

Offset: 0x0000



Bits	Name	Memory Access	Description
8:0	RBR	RO	<p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an over-run error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost and an over-run error occurs.</p> <p>Value After Reset : 0x0</p>
31:9	RSVD_RBR	RO	RBR 31to9or8 Reserved bits and read as zero (0).

7.8.2.2 DLL (Divisor Latch Low)

Size: 32 bits

Offset: 0x0000

Bits	Name	Memory Access	Description
7:0	DLL	RW	This register can be accessed only when the DLAB bit (LCR[7]) is set.



Bits	Name	Memory Access	Description
			<p>This register makes up the lower 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART.</p> <p>The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows:</p> $\text{baud rate} = (\text{serial clock freq}) / (16 * \text{divisor}).$ <p>Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur. Also, once the DLL is set, at least 8 clock cycles of the slowest uart clock should be allowed to pass before transmitting or receiving data.</p> <p>Value After Reset : 0x0</p>
31:8	RSVD_DLL_31to8	RO	Reserved

7.8.2.3 THR (Transmit Holding Register)

Size: 32 bits

Offset: 0x0000

Bits	Name	Memory Access	Description
8:0	THR	WO	<p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data</p>



Bits	Name	Memory Access	Description
			<p>should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that is set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>When UART_9BIT_DATA_EN=0, this field width is 8</p> <p>When UART_9BIT_DATA_EN=1, this field width is 9</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1</p> <p>Value After Reset : 0x0</p>
31:9	RSVD_THR	RO	Reserved

7.8.2.4 DLH (Divisor Latch High)

Size: 32 bits

Offset: 0x0004

Bits	Name	Memory Access	Description
7:0	DLH	RW	Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate



			<p>divisor for the UART.</p> <p>The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled) frequency divided by sixteen times the value of the baud rate divisor, as follows:</p> $\text{baud rate} = (\text{serial clock freq}) / (16 * \text{divisor})$ <p>With the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications will occur.</p> <p>Also, once the DLH is set, at least 8 clock cycles of the slowest Uart clock should be allowed to pass before transmitting or receiving data.</p> <p>Value After Reset : 0x0</p>
31:8	RSVD_DLH	RO	Reserved

7.8.2.5 IER (Interrupt Enable Register)

Size: 32 bits

Offset: 0x0004

Bits	Name	Memory Access	Description
0	ERBFI	RW	<p>Enable Received Data Available Interrupt</p> <p>This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFO's enabled). These are the second highest priority interrupts.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Disable Receive data Interrupt 0x1 (ENABLED): Enable Receive data Interrupt <p>Value After Reset : 0x0</p>



1	ETBEI	RW	<p>Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Disable Transmit empty interrupt 0x1 (ENABLED): Enable Transmit empty interrupt <p>Value After Reset : 0x0</p>
2	ELSI	RW	<p>Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Disable Receiver Line Status Interrupt 0x1 (ENABLED): Enable Receiver Line Status Interrupt <p>Value After Reset : 0x0</p>
3	EDSSI	RW	<p>Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Disable Modem Status Interrupt 0x1 (ENABLED): Enable Modem Status Interrupt <p>Value After Reset : 0x0</p>
4	ELCOLR	RO	<p>Interrupt Enable Register: ELCOLR, this bit controls the method for clearing the status in the LSR register.</p> <p>0 = LSR status bits are cleared either on reading Rx FIFO (RBR Read) or On reading LSR register.</p> <p>1 = LSR status bits are cleared only on reading LSR register</p>



			Writeable only when LSR_STATUS_CLEAR == Enabled, always readable. Values: 0x0 (DISABLED): Disable ALC 0x1 (ENABLED): Enable ALC Value After Reset : 0x0
6:5	RSVD_IER_6to5	RO	Reserved
7	PTIME	RW	Programmable THRE Interrupt Mode Enable Writeable only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. Values: 0x0 (DISABLED): Disable Programmable THRE Interrupt Mode 0x1 (ENABLED): Enable Programmable THRE Interrupt Mode Value After Reset : 0x0
31:8	RSVD_IER_31to8	RO	Reserved

7.8.2.6 FCR (FIFO Control Register)

Size: 32 bits

Offset: 0x0008

Bits	Name	Memory Access	Description
0	FIFOE	WO	FIFO Enable (or FIFOE). This register is only valid when the Uart is configured to have FIFO's implemented (FIFO_MODE != 0). This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.



			<p>Values: 0x0 (DISABLED): FIFO disabled 0x1 (ENABLED): FIFO enabled Value After Reset : 0x0</p>
1	RFIFOR	WO	<p>RCVR FIFO Reset (or RFIFOR). This resets the control portion of the receive FIFO and treats the FIFO as empty. This will also de-assert the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'selfclearing' and it is not necessary to clear this bit.</p> <p>Values: 0x1 (RESET): Receive FIFO reset Value After Reset : 0x0</p>
2	XFIFOR	WO	<p>XMIT FIFO Reset (or XFIFOR). This resets the control portion of the transmit FIFO and treats the FIFO as empty. This will also de-assert the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'selfclearing' and it is not necessary to clear this bit.</p> <p>Values: 0x1 (RESET): Transmit FIFO reset Value After Reset : 0x0</p>
3	DMAM	WO	<p>DMA Mode (or DMAM) This determines the DMA signaling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO).</p> <p>Values: 0x0 (MODE0): Mode 0 0x1 (MODE1): Mode 1 Value After Reset : 0x0</p>
5:4	TET	WO	<p>TX Empty Trigger (or TET) Writes will have no effect when THRE_MODE_USER == Disabled. This is</p>



			<p>used to select the empty threshold level at which the THRE Interrupts will be generated when the mode is active. It also determines when the dma_tx_req_n signal will be asserted when in certain modes of operation.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (FIFO_EMPTY): FIFO Empty 0x1 (FIFO_CHAR_2): 2 characters in FIFO 0x2 (FIFO_QUARTER_FULL): FIFO 1/4 full 0x3 (FIFO_HALF_FULL): FIFO 1/2 full <p>Value After Reset : 0x0</p>
7:6	RT	WO	<p>RCVR Trigger (or RT).</p> <p>This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. In auto flow control mode, it is used to determine when the rts_n signal will be de-asserted only when RTC_FCT is disabled.</p> <p>It also determines when the dma_rx_req_n signal will be asserted when in certain modes of operation.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (FIFO_CHAR_1): 1 character in FIFO 0x1 (FIFO_QUARTER_FULL): FIFO 1/4 full 0x2 (FIFO_HALF_FULL): FIFO 1/2 full 0x3 (FIFO_FULL_2): FIFO 2 less than full <p>Value After Reset : 0x0</p>
31:8	RSVD_FCR_31to8	RO	Reserved

7.8.2.7 IIR (Interrupt Identification Register)

Size: 32 bits

Offset: 0x0008



Bits	Name	Memory Access	Description
3:0	IID	RO	<p>Interrupt ID (or IID) This indicates the highest priority pending interrupt which can be one of the following types specified in Values. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (MODEM_STATUS): modem status 0x1 (NO_INTERRUPT_PENDING): no interrupt pending 0x2 (THR_EMPTY): THR empty 0x4 (RECEIVED_DATA_AVAILABLE): received data available 0x6 (RECEIVER_LINE_STATUS): receiver line status 0x7 (BUSY_DETECT): busy detect 0xc (CHARACTER_TIMEOUT): character timeout <p>Value After Reset : 0x1</p>
5:4	RSVD_IIR_5to4	RO	Reserved
7:6	FIFOSE	RO	<p>FIFOs Enabled (or FIFOSE). This is used to indicate whether the FIFOs are enabled or disabled.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): FIFOs are disabled 0x3 (ENABLED): FIFOs are enabled <p>Value After Reset : 0x0</p>
31:8	RSVD_IIR_31to8	RO	Reserved

7.8.2.8 LCR (Line Control Register)

Size: 32 bits

Offset: 0x000C



Bits	Name	Memory Access	Description
1:0	DLS	RW	<p>Data Length Select (or CLS as used in legacy)</p> <p>If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable.</p> <p>When DLS_E in LCR_EXT is set to 0, this register is used to select the number of data bits per character that the peripheral will transmit and receive.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (CHAR_5BITS): 5 data bits per character 0x1 (CHAR_6BITS): 6 data bits per character 0x2 (CHAR_7BITS): 7 data bits per character 0x3 (CHAR_8BITS): 8 data bits per character <p>Value After Reset : 0x0</p>
2	STOP	RW	<p>Number of stop bits</p> <p>If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable. This is used to select the number of stop bits per character that the peripheral will transmit and receive. If set to zero, one stop bit is transmitted in the serial data.</p> <p>If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected the receiver will only check the first stop bit.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (STOP_1BIT): 1 stop bit



Bits	Name	Memory Access	Description
			0x1 (STOP_1_5BIT_OR_2BIT): 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit Value After Reset : 0x0
3	PEN	RW	<p>Parity Enable</p> <p>If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable.</p> <p>This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): disable parity 0x1 (ENABLED): enable parity <p>Value After Reset : 0x0</p>
4	EPS	RW	<p>Even Parity Select</p> <p>If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable.</p> <p>This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic '1's is transmitted or checked. If set to zero, an odd number of logic '1's is transmitted or checked.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (ODD_PARITY): an odd parity is transmitted or checked 0x1 (EVEN_PARITY): an even parity is transmitted or checked <p>Value After Reset : 0x0</p>
5	SP	RW	<p>Stick Parity</p> <p>If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable.</p> <p>This bit is used to force parity value. When</p>



Bits	Name	Memory Access	Description
			<p>PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Stick parity disabled 0x1 (ENABLED): Stick parity enabled <p>Value After Reset : 0x0</p>
6	BC	RW	<p>Break Control Bit.</p> <p>This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared.</p> <p>If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Serial output is released for data transmission 0x1 (ENABLED): Serial output is forced to spacing state <p>Value After Reset : 0x0</p>
7	DLAB	RW	<p>Divisor Latch Access Bit.</p> <p>If UART_16550_COMPATIBLE == NO then, writeable only when UART is not busy (USR[0] is zero), otherwise always writable and always readable.</p> <p>This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH/LPDLL and LPDLH) to set the baud</p>



Bits	Name	Memory Access	Description
			<p>rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Divisor Latch register is writable only when UART Not BUSY 0x1 (ENABLED): Divisor Latch register is always readable and writable <p>Value After Reset : 0x0</p>
31:8	RSVD_LCR_31to8	RO	Reserved

7.8.2.9 MCR (Modem Control Register)

Size: 32 bits

Offset: 0x0010

Bits	Name	Memory Access	Description
0	DTR	RW	<p>Data Terminal Ready.</p> <p>This is used to directly control the Data Terminal Ready (dtr_n) output.</p> <p>The value written to this location is inverted and driven out on dtr_n.</p> <p>The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (INACTIVE): dtr_n de-asserted (logic1) 0x1 (ACTIVE): dtr_n asserted (logic 0)



Bits	Name	Memory Access	Description
			Value After Reset : 0x0
1	RTS	RW	<p>Request to Send.</p> <p>This is used to directly control the Request to Send (rts_n) output.</p> <p>The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data.</p> <p>When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal will be de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (INACTIVE): Request to Send rts_n de-asserted (logic 1) 0x1 (ACTIVE): Request to Send rts_n asserted (logic 0) <p>Value After Reset : 0x0</p>
2	OUT1	RW	<p>OUT1</p> <p>This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n. Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while</p>



Bits	Name	Memory Access	Description
			<p>the value of this location is internally looped back to an input.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (OUT1_0): out1_n de-asserted (logic 1) 0x1 (OUT1_1): out1_n asserted (logic 0) <p>Value After Reset : 0x0</p>
3	OUT2	RW	<p>OUT2 .</p> <p>This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n. Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (OUT2_0): out2_n de-asserted (logic 1) 0x1 (OUT2_1): out2_n asserted (logic 0) <p>Value After Reset : 0x0</p>
4	LoopBack	RW	<p>LoopBack Bit .</p> <p>This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled OR NOT active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low,</p>



Bits	Name	Memory Access	Description
			<p>while serial data output is inverted and looped back to the sir_in line.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Loopback mode disabled 0x1 (ENABLED): Loopback mode enabled <p>Value After Reset : 0x0</p>
5	AFCE	RO	<p>Auto Flow Control Enable .</p> <p>Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled .</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Auto Flow Control Mode disabled 0x1 (ENABLED): Auto Flow Control Mode enabled <p>Value After Reset: 0x0</p>
6	SIRE	RO	<p>SIR Mode Enable</p> <p>Writeable only when SIR_MODE == Enabled, always readable. Note: To enable SIR mode, write the appropriate value to the MCR register before writing to the LCR register.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): IrDA SIR Mode disabled 0x1 (ENABLED): IrDA SIR Mode enabled <p>Value After Reset : 0x0</p>
31:7	RSVD_MCR_31to7	RO	Reserved

7.8.2.10 LSR (Line Status Register)

Size: 32 bits

Offset: 0x0014



Bits	Name	Memory Access	Description
0	DR	RO	<p>Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. This bit is cleared when the RBR is read in the non-FIFO mode, or when the receiver FIFO is empty, in the FIFO mode.</p> <p>Values: 0x0 (NOT_READY): data not ready 0x1 (READY): data ready Value After Reset : 0x0</p>
1	OE	RO	<p>Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. Reading the LSR clears the OE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the OE bit (if LSR_STATUS_CLEAR==0).</p> <p>Values: 0x0 (NO_OVER_RUN_ERROR): no overrun error 0x1 (OVER_RUN_ERROR): overrun error Value After Reset : 0x0</p>
2	PE	RO	<p>Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set.</p>



Bits	Name	Memory Access	Description
			<p>If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time +data bits + parity + stop bits.</p> <p>If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART.</p> <p>In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO.</p> <p>It should be noted that the Parity Error (PE) bit (LSR[2]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). In this situation, the Parity Error bit is set if parity generation and detection is enabled (LCR[3]=1) and the parity is set to odd (LCR[4]=0). Reading the LSR clears the PE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the PE bit (if LSR_STATUS_CLEAR==0).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_PARITY_ERROR): no parity error 0x1 (PARITY_ERROR): parity error <p>Value After Reset : 0x0</p>
3	FE	RO	<p>Framing Error bit.</p> <p>This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data.</p> <p>In the FIFO mode, since the framing error is associated with a character received, it is</p>



Bits	Name	Memory Access	Description
			<p>revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs the UART will try resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) will be set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).</p> <p>This happens because the break character implicitly generates a framing error by holding the sin input to logic 0 for longer than the duration of a character. Reading the LSR clears the FE bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the FE bit (if LSR_STATUS_CLEAR==0).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_FRAMING_ERROR): no framing error 0x1 (FRAMING_ERROR): framing error <p>Value After Reset : 0x0</p>
4	BI	RO	<p>Break Interrupt bit.</p> <p>This is used to indicate the detection of a break sequence on the serial input data. If in UART mode it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be</p>



Bits	Name	Memory Access	Description
			<p>received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO.</p> <p>Reading the LSR clears the BI bit (if LSR_STATUS_CLEAR==1) Or Reading the LSR or RBR clears the BI bit (if LSR_STATUS_CLEAR==0). In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.</p> <p>Note: If a FIFO is full when a break condition is received, a FIFO overrun occurs. The break condition and all the information associated with it-parity and framing errors-is discarded; any information that a break character was received is lost.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_BREAK): No break sequence detected 0x1 (BREAK): Break sequence detected <p>Value After Reset : 0x0</p>
5	THRE	RO	<p>Transmit Holding Register Empty bit.</p> <p>If THRE_MODE_USER = Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are</p>



Bits	Name	Memory Access	Description
			<p>active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): THRE interrupt control is disabled 0x1 (ENABLED): THRE interrupt control is enabled <p>Value After Reset: 0x1</p>
6	TEMT	RO	<p>Transmitter Empty bit.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFO's enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in the non-FIFO mode or FIFO's are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Transmitter not empty 0x1 (ENABLED): Transmitter empty <p>Value After Reset: 0x1</p>
7	RFE	RO	<p>Receiver FIFO Error bit.</p> <p>This bit is only relevant when FIFO_MODE != NONE AND FIFO's are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_RX_FIFO_ERROR): No error in RX FIFO

Bits	Name	Memory Access	Description
			0x1 (RX_FIFO_ERROR): Error in RX FIFO Value After Reset: 0x0 Exists: FIFO_MODE != 0
8	ADDR_RCVD	RO	Address Received Bit. If 9Bit data mode (LCR_EXT[0]=1) is enabled, this bit is used to indicate the 9th bit of the receive data is set to 1. This bit can also be used to indicate whether the incoming character is address or data. 1 = Indicates the character is address. 0 = Indicates the character is data. In the FIFO mode, since the 9th bit is associated with a character received, it is revealed when the character with the 9th bit set to 1 is at the top of the FIFO. Reading the LSR clears the 9BIT. Note: User needs to ensure that interrupt gets cleared (reading LSR register) before the next address byte arrives. If there is a delay in clearing the interrupt, then Software will not be able to distinguish between multiple address related interrupt. Exists: UART_9BIT_DATA_EN == 1 Value After Reset : 0x0
31:9	RSVD_LSR_31to9	RO	Reserved

7.8.2.11 MSR (Modem Status Register)

Size: 32 bits

Offset: 0x0018



Bits	Name	Memory Access	Description
0	DCTS	RO	<p>Delta Clear to Send.</p> <p>This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] set to one), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit will get set when the reset is removed if the cts_n signal remains asserted.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_CHANGE): no change on cts_n since last read of MSR 0x1 (CHANGE): change on cts_n since last read of MSR <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
1	DDSR	RO	<p>Delta Data Set Ready.</p> <p>This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] set to one), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit will get set when the reset is removed if the dsr_n signal remains asserted.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_CHANGE): no change on dsr_n since last read of MSR 0x1 (CHANGE): change on dsr_n since last read of MSR <p>Value After Reset: 0x0</p> <p>Exists: Always</p>



Bits	Name	Memory Access	Description
2	TERI	RO	<p>Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active low, to an inactive high state) has occurred since the last time the MSR was read. Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] set to one), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_CHANGE): no change on ri_n since last read of MSR 0x1 (CHANGE): change on ri_n since last read of MSR <p>Value After Reset: 0x0 Exists: Always</p>
3	DDCD	RO	<p>Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] set to one), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit will get set when the reset is removed if the dcd_n signal remains asserted.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_CHANGE): No change on dcd_n since last read of MSR 0x1 (CHANGE): change on dcd_n since last read of MSR <p>Value After Reset: 0x0 Exists: Always</p>
4	CTS	RO	<p>Clear to Send. This is used to indicate the current state of the modem control line cts_n. That is,</p>



Bits	Name	Memory Access	Description
			<p>this bit is the complement cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the Uart. In Loopback Mode (MCR[4] set to one), CTS is the same as MCR[1] (RTS).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DEASSERTED): cts_n input is de-asserted (logic 1) 0x1 (ASSERTED): cts_n input is asserted (logic 0) <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
5	DSR	RO	<p>Data Set Ready.</p> <p>This is used to indicate the current state of the modem control line dsr_n. That is this bit is the complement dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the Uart. In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DEASSERTED): dsr_n input is de-asserted (logic 1) 0x1 (ASSERTED): dsr_n input is asserted (logic 0) <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
6	RI	RO	<p>Ring Indicator. This is used to indicate the current state of the modem control line ri_n. That is this bit is the complement ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. In Loopback Mode (MCR[4] set to one), RI is</p>



Bits	Name	Memory Access	Description
			<p>the same as MCR[2] (Out1).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DEASSERTED): ri_n input is de-asserted (logic 1) 0x1 (ASSERTED): ri_n input is asserted (logic 0) <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
7	DCD	RO	<p>Data Carrier Detect.</p> <p>This is used to indicate the current state of the modem control line dcd_n. That is this bit is the complement dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set.</p> <p>In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DEASSERTED): dcd_n input is de-asserted (logic 1) 0x1 (ASSERTED): dcd_n input is asserted (logic 0) <p>Value After Reset : 0x0</p>
31:8	RSVD_MSR_31to8	RO	Reserved

7.8.2.12 SCR (Scratchpad Register)

Size: 32 bits

Offset: 0x001C

Bits	Name	Memory Access	Description
7:0	SCR	RW	This register is for programmers to use as a temporary storage space.



Bits	Name	Memory Access	Description
			It has no defined purpose in the Uart. Value After Reset: 0x0 Exists: Always
31:8	RSVD_SCR_31to8	RO	Reserved

7.8.2.13 SRBR0 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0030

Bits	Name	Memory Access	Description
8:0	SRBRn	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this</p>



Bits	Name	Memory Access	Description
			<p>register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBRn	RO	Reserved

7.8.2.14 STHR0 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0030

Bits	Name	Memory Access	Description
8:0	STHRn	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow</p>



Bits	Name	Memory Access	Description
			<p>registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHRn	RO	Reserved



7.8.2.15 SRBR1 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0034

Bits	Name	Memory Access	Description
8:0	SRBR1	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p>



Bits	Name	Memory Access	Description
			If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur. Value After Reset: 0x0
31:9	RSVD_SRBRn	RO	Reserved

7.8.2.16 STHR1 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0034

Bits	Name	Memory Access	Description
8:0	STHR1	WO	<p>Shadow Transmit Holding Register .</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES).</p> <p>If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be</p>



Bits	Name	Memory Access	Description
			<p>written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHRn	RO	Reserved

7.8.2.17 SRBR2 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0038

Bits	Name	Memory Access	Description
8:0	SRBR2	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES).</p> <p>If shadow</p>



Bits	Name	Memory Access	Description
			<p>registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:9	RSVD_SRBRn	RO	Reserved

7.8.2.18 STHR2 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0038

Bits	Name	Memory Access	Description
8:0	STHR2	WO	<p>Shadow Transmit Holding Register .</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR</p>



			<p>before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHRn	RO	Reserved

7.8.2.19 SRBR3 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x003C

Bits	Name	Memory Access	Description
8:0	SRBR3	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations</p>



Bits	Name	Memory Access	Description
			<p>so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBRn	RO	Reserved

7.8.2.20 STHR3 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x003C

Bits	Name	Memory Access	Description
8:0	STHR3	WO	Shadow Transmit Holding Register . This register is valid only when the Uart



Bits	Name	Memory Access	Description
			<p>is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:9	RSVD_STHRn	RO	Reserved

7.8.2.21 SRBR4 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0040

Bits	Name	Memory Access	Description
8:0	SRBR4	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before</p>

			<p>the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.22 STHR4 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0040

Bits	Name	Memory Access	Description
8:0	STHR4	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in</p>



Bits	Name	Memory Access	Description
			<p>infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full.</p> <p>The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.23 SRBR5 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0044

Bits	Name	Memory Access	Description
8:0	SRBR5	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow</p>



Bits	Name	Memory Access	Description
			<p>registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved



7.8.2.24 STHR5 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0044

Bits	Name	Memory Access	Description
8:0	STHR5	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data</p>



			when the FIFO is full results in the write data being lost. The 9th bit is applicable only when LCR_EXT[3]=1. Value After Reset: 0x0
31:9	RSVD_ STHR	RO	Reserved

7.8.2.25 SRBR6 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0048

Bits	Name	Memory Access	Description
8:0	SRBR6	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero),</p>



Bits	Name	Memory Access	Description
			<p>the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.26 STHR6 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0048

Bits	Name	Memory Access	Description
8:0	STHR6	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations</p>



Bits	Name	Memory Access	Description
			<p>so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.27 SRBR7 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x004C



Bits	Name	Memory Access	Description
8:0	SRBR7	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:9	RSVD_SRBR	RO	Reserved

7.8.2.28 STHR7 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x004C

Bits	Name	Memory Access	Description
8:0	STHR7	WO	<p>Shadow Transmit Holding Register .</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR</p>



Bits	Name	Memory Access	Description
			<p>before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full.</p> <p>The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.29 SRBR8 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0050

Bits	Name	Memory Access	Description
8:0	SRBR8	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented,</p>

Bits	Name	Memory Access	Description
			<p>this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.30 STHR8 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0050



Bits	Name	Memory Access	Description
8:0	STHR8	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p>



Bits	Name	Memory Access	Description
			Value After Reset: 0x0
31:9	RSVD_STHR	RO	Reserved

7.8.2.31 SRBR9 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0054

Bits	Name	Memory Access	Description
8:0	SRBR9	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p>



Bits	Name	Memory Access	Description
			<p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.32 STHR9 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0054

Bits	Name	Memory Access	Description
8:0	STHR9	WO	<p>Shadow Transmit Holding Register .</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p>

Bits	Name	Memory Access	Description
			<p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.33 SRBR10 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0058



Bits	Name	Memory Access	Description
8:0	SRBR10	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:9	RSVD_SRBR	RO	Reserved

7.8.2.34 STHR10 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0058

Bits	Name	Memory Access	Description
8:0	STHR10	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR</p>



Bits	Name	Memory Access	Description
			<p>before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full.</p> <p>The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.35 SRBR11 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x005C

Bits	Name	Memory Access	Description
8:0	SRBR11	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented,</p>



Bits	Name	Memory Access	Description
			<p>this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.36 STHR11 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x005C



Bits	Name	Memory Access	Description
8:0	STHR11	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p>



Bits	Name	Memory Access	Description
			Value After Reset: 0x0
31:9	RSVD_STHR	RO	Reserved

7.8.2.37 SRBR12 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0060

Bits	Name	Memory Access	Description
8:0	SRBR12	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p>



Bits	Name	Memory Access	Description
			<p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.38 STHR12 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0060

Bits	Name	Memory Access	Description
8:0	STHR12	WO	<p>Shadow Transmit Holding Register.</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p>



Bits	Name	Memory Access	Description
			<p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.39 SRBR13 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0064



Bits	Name	Memory Access	Description
8:0	SRBR13	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared. If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:9	RSVD_SRBR	RO	Reserved

7.8.2.40 STHR13 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0064

Bits	Name	Memory Access	Description
8:0	STHR13	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR</p>



Bits	Name	Memory Access	Description
			<p>before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.41 SRBR14 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x0068

Bits	Name	Memory Access	Description
8:0	SRBR14	RO	<p>Shadow Receive Buffer Register</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented,</p>

Bits	Name	Memory Access	Description
			<p>this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.42 STHR14 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x0068



Bits	Name	Memory Access	Description
8:0	STHR14	WO	<p>Shadow Transmit Holding Register . This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p>



Bits	Name	Memory Access	Description
			Value After Reset: 0x0
31:9	RSVD_STHR	RO	Reserved

7.8.2.43 SRBR15 (Shadow Receive Buffer Register)

Size: 32 bits

Offset: 0x006C

Bits	Name	Memory Access	Description
8:0	SRBR15	RO	<p>Shadow Receive Buffer Register This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p> <p>If shadow registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p>



Bits	Name	Memory Access	Description
			<p>If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it will be overwritten, resulting in an overrun error.</p> <p>If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO.</p> <p>If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO will be preserved but any incoming data will be lost. An overrun error will also occur.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_SRBR	RO	Reserved

7.8.2.44 STHR15 (Shadow Transmit Holding Register)

Size: 32 bits

Offset: 0x006C

Bits	Name	Memory Access	Description
8:0	STHR15	WO	<p>Shadow Transmit Holding Register.</p> <p>This register is valid only when the Uart is configured to have additional shadow registers implemented (SHADOW = YES). If shadow registers are not implemented, this register does not exist, and reading from this register address returns 0.</p> <p>This register can be accessed only when the DLAB bit (LCR[7]) is cleared.</p>

Bits	Name	Memory Access	Description
			<p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If in non-FIFO mode or FIFO's are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If in FIFO mode and FIFO's are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p>The 9th bit is applicable only when LCR_EXT[3]=1.</p> <p>Value After Reset: 0x0</p>
31:9	RSVD_STHR	RO	Reserved

7.8.2.45 FAR (FIFO Access Register)

Size: 32 bits

Offset: 0x0070



Bits	Name	Memory Access	Description
0	FAR	RW	<p>Writes will have no effect when FIFO_ACCESS == No, always readable.</p> <p>This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFO's are implemented and enabled.</p> <p>When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFO's are treated as empty.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): FIFO access mode disabled 0x1 (ENABLED): FIFO access mode enabled <p>Value After Reset: 0x0</p>
31:1	RSVD_FAR_31to1	RO	Reserved

7.8.2.46 TFR (Transmit FIFO Read)

Size: 32 bits

Offset: 0x0074

Bits	Name	Memory Access	Description
7:0	TFR	RO	<p>Transmit FIFO Read.</p> <p>These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one).</p> <p>When FIFO's are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive</p>



Bits	Name	Memory Access	Description
			read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFO's are not implemented or not enabled, reading this register gives the data in the THR. Value After Reset: 0x0
31:8	RSVD_TFR_31to8	RO	Reserved

7.8.2.47 RFW (Receive FIFO Write)

Size: 32 bits

Offset: 0x0078

Bits	Name	Memory Access	Description
7:0	RFWD	WO	Receive FIFO Write Data. Exists: <u>FIFO_ACCESS == 1</u> These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFO's are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFO's are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR. Value After Reset: 0x0 Exists: Always
8	RFPE	WO	Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFO's are implemented and enabled, this bit is used to write parity error detection



Bits	Name	Memory Access	Description
			<p>information to the receive FIFO. When FIFO's are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Parity error disabled 0x1 (ENABLED): Parity error enabled <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
9	RFFE	WO	<p>Receive FIFO Framing Error.</p> <p>These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one).</p> <p>When FIFO's are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFO's are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Frame error disabled 0x1 (ENABLED): Frame error enabled <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
31:10	RSVD_RFW_31to10	RO	Reserved

7.8.2.48 USR (UART Status register)

Size: 32 bits

Offset: 0x007C

Bits	Name	Memory Access	Description
0	BUSY	RO	UART Busy. This bit is only valid when



Bits	Name	Memory Access	Description
			<p>UART_16550_COMPATIBLE == NO. This indicates that a serial transfer is in progress, when cleared indicates that the Uart is idle or inactive. This bit will be set to 1 (busy) under any of the following conditions:</p> <ul style="list-style-type: none"> - Transmission in progress on serial interface - Transmit data present in THR, when FIFO access mode is not being used (FAR = 0) and the baud divisor is non-zero ($\{DLH,DLL\}$ does not equal 0) when the divisor latch access bit is 0 (LCR.DLAB = 0) - Reception in progress on the interface - Receive data present in RBR, when FIFO access mode is not being used (FAR = 0) <p>Values:</p> <ul style="list-style-type: none"> 0x0 (IDLE): Uart is idle or inactive 0x1 (BUSY): Uart is busy (actively transferring data) <p>Value After Reset: 0x0</p> <p>Volatile: true</p>
1	TFNF	RO	<p>Transmit FIFO Not Full.</p> <p>This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is not full. This bit is cleared when the TX FIFO is full.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (FULL): Transmit FIFO is full 0x1 (NOT_FULL): Transmit FIFO is not full <p>Value After Reset: 0x1</p> <p>Volatile: true</p>
2	TFE	RO	<p>Transmit FIFO Empty.</p> <p>This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. This bit is cleared when the TX FIFO is no longer empty.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NOT_EMPTY): Transmit FIFO is not



Bits	Name	Memory Access	Description
			empty 0x1 (EMPTY): Transmit FIFO is empty Value After Reset: 0x1 Volatile: true
3	RFNE	RO	Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. This bit is cleared when the RX FIFO is empty. Values: 0x0 (EMPTY): Receive FIFO is empty 0x1 (NOT_EMPTY): Receive FIFO is not empty Value After Reset: 0x0 Volatile: true
4	RFF	RO	Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. That is: This bit is cleared when the RX FIFO is no longer full. Values: 0x0 (NOT_FULL): Receive FIFO not full 0x1 (FULL): Receive FIFO full Value After Reset: 0x0 Volatile: true
31:5	RSVD_USR_31to5	RO	Reserved

7.8.2.49 TFL (Transmit FIFO Level)

Size: 32 bits

Offset: 0x0080

Bits	Name	Memory Access	Description
6:0	tfl	RO	<p>Transmit FIFO Level</p> <p>TFL register is valid only when the Uart is configured to have additional FIFO status registers implemented (FIFO_STAT = YES).</p> <p>If status registers are not implemented, this register does not exist and reading from this register address returns 0.</p> <p>This indicates the number of data entries in the transmit FIFO.</p> <p>Value After Reset: 0x0</p>
31:7	RSVD_TFL_31to ADDR_WIDTH	RO	Reserved

7.8.2.50 RFL (Transmit FIFO Level)

Size: 32 bits

Offset: 0x0084

Bits	Name	Memory Access	Description
6:0	rfl	RO	<p>Receive FIFO Level.</p> <p>This indicates the number of data entries in the receive FIFO.</p> <p>Value After Reset: 0x0</p>
31:7	RSVD_RFL_31to ADDR_WIDTH	RO	Reserved

7.8.2.51 SRR (Software Reset Register)

Size: 32 bits

Offset: 0x0088



Bits	Name	Memory Access	Description
0	UR	WO	<p>UART Reset. This asynchronously resets the Uart and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains will be reset.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (NO_RESET): No Uart Reset 0x1 (RESET): Uart reset <p>Value After Reset: 0x0</p>
1	RFR	WO	<p>RCVR FIFO Reset.</p> <p>Writes will have no effect when FIFO_MODE == NONE. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO.</p> <p>This resets the control portion of the receive FIFO and treats the FIFO as empty.</p> <p>This will also de-assert the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES).</p> <p>Note that this bit is 'selfclearing' and it is not necessary to clear this bit.</p> <p>Value After Reset: 0x0</p>
2	XFR	WO	<p>XMIT FIFO Reset</p> <p>Writes will have no effect when FIFO_MODE == NONE.</p> <p>This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO.</p> <p>This resets the control portion of the transmit FIFO and treats the FIFO as empty.</p> <p>This will also de-assert the DMA TX request and single signals when additional</p>



Bits	Name	Memory Access	Description
			DMA handshaking signals are selected (DMA_EXTRA = YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit. Value After Reset: 0x0
31:3	RSVD_SRR_31to3	RO	Reserved

7.8.2.52 SRTS (Shadow Request to Send)

Size: 32 bits

Offset: 0x008C

Bits	Name	Memory Access	Description
0	SRTS	RW	Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read modify write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFO's enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold) only when RTC Flow Trigger is disabled; otherwise it is



Bits	Name	Memory Access	Description
			<p>gated by the receiver FIFO almost-full trigger, where 'almost full' refers to two available slots in the FIFO (rts_n is inactive high when above the threshold).</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DEASSERTED): Shadow Request to Send uart_rts_n logic1 0x1 (ASSERTED): Shadow Request to Send uart_rts_n logic0 <p>Value After Reset: 0x0</p>
31:1	RSVD_SRTS_31to1	RO	Reserved

7.8.2.53 SBCR (Shadow Break Control Register)

Size: 32 bits

Offset: 0x0090

Bits	Name	Memory Access	Description
0	SBCB	RW	<p>Shadow Break Control Bit.</p> <p>This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.</p>



Bits	Name	Memory Access	Description
			<p>Values:</p> <p>0x0 (NO_BREAK): No spacing on serial output</p> <p>0x1 (BREAK): Serial output forced to the spacing</p> <p>Value After Reset: 0x0</p>
31:1	RSVD_SBCR_31to1	RO	Reserved

7.8.2.54 SDMAM (Shadow DMA Mode Register)

Size: 32 bits

Offset: 0x0094

Bits	Name	Memory Access	Description
0	SDMAM	RW	<p>Shadow DMA Mode.</p> <p>This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signaling mode used for the <code>dma_tx_req_n</code> and <code>dma_rx_req_n</code> output signals when additional DMA handshaking signals are not selected (<code>DMA_EXTRA == NO</code>). See section 5.9 on page 54 for details on DMA support.</p> <p>Values:</p> <p>0x0 (MODE_0): Mode 0</p> <p>0x1 (MODE_1): Mode 1</p> <p>Value After Reset: 0x0</p>
31:1	RSVD_SDMAM_31to1	RO	Reserved



7.8.2.55 SFE (Shadow FIFO Enable Register)

Size: 32 bits

Offset: 0x0098

Bits	Name	Memory Access	Description
0	SFE	RW	<p>Shadow FIFO Enable.</p> <p>This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFO's. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFO's will be reset.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): FIFOs are disabled 0x1 (ENABLED): FIFOs are enabled <p>Value After Reset: 0x0</p>
31:1	RSVD_SFE_31to1	RO	Reserved

7.8.2.56 SRT (Shadow RCVR Trigger Register)

Size: 32 bits

Offset: 0x009C

Bits	Name	Memory Access	Description
1:0	SRT	RW	<p>Shadow RCVR Trigger.</p> <p>This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the</p>



Bits	Name	Memory Access	Description
			<p>previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt will be generated. It also determines when the dma_rx_req_n signal will be asserted when DMA Mode (FCR[3]) is set to one. Values:</p> <ul style="list-style-type: none"> 0x0 (FIFO_CHAR_1): 1 character in FIFO 0x1 (FIFO_QUARTER_FULL): FIFO 1/4 full 0x2 (FIFO_HALF_FULL): FIFO 1/2 full 0x3 (FIFO_FULL_2): FIFO 2 less than full <p>Value After Reset: 0x0</p> <p>Exists: Always</p>
31:2	RSVD_SRT_31to2	RO	Reserved

7.8.2.57 STET (Shadow TX Empty Trigger Register)

Size: 32 bits

Offset: 0x00A0

Bits	Name	Memory Access	Description
1:0	STET	RW	<p>Shadow TX Empty Trigger.</p> <p>This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. Writes will have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts will be</p>

Bits	Name	Memory Access	Description
			<p>generated when the mode is active.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (FIFO_EMPTY): FIFO empty 0x1 (FIFO_CHAR_2): 2 characters in FIFO 0x2 (FIFO_QUARTER_FULL): FIFO 1/4 full 0x3 (FIFO_HALF_FULL): FIFO 1/2 full <p>Value After Reset: 0x0</p>
31:2	RSVD_STET_31to2	RO	Reserved

7.8.2.58 HTX (Halt TX)

Size: 32 bits

Offset: 0x00A4

Bits	Name	Memory Access	Description
0	HTX	RW	<p>Halt TX.</p> <p>Writes will have no effect when FIFO_MODE == NONE, always readable.</p> <p>This register is used to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFO's are implemented and enabled. Note, if FIFO's are implemented and not enabled the setting of the halt TX register will have no effect on operation.</p> <p>Values:</p> <ul style="list-style-type: none"> 0x0 (DISABLED): Halt Transmission disabled 0x1 (ENABLED): Halt Transmission enabled <p>Value After Reset: 0x0</p>
31:1	RSVD_HTX_31to1	RO	Reserved



7.8.2.59 DMASA (DMA Software Acknowledge Register)

Size: 32 bits

Offset: 0x00A8

Bits	Name	Memory Access	Description
0	DMASA	RO	<p>DMA Software Acknowledge. Writes will have no effect when DMA_EXTRA == No. This register is use to perform DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the uart should clear its request. This will cause the TX request, TX single, RX request and RX single signals to dessert. Note that this bit is 'self-clearing' and it is not necessary to clear this bit.</p> <p>Values: 0x1 (SOFT_ACK): DMA software acknowledge Value After Reset: 0x0</p>
31:1	RSVD_DMASA_31 to1	RO	Reserved

7.8.2.60 DLF (Divisor Latch Fraction Register)

Size: 32 bits

Offset: 0x00C0

Bits	Name	Memory Access	Description
3:0	DLF	RW	<p>Fractional part of divisor. The fractional value is added to integer value set by DLH, DLL. Fractional value is determined by (Divisor Fraction value)/(2^DLF_SIZE). Value After Reset: 0x0</p>



Bits	Name	Memory Access	Description
31:4	RSVD_DLF	RO	Reserved

7.8.2.61 RAR (Receive Address Register)

Size: 32 bits

Offset: 0x00C4

Bits	Name	Memory Access	Description
7:0	RAR	RW	<p>This is an address matching register during receive mode.</p> <p>If the 9-th bit is set in the incoming character then the remaining 8-bits will be checked against this register value. If the match happens then subsequent characters with 9-th bit set to 0 will be treated as data byte until the next address byte is received.</p> <p>Note: - This register is applicable only when 'ADDR_MATCH'(LCR_EXT[1] and 'DLS_E' (LCR_EXT[0]) bits are set to 1. - If UART_16550_COMPATIBLE is configured to 0, then RAR should be programmed only when UART is not busy. - If UART_16550_COMPATIBLE is configured to 0, then RAR can be programmed at any point of the time. However, user must not change this register value when any receive is in progress.</p> <p>Value After Reset: 0x0</p>
31:8	RSVD_RAR_31_to8	RO	Reserved



7.8.2.62 TAR (Transmit Address Register)

Size: 32 bits

Offset: 0x00C8

Bits	Name	Memory Access	Description
7:0	TAR	RW	<p>This is an address matching register during transmit mode.</p> <p>If DLS_E (LCR_EXT[0]) bit is enabled, then Uart will send the 9-bit character with 9-th bit set to 1 and remaining 8-bit address will be sent from this register provided 'SEND_ADDR' (LCR_EXT[2]) bit is set to 1.</p> <p>Note: - This register is used only to send the address. The normal data should be sent by programming THR register. - Once the address is started to send on the uart serial lane, then 'SEND_ADDR' bit will be auto-cleared by the hardware.</p> <p>Value After Reset: 0x0</p>
31:8	RSVD_TAR_31 to8	RO	Reserved

7.8.2.63 LCR_EXT (Line Extended Control Register)

Size: 32 bits

Offset: 0x00CC

Bits	Name	Memory Access	Description
0	DLS_E	RW	<p>Extension for DLS.</p> <p>This bit is used to enable 9-bit data for transmit and receive transfers.</p> <p>Value After Reset: 0x0</p> <p>Exists: Always Volatile: true</p>
1	ADDR_MATCH	RW	<p>Address Match Mode. This bit is used to enable the address match feature during receive.</p> <p>1 = Address match mode; UART IP will</p>



Bits	Name	Memory Access	Description
			<p>wait until the incoming character with 9-th bit set to 1. And further checks to see if the address matches with what is programmed in 'Receive Address Match Register'. If match is found, then subsequent characters will be treated as valid data and Uart starts receiving data.</p> <p>0 = Normal mode; UART will start to receive the data and 9-bit character will be formed and written into the receive RXFIFO.</p> <p>User is responsible to read the data and differentiate b/n address and data.</p> <p>Note: This field is applicable only when DLS_E is set to 1.</p> <p>Value After Reset: 0x0</p> <p>Exists: Always</p> <p>Volatile: true</p>
2	SEND_ADDR	RW	<p>Send address control bit. This bit is used as a control knob for the user to determine when to send the address during transmit mode.</p> <p>1 = 9-bit character will be transmitted with 9-th bit set to 1 and the remaining 8-bits will match to what is being programmed in 'Transmit Address Register'.</p> <p>0 = 9-bit character will be transmitted with 9-th bit set to 0 and the remaining 8-bits will be taken from the TXFIFO which is programmed through 8-bit wide THR/STHR register.</p> <p>Value After Reset: 0x0</p> <p>Exists: UART_9BIT_DATA_EN == 1</p> <p>Volatile: true</p>
3	TRANSMIT_MODE	RW	Transmit mode control bit. This bit is used to control the type of transmit mode during 9-bit data transfers.



Bits	Name	Memory Access	Description
			<p>1: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding Register (STHR) are 9-bit wide.</p> <p>The user needs to ensure that the THR/STHR register is written correctly for address/data.</p> <p>Address: 9th bit is set to 1, Data : 9th bit is set to 0.</p> <p>Note: Transmit address register (TAR) is not applicable in this mode of operation.</p> <p>0: In this mode of operation, Transmit Holding Register (THR) and Shadow Transmit Holding register (STHR) are 8-bit wide.</p> <p>The user needs to program the address into Transmit Address Register (TAR) and data into the THR/STHR register.</p> <p>SEND_ADDR bit is used as a control knob to indicate the uart on when to send the address.</p> <p>Value After Reset: 0x0</p> <p>Exists: Always</p> <p>Volatile: true</p>
31:4	RSVD_LCR_EXT	RO	Reserved

7.8.2.64 UART_PROT_LEVEL (UART Protection level register)

Size: 32 bits

Offset: 0x00D0

Bits	Name	Memory Access	Description
2:0	UART_PROT_LEVEL	RW	Protection level register. Enabling protection on any of its three bits would require a privilege greater than or



Bits	Name	Memory Access	Description
			equal to PPROT signal to gain access to protected registers. Value After Reset: 3'h2 Exists: Always
31:3	RSVD_UART_PROT_LEVEL	RO	Reserved

7.8.2.65 REG_TIMEOUT_RST (Register timeout counter reset value)

Size: 32 bits

Offset: 0x00D4

Bits	Name	Memory Access	Description
3:0	REG_TIMEOUT_RST	RW	This field holds reset value of REG_TIMEOUT counter register. Value After Reset: 8 Volatile: true
31:3	RSVD_REG_TIMEOUT_RST	RO	Reserved

7.8.2.66 CPR (Component Parameter Register)

Size: 32 bits

Offset: 0x00F4

Bits	Name	Memory Access	Description
1:0	APB_DATA_WIDTH	RO	Encoding of APB_DATA_WIDTH configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (APB_8BITS): APB data width is 8 bits■ 0x1 (APB_16BITS): APB data width is 16 bits■ 0x2 (APB_32BITS): APB data width is 32 bits Value After Reset: 2'h2 Exists: Always



Bits	Name	Memory Access	Description
3:2	RSVD_CPR_3to2	RO	CPR 3to2 Reserved bits read as 0. Value After Reset: 0x0 Exists: Always
4	AFCE_MODE	RO	Encoding of AFCE_MODE configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (DISABLED): AFCE mode disabled■ 0x1 (ENABLED): AFCE mode enabled Value After Reset: 0x0 Exists: Always
5	THRE_MODE	RO	Encoding of THRE_MODE configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (DISABLED): THRE mode disabled■ 0x1 (ENABLED): THRE mode enabled Value After Reset: 0x1 Exists: Always
6	SIR_MODE	RO	Encoding of SIR_MODE configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (DISABLED): SIR mode disabled■ 0x1 (ENABLED): SIR mode enabled Value After Reset: 0x0 Exists: Always
7	SIR_LP_MODE	RO	Encoding of SIR_LP_MODE configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (DISABLED): SIR_LP mode disabled■ 0x1 (ENABLED): SIR_LP mode enabled Value After Reset: 0x0 Exists: Always
8	ADDITIONAL_FEAT	RO	Encoding of ADDITIONAL_FEATURES configuration parameter value. Values: <ul style="list-style-type: none">■ 0x0 (DISABLED): Additional features disabled■ 0x1 (ENABLED): Additional features enabled



Bits	Name	Memory Access	Description
			<p>Value After Reset: 0x1 Exists: Always</p>
9	FIFO_ACCESS	RO	<p>Encoding of FIFO_ACCESS configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (DISABLED): FIFO_ACCESS disabled ■ 0x1 (ENABLED): FIFO ACCESS enabled Value After Reset: 0x1 Exists: Always</p>
10	FIFO_STAT	RO	<p>Encoding of FIFO_STAT configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (DISABLED): FIFO_STAT disabled ■ 0x1 (ENABLED): FIFO_STAT enabled Value After Reset: 0x1 Exists: Always</p>
11	SHADOW	RO	<p>Encoding of SHADOW configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (DISABLED): SHADOW disabled ■ 0x1 (ENABLED): SHADOW enabled Value After Reset: 0x1 Exists: Always</p>
12	UART_ADD_ENCODED_PARAMS	RO	<p>Encoding of UART_ADD_ENCODED_PARAMS configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (DISABLED): UART_ADD_ENCODED_PARAMS disabled ■ 0x1 (ENABLED): UART_ADD_ENCODED_PARAMS enabled Value After Reset: 0x1 Exists: Always</p>
13	DMA_EXTRA	RO	<p>Encoding of DMA_EXTRA configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (DISABLED): DMA_EXTRA disabled </p>



Bits	Name	Memory Access	Description
			<ul style="list-style-type: none"> ■ 0x1 (ENABLED): DMA_EXTRA enabled Value After Reset: 0x0 Exists: Always
15:14	RSVD_CPR_15to14	RO	CPR 15to14 Reserved bits read as 0. Value After Reset: 0x0 Exists: Always
23:16	FIFO_MODE	RO	Encoding of FIFO_MODE configuration parameter value. Values: <ul style="list-style-type: none"> ■ 0x0 (FIFO_MODE_0): FIFO mode is 0 ■ 0x1 (FIFO_MODE_16): FIFO mode is 16 ■ 0x2 (FIFO_MODE_32): FIFO mode is 32 ■ 0x4 (FIFO_MODE_64): FIFO mode is 64 ■ 0x8 (FIFO_MODE_128): FIFO mode is 128 ■ 0x10 (FIFO_MODE_256): FIFO mode is 256 ■ 0x20 (FIFO_MODE_512): FIFO mode is 512 ■ 0x40 (FIFO_MODE_1024): FIFO mode is 1024 ■ 0x80 (FIFO_MODE_2048): FIFO mode is 2048 Value After Reset: 0x4 Exists: Always
31:24	RSVD_CPR_31to24	RO	CPR 15to14 Reserved bits read as 0. Value After Reset: 0x0 Exists: Always

7.8.2.67 UCV (UART Component Version)

Size: 32 bits

Offset: 0x00F8



Bits	Name	Memory Access	Description
31:0	UART_Component_Version	RO	ASCII value for each number in the version, followed by *. For example 32_30_31_2A represents the version 2.01* Value After Reset: 32'h3430322a Exists: Always

7.8.2.68 CTR (Component Type Register)

Size: 32 bits

Offset: 0x00FC

Bits	Name	Memory Access	Description
31:0	Peripheral_ID	RO	This register contains the peripherals identification code. Value After Reset: 32'h44570110 Exists: Always

7.9 GPIO registers

7.9.1 List of registers and offset details

Base Address : GPIO_CNTRL_BASE



Register	Offset	Memory Access	Description
GPIO_SWPORTA_DR	0x0	RW	Value After Reset: 0x0 Name: Port A data register Size: 1-32 bits Address Offset: 0x00 Read/Write Access: Read/Write
GPIO_SWPORTA_DDR	0x4	RW	Value After Reset: 0x0 Name: Port A Data Direction Register Size: 1-32 bits Address Offset: 0x04 Read/Write Access: Read/Write
GPIO_SWPORTA_CTL	0x8	RW	Value After Reset: 0x0 Name: Port A data source register Size: 1-32 bits Address Offset: 0x08 Read/Write Access: Read/Write
GPIO_INTEN	0x30	RW	Value After Reset: 0x0 Name: Interrupt enable Register Size: 1-32 bits Address Offset: 0x30 Read/Write Access: Read/Write
GPIO_INTMASK	0x34	RW	Value After Reset: 0x0 Name: Interrupt mask Register Size: 1-32 bits Address Offset: 0x34 Read/Write Access: Read/Write
GPIO_INTTYPE_LEVEL	0x38	RW	Value After Reset: 0x0 Name: Interrupt level Register Size: 1-32 bits Address Offset: 0x38 Read/Write Access: Read/Write
GPIO_INT_POLARITY	0x3c	RW	Value After Reset: 0x0 Name: Interrupt polarity Register Size: 1-32 bits Address Offset: 0x3c Read/Write Access: Read/Write
GPIO_INTSTATUS	0x40	RO	Value After Reset: 0x0 Name: Interrupt status Register Size: 1-32 bits Address Offset: 0x40 Read/Write Access: Read



GPIO_RAW_INTSTATUS	0x44	RO	Value After Reset: 0x0 Name: Raw interrupt status Register Size: 1-32 bits Address Offset: 0x44 Read/Write Access: Read
GPIO_DEBOUNCE	0x48	RW	Value After Reset: 0x0 Name: Debounce enable Register Size: 1-32 bits Address Offset: 0x48 Read/Write Access: Read/Write
GPIO_PORTA_EOI	0x4c	WO	Value After Reset: 0x0 Name: Port A clear interrupt Register Size: 1-32 bits Address Offset: 0x4c Read/Write Access: Write
GPIO_EXT_PORTA	0x50	RO	Value After Reset: 0x0 Name: Port A external port Register Size: 1-32 bits Address Offset: 0x50 Read/Write Access: Read
GPIO_LS_SYNC	0x60	RW	Value After Reset: 0x0 Name: Synchronization level Register Size: 1 bit Address Offset: 0x60 Read/Write Access: Read/Write
GPIO_ID_CODE	0x64	RO	Value After Reset: 0x0 Name: GPIO ID code Register Size: 1-32 bits Address Offset: 0x64 Read/Write Access: Read
GPIO_VER_ID_CODE	0x6c	RO	Value After Reset: 0x3230392a Name: GPIO Component Version Register Size: 32 bits Address Offset: 0x6c Read/Write Access: Read
GPIO_CONFIG_REG2	0x70	RO	Value After Reset: 0x39cf5 Name: GPIO Configuration Register 2 Register Size: 32 bits Address Offset: 0x70 Read/Write Access: Read



GPIO_CONFIG_REG1	0x74	RO	Value After Reset: 0x1f71e2 Name: GPIO Configuration Register 1 Size: 32 bits Address Offset: 0x74 Read/Write Access: Read
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7.9.2 Register definition

7.9.2.1 GPIO_SWPORTA_DR

Size: 32 bits

Offset: 0x0000

Bit #	Type	Name	Comments	Default
31:0	RW	SWPORTA_DR	Values written to this register are output on the I/O signals for Port A if the corresponding data direction bits for Port A are set to Output mode and the corresponding control bit for Port A is set to Software mode. The value read back is equal to the last value written to this register.	0

7.9.2.2 GPIO_SWPORTA_DDR

Size: 32 bits

Offset: 0x0004

Bit #	Type	Name	Comments	Default
31:0	RW	SWPORTA_DDR	Values written to this register independently control the direction of the corresponding data bit in Port A. The default direction can be configured as input or output after system reset through the GPIO_DFLT_DIR_A parameter. 0x0 (IN): Input Direction 0x1 (OUT): Output Direction	0

7.9.2.3 GPIO_SWPORTA_CTL

Size: 32 bits

Offset: 0x0008

Bit #	Type	Name	Comments	Default
31:0	RW	SWPORTA_CTL	The data and control source for a signal can come from either software or hardware; this bit selects	0



Bit #	Type	Name	Comments	Default
			<p>between them. The default source is configurable through the GPIO_DFLT_DIR_A configuration parameter. If GPIO_PORTA_SINGLE_CTL = 0, the register will contain one bit for each bit of the signal. Upon reset in this case, the value of GPIO_DFLT_SRC_A is replicated across all bits of the signal so that all bits power up with the same operating mode. Furthermore, the default source of each bit of the signal can subsequently be changed by writing to the corresponding bit of this register. This register is not available unless GPIO_HW_PORTA = 1.</p> <p>If GPIO_PORTA_SINGLE_CTL = 1, then the reset value is GPIO_DFLT_SRC_A. If GPIO_PORTA_SINGLE_CTL = 0, then the reset value is {GPIO_PWIDTH_A{GPIO_DFLT_SRC_A in each bit}}.</p> <p>The values of this field depends on the size. Individual bit values will indicate whether the data source is hardware or software.</p> <p>0 : Indicates Software mode 1 : Indicates Hardware mode</p>	

7.9.2.4 GPIO_INTEN

Size: 32 bits

Offset: 0x00C0

Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_INTEN	Allows each bit of Port A to be configured for interrupts. By default the generation of interrupts is disabled. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on Port A to become an interrupt; otherwise, Port A operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of Port A if the corresponding data direction register is set to Output or if Port A mode is set to Hardware.	0



Bit #	Type	Name	Comments	Default
			0x0 (DISABLED): Interrupt is disabled 0x1 (ENABLED): Interrupt is enabled	

7.9.2.5 GPIO_INTMASK

Size: 32 bits

Offset: 0x0034

Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_INTMASK	Controls whether an interrupt on Port A can create an interrupt for the interrupt controller by not masking it. By default, all interrupts bits are unmasked. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. The unmasked status can be read as well as the resultant status after masking. 0x0 (DISABLED): Interrupt bits are unmasked 0x1 (ENABLED): Mask interrupt	0

7.9.2.6 GPIO_INTPTYPE_LEVEL

Size: 32 bits

Offset: 0x0038

Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_INTMASK	Controls the type of interrupt that can occur on Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to be level-sensitive; otherwise, it is edge-sensitive. 0x0 (LEVEL_SENSITIVE): Interrupt is level sensitive 0x1 (EDGE_SENSITIVE): Interrupt is edge sensitive	0

7.9.2.7 GPIO_INT_POLARITY

Size: 32 bits

Offset: 0x003C



Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_INT_POLARITY	Controls the polarity of edge or level sensitivity that can occur on input of Port A. Whenever a 0 is written to a bit of this register, it configures the interrupt type to falling-edge or active-low sensitive; otherwise, it is rising-edge or active-high sensitive. 0x0 (ACTIVE_LOW): Active Low polarity 0x1 (ACTIVE_HIGH): Active High polarity	0

7.9.2.8 GPIO_INTSTATUS

Size: 32 bits

Offset: 0x0040

Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_INTSTATUS	Interrupt status of Port A. 0x0 (INACTIVE): Inactive 0x1 (ACTIVE): Active	0

7.9.2.9 GPIO_RAW_INTSTATUS

Size: 32 bits

Offset: 0x0044

Bit #	Type	Name	Comments	Default
31:0	RO	GPIO_RAW_INTSTATUS	Raw interrupt of status of Port A (premasking bits) 0x0 (INACTIVE): Inactive 0x1 (ACTIVE): Active	0

7.9.2.10 GPIO_DEBOUNCE

Size: 32 bits

Offset: 0x0048



Bit #	Type	Name	Comments	Default
31:0	RW	GPIO_DEBOUNCE	Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 0x0 (DISABLED): No debounce 0x1 (ENABLED): Enable debounce	0

7.9.2.11 GPIO_PORTA_EOI

Size: 32 bits

Offset: 0x004C

Bit #	Type	Name	Comments	Default
31:0	WO	GPIO_PORTA_EOI	Controls the clearing of edge type interrupts from Port A. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. All interrupts are cleared when Port A is not configured for interrupts. 0x0 (DISABLED): No interrupt clear 0x1 (ENABLED): Clear Interrupt	0

7.9.2.12 GPIO_EXT_PORTA

Size: 32 bits

Offset: 0x0050

Bit #	Type	Name	Comments	Default
31:0	RO	GPIO_EXT_PORTA	When Port A is configured as Input, then reading this location reads the values on the signal. When the data direction of Port A is set as Output, reading this location reads the data register for Port A.	32' h00 0C0 0F0

7.9.2.13 GPIO_LS_SYNC

Size: 32 bits

Offset: 0x0060



Bit #	Type	Name	Comments	Default
0	RW	GPIO_LS_SYNC	Writing a 1 to this register results in all level-sensitive interrupts being synchronized to pclk_intr. 0x0 (DISABLED): No synchronization to pclk_int (default) 0x1 (ENABLED): Synchronize to pclk_intr	0
31:1	RO	RESERVED		0

7.9.2.14 GPIO_ID_CODE

Size: 32 bits

Offset: 0x0064

Bit #	Type	Name	Comments	Default
31:0	RO	GPIO_ID_CODE	This is a user-specified code that a system can read. It can be used for chip identification, and so on.	0

7.9.2.15 GPIO_VER_ID_CODE

Size: 32 bits

Offset: 0x006C

Bit #	Type	Name	Comments	Default
31:0	RO	GPIO_VER_ID_CODE	ASCII value for each number in the version	32'h3231 332A

7.9.2.16 GPIO_CONFIG_REG2

Size: 32 bits

Offset: 0x0070



Bit #	Type	Name	Comments	Default
4:0	RO	ENCODED_ID_PWIDTH_A	The value of this register is derived from the GPIO_PWIDTH_A configuration parameter.	5'h1F
9:5	RO	ENCODED_ID_PWIDTH_B	The value of this register is derived from the GPIO_PWIDTH_B configuration parameter.	5'h07
14:10	RO	ENCODED_ID_PWIDTH_C	The value of this register is derived from the GPIO_PWIDTH_C configuration parameter.	00111
19:15	RO	ENCODED_ID_PWIDTH_D	The value of this register is derived from the GPIO_PWIDTH_D configuration parameter.	00111
31:20	RO	RESERVED		0

7.9.2.17 GPIO_CONFIG_REG1

Size: 32 bits

Offset: 0x74

Memory Access: R

Value After Reset: 0x1f71f2

Bit #	Type	Name	Comments	Default
1:0	RO	APB_DATA_WIDTH	The value of this register is derived from the GPIO_APB_DATA_WIDTH configuration parameter. 0x0 (APB_8BITS): APB DATA WIDTH is 8 bits 0x1 (APB_16BITS): APB DATA WIDTH is 16 bits 0x2 (APB_32BITS): APB DATA WIDTH is 32 bits	2'b10
3:2	RO	NUM_PORTS	The value of this register is derived from the GPIO_NUM_PORT configuration parameter. 0x0 (NUM_PORTS_1): Number of ports is 1 0x1 (NUM_PORTS_2): Number of ports is 2 0x2 (NUM_PORTS_3): Number of ports is 3 0x3 (NUM_PORTS_4): Number of ports is 4	2'b00
4	RO	PORTA_SINGLE_CTL	The value of this register is derived from the GPIO_PORTA_SINGLE_CTL configuration parameter. 0x0 (DISABLED): PORTA is not controlled from a single source 0x1 (ENABLED): PORTA is controlled from a single source	1'b0



Bit #	Type	Name	Comments	Default
5	RO	PORTB_SINGLE_CTL	The value of this register is derived from the GPIO_PORTB_SINGLE_CTL configuration parameter. 0x0 (DISABLED): PORTB is not controlled from a single source 0x1 (ENABLED): PORTB is controlled from a single source	1'b1
6	RO	PORTC_SINGLE_CTL	The value of this register is derived from the GPIO_PORTC_SINGLE_CTL configuration parameter. 0x0 (DISABLED): PORTC is not controlled from a single source 0x1 (ENABLED): PORTC is controlled from a single source	1'b1
7	RO	PORTD_SINGLE_CTL	The value of this register is derived from the GPIO_PORTD_SINGLE_CTL configuration parameter. 0x0 (DISABLED): PORTD is not controlled from a single source 0x1 (ENABLED): PORTD is controlled from a single source	1'b1
8	RO	HW_PORTA	The value of this register is derived from the GPIO_HW_PORTA configuration parameter. 0x0 (DISABLED): Port A has external, auxiliary hardware signals excluded 0x1 (ENABLED): Port A has external, auxiliary hardware signals included	1'b1
9	RO	HW_PORTB	The value of this register is derived from the GPIO_HW_PORTB configuration parameter. 0x0 (DISABLED): Port B has external, auxiliary hardware signals excluded 0x1 (ENABLED): Port B has external, auxiliary hardware signals included	1'b0
10	RO	HW_PORTC	The value of this register is derived from the GPIO_HW_PORTC configuration parameter. 0x0 (DISABLED): Port C has external, auxiliary hardware signals excluded 0x1 (ENABLED): Port C has external, auxiliary hardware signals included	1'b0
11	RO	HW_PORTD	The value of this register is derived from the GPIO_HW_PORTD configuration parameter. 0x0 (DISABLED): Port D has external, auxiliary hardware signals excluded	1'b0



Bit #	Type	Name	Comments	Default
			0x1 (ENABLED): Port D has external, auxiliary hardware signals included	
12	RO	PORTA_INTR	The value of this register is derived from the GPIO_PORTA_INTR configuration parameter. 0x0 (DISABLED): PORT A is not used as an interrupt source 0x1 (ENABLED): PORT A is required to be used as an interrupt source	1'b1
13	RO	DEBOUNCE	The value of this register is derived from the GPIO_DEBOUNCE configuration parameter. 0x0 (DISABLED): Exclude debounce capability 0x1 (ENABLED): Include debounce capability	1'b1
14	RO	ADD_ENCODED_PARAMS	The value of this register is derived from the GPIO_ADD_ENCODED_PARAMS configuration parameter. 0x0 (DISABLED): Encoded parameters not added 0x1 (ENABLED): Encoded parameters added	1'b1
15	RO	GPIO_ID	The value of this register is derived from the GPIO_ID configuration parameter. 0x0 (DISABLED): GPIO_ID not included 0x1 (ENABLED): GPIO_ID is included	1'b0
20:16	RO	ENCODED_ID_WIDTH	The value of this register is derived from the GPIO_ID_WIDTH configuration parameter.	5'h1F
21	RO	INTERRUPT_BOTH_EDGE_TYPE	The value of this register is derived from the GPIO_INT_BOTH_EDGE configuration parameter 0x0 (DISABLED): Interrupt generation on rising or falling edge 0x1 (ENABLED): Interrupt generation on both rising and falling edge	1'b0
31:22	RO	RESERVED	RSVD_GPIO_CONFIG_REG1 Reserved bits - read as zero	0

7.10 WDT registers

7.10.1 List of registers and offset details

BASE Address : APB_WDT_BASE



Register	Offset	Memory Access	Description
WDT_CR	0x0	RW	Value After Reset: 0x6 Control Register
WDT_TORR	0x4	RW	Value After Reset: 0xf Timeout Range Register
WDT_CCVR	0x8	RO	Value After Reset: 0xffffffff Current Counter Value Register.
WDT_CRR	0xc	WO	Value After Reset: 0x0 Counter Restart Register.
WDT_STAT	0x10	RO	Value After Reset: 0x0 Interrupt Status Register.
WDT_EOI	0x14	RO	Value After Reset: 0x0 Interrupt Clear Register.
WDT_PROT_LEVEL	0x1C	RW	Value After Reset: 0x2 Protection Level Register.
WDT_COMP_PARAM_5	0xe4	RO	Value After Reset: 0xffffffff Component Parameters Register 5
WDT_COMP_PARAM_4	0xe8	RO	Value After Reset: 0x0 Component Parameters Register 4
WDT_COMP_PARAM_3	0xec	RO	Value After Reset: 0xf Component Parameters Register 3
WDT_COMP_PARAM_2	0xf0	RO	Value After Reset: 0xffffffff Component Parameters Register 2
WDT_COMP_PARAM_1	0xf4	RO	Value After Reset: 0x100f0602 Component Parameters Register 1
WDT_COMP_VERSION	0xf8	RO	Value After Reset: 0x3131312a Component Version Register
WDT_COMP_TYPE	0xfc	RO	Value After Reset: 0x44570120 Component Type Register

7.10.2 Register definition

7.10.2.1 WDT_CR

Size: 32 bits

Offset: 0x0000

Bit #	Type	Name	Comments	Default
0	RW	WDT_EN	WDT enable	0
1	RW	RMOD	Response mode	0
4:2	RW	RPL	Reset pulse length	3'h1
31:5	RO	RESERVED	Reserved for future use.	26'h0



WDT_EN:

This bit is used to enable and disable the DW_apb_wdt. When disabled, the counter does not decrement. Thus, no interrupts or system resets are generated. To prevent a software bug from disabling the DW_apb_wdt, once this bit has been enabled, it can be cleared only by a system reset.

0x0 (DISABLED): Watchdog timer disabled

0x1 (ENABLED): Watchdog timer enabled

RMOD:

Selects the output response generated to a timeout.

0x0 (RESET): Generate a system reset

0x1 (INTERRUPT): First generate an interrupt and even if it is cleared by the time a second timeout occurs then generate a system reset

RPL:

This is used to select the number of pclk cycles for which the WDT system reset stays asserted.

The range of values available is 2 to 256 pclk cycles.

0x0 (PCLK_CYCLES_2): 2 pclk cycles

0x1 (PCLK_CYCLES_4): 4 pclk cycles

0x2 (PCLK_CYCLES_8): 8 pclk cycles

0x3 (PCLK_CYCLES_16): 16 pclk cycles

0x4 (PCLK_CYCLES_32): 32 pclk cycles

0x5 (PCLK_CYCLES_64): 64 pclk cycles

0x6 (PCLK_CYCLES_128): 128 pclk cycles

0x7 (PCLK_CYCLES_256): 256 pclk cycles

7.10.2.2 WDT_TORR (Timeout Range Register)

Size: 32 bits

Offset: 0x0004

Bit #	Type	Name	Comments	Default
3:0	RW	TOP	Timeout period.	4'hF
7:4	RO	RSVD_TOP_INIT	Reserved for TOP_INIT	0
31:8	RO	RESERVED	Reserved for future use.	26'h0

TOP:

This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick).

The range of values is limited by the WDT_CNT_WIDTH. If TOP is programmed to select a range that is greater than the counter width, the timeout period is truncated to fit to the counter width. This affects only the non-user specified values as users are limited to these boundaries during configuration.

The range of values available for a 32-bit watchdog counter are:

0-0xff (256 clocks)

1-0x3FF (1024 clocks)

2-0xffff (4K clock)



3-0xf_ffff
 4-0x1f_ffff
 5-0x3f_ffff
 6-0x7f_ffff
 7-0xff_ffff
 8-0x1ff_ffff
 9-0x3ff_ffff
 10-0x7ff_ffff
 11-0xffff_ffff
 12-0x1fff_ffff
 13-0x3fff_ffff
 14-0x7fff_ffff
 15-ffff_ffff [4G clock]

7.10.2.3 WDT_CCVR (Current Counter Value Register)

Size: 32 bits

Offset: 0x0008

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_CCVR	WDT Current Counter Value Register.	32'hFFFFFFF

WDT_CCVR:

This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read, which is relevant when the APB_DATA_WIDTH(32'd32) is less than the counter width.

7.10.2.4 WDT_CRR (Counter Restart Register)

Size: 32 bits

Offset: 0x000C

Bit #	Type	Name	Comments	Default
7:0	RW	WDT_CRR	Counter Restart Register.	8'h0
31:8	RO	RESERVED	Reserved for future use.	26'h0

TOP:

This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

7.10.2.5 WDT_STAT (Interrupt Status Register)

Size: 32 bits

Offset: 0x0010



Bit #	Type	Name	Comments	Default
0	RO	WDT_STAT	Interrupt status register	1'h0
31:1	RO	RESERVED	Reserved for future use.	31'h0

WDT_STAT:

This register shows the interrupt status of the WDT.

0x0 (INACTIVE): Interrupt is inactive

0x1 (ACTIVE): Interrupt is active regardless of polarity

7.10.2.6 WDT_EOI (Interrupt Clear Register)

Size: 32 bits

Offset: 0x0014

Bit #	Type	Name	Comments	Default
0	RO	WDT_EOI	Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter.	1'h0
31:1	RO	RESERVED	Reserved for future use.	31'h0

7.10.2.7 WDT_PROT_LEVEL (WDT Protection level Register),

Size: 32 bits

Offset: 0x001C

Bit #	Type	Name	Comments	Default
2:0	RW	WDT_PROT_LEVEL	Protection level register. Enabling protection on any of its three bits would require a match on the input PPROT signal to gain access to protected registers of the WDT.	3'h2
31:3	RO	RESERVED	Reserved for future use.	31'h0

Note: Below registers are constant read-only registers that contains encoded information about the component's parameter settings. Some of the reset values depend on coreConsultant parameter(s).



7.10.2.8 WDT_COMP_PARAM_5 (Component Parameters Register 5)

Size: 32 bits

Offset: 0x00E4

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_PARAM_5	Upper limit of Timeout Period parameters. The value of this register is derived from the WDT_USER_TOP_* coreConsultant parameters.	32'hffffff ff

7.10.2.9 WDT_COMP_PARAM_4 (Component Parameters Register 4)

Size: 32 bits

Offset: 0x00E8

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_PARAM_4	Upper limit of Initial Timeout Period parameters. The value of this register is derived from the WDT_USER_TOP_INIT_* coreConsultant parameters.	32'h0

7.10.2.10 WDT_COMP_PARAM_3 (Component Parameters Register 3)

Size: 32 bits

Offset: 0x00EC

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_PARAM_3	The value of this register is derived from the WDT_TOP_RST coreConsultant parameter.	32'hF

7.10.2.11 WDT_COMP_PARAM_2 (Component Parameters Register 2)

Size: 32 bits

Offset: 0x00FO

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_PARAM_2	The value of this register is derived from the WDT_RST_CNT coreConsultant parameter.	32'hffff ff



7.10.2.12 WDT_COMP_PARAM_1 (Component Parameters Register 1)

Size: 32 bits

Offset: 0x00F4

Bit #	Type	Name	Comments	Default
0	RO	WDT_ALWAYS_EN	Decides whether WDT is enabled immediately after reset.	0
1	RO	WDT_DFLT_RMOD	The output response mode that is available directly after reset	1
2	RO	WDT_DUAL_TOP	When set to 1, includes a second timeout period that is used for initialization prior to the first kick	0
3	RO	WDT_HC_RMOD	Defines whether the output response mode to be hard coded	0
4	RO	WDT_HC_RPL	Defines whether the reset pulse length to be hard coded or not.	0
5	RO	WDT_HC_TOP	When set to 1, the selected timeout period(s) is set to be hard coded.	0
6	RO	WDT_USE_FIX_TOP	When this setting is 0, the user must define the timeout period range (2^8 to $2^{WDT_CNT_WIDTH} - 1$) using the WDT_USER_TOP	0
7	RO	WDT_PAUSE	Configuration which decides the peripheral to have a pause enable signal (pause) on the interface that can be used to freeze the watchdog counter during pause mode	0
9:8	RO	APB_DATA_WIDTH	Encoded APB data width <i>(APB_DATA_WIDTH == 32) = 2</i>	2'h2
12:10	RO	WDT_DFLT_RPL	The reset pulse length that is available directly after reset	3'h1
15:13	RO	RSVD_15_13	Reserved and read as zero	0
19:16	RO	WDT_DFLT_TOP	The timeout period that is available directly after reset	4'hF
23:20	RO	WDT_DFLT_TOP_INIT	Default Init value in case of dual top mode	0
28:24	RO	WDT_CNT_WIDTH	The Watchdog Timer counter width	5'h10
31:29	RO	RSVD_31_29	Reserved and read as zero	0



WDT_ALWAYS_EN:

Configures the WDT to be enabled from reset. If this setting is 1, the WDT is always enabled and a write to the WDT_EN field (bit 0) of the Watchdog Timer Control Register (WDT_CR) to disable it has no effect.

0x0 (DISABLED): Watchdog timer disabled on reset

0x1 (ENABLED): Watchdog timer enabled on reset

WDT_DFLT_RMOD:

Describes the output response mode that is available directly after reset. Indicates the output response the WDT gives if a zero count is reached; that is, a system reset if equals 0 and an interrupt followed by a system reset, if equals 1. If WDT_HC_RMOD is 1, then default response mode is the only possible output response mode.

0x0 (DISABLED): System reset only

0x1 (ENABLED): Interrupt and system reset

WDT_DUAL_TOP:

When set to 1, includes a second timeout period that is used for initialization prior to the first kick.

0x0 (DISABLED): Second timeout period is not present

0x1 (ENABLED): Second timeout period is present

WDT_HC_RMOD:

Configures the output response mode to be hard coded.

0x0 (PROGRAMMABLE): Output response mode is programmable

0x1 (HARDCODED): Output response mode is hard coded

WDT_HC_RPL:

Configures the reset pulse length to be hard coded.

0x0 (PROGRAMMABLE): Reset pulse length is programmable

0x1 (HARDCODED): Reset pulse length is hardcoded

WDT_HC_TOP:

When set to 1, the selected timeout period(s) is set to be hard coded.

0x0 (PROGRAMMABLE): Timeout period is programmable

0x1 (HARDCODED): Timeout period is hard coded

WDT_USE_FIX_TOP:

When this parameter is set to 1, timeout period range is fixed. The range increments by the power of 2 from 2^{16} to $2^{(WDT_CNT_WIDTH-1)}$. When this parameter is set to 0, the user must define the timeout period range (2^8 to $2^{(WDT_CNT_WIDTH-1)}$) using the WDT_USER_TOP_(i) parameter.

0x0 (USERDEFINED): User must define timeout values

0x1 (PREDEFINED): Use predefined timeout values



WDT_PAUSE:

Configures the peripheral to have a pause enable signal (pause) on the interface that can be used to freeze the watchdog counter during pause mode.

0x0 (DISABLED): Pause enable signal is non existent

0x1 (ENABLED): Pause enable signal is included

APB_DATA_WIDTH:

Width of the APB Data Bus to which this component is attached.

0x0 (APB_8BITS): APB data width is 8 bits

0x1 (APB_16BITS): APB data width is 16 bits

0x2 (APB_32BITS): APB data width is 32 bits

WDT_DFLT_TOP:

Selects the timeout period that is available directly after reset. It controls the reset value of the register. If WDT_HC_TOP is set to 1, then the default timeout period is the only possible timeout period. Can choose one of 16 values.

WDT_DFLT_TOP_INIT:

Describes the initial timeout period that is available directly after reset. It controls the reset value of the register. If WDT_HC_TOP is 1, then the default initial time period is the only possible period.

7.10.2.13 WDT_COMP_VERSION (Component Version register)

Size: 32 bits

Offset: 0x00F8

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_VERSION	The value of this register is derived from the WDT_TOP_RST coreConsultant parameter.	32'h3131312A

7.10.2.14 WDT_COMP_TYPE (Component Type register)

Size: 32 bits

Offset: 0x00FC

Bit #	Type	Name	Comments	Default
31:0	RO	WDT_COMP_TYPE	Designware Component Type number = 0x44_57_01_20. This assigned unique hex value is constant, and is derived from the two ASCII letters "DW" followed by a 16-bit unsigned number.	32'h44570120



7.11 Analog interface registers

7.11.1 List of registers and offset details

BASE Address : APB_ANA_INTF_BASE (0x98_3400)

Register Name	Access Read/Write	Address
ANA_CFG_INTF_CTRL0	Read/Write	0x00
ANA_CFG_INTF_CTRL1	Read/Write	0x04
ANA_CFG_INTF_WR	Read/Write	0x10
ANA_CFG_INTF_RD	Read only	0x14
ANA_DAC_STATUS	Read/Write	0x18
ANA_CFG_REG0	Read/Write	0x20
ANA_CFG_REG1	Read/Write	0x24
ANA_CFG_REG2	Read/Write	0x28
ANA_CFG_REG3	Read/Write	0x2C
ANA_CFG_REG4	Read/Write	0x30
ANA_STA_REG0	Read only	0x40
ANA_STA_REG1	Read only	0x44
ANA_STA_REG2	Read only	0x48
ANA_CFG_REG5	Read/Write	0x4C
ANA_CFG_REG6	Read/Write	0x50
ANA_OVERRIDE_CONTROL_REG	Read/Write	0x54
T_TRM_REG1	Read/Write	0x404
T_TRM_REG2	Read/Write	0x408
T_TRM_REG3	Read/Write	0x40C
T_TRM_REG4	Read/Write	0x410
T_TRM_REG5	Read/Write	0x414
T_TRM_REG6	Read/Write	0x418
T_TRM_REG7	Read/Write	0x41C
T_TRM_REG8	Read/Write	0x420
T_TRM_REG9	Read/Write	0x424
T_TRM_REG10	Read/Write	0x428
T_TRM_REG11	Read/Write	0x42C
T_TRM_REG12	Read/Write	0x430
T_TRM_REG13	Read/Write	0x434
T_TRM_REG14	Read/Write	0x438
T_TRM_REG15	Read/Write	0x43C
T_TRM_REG16	Read/Write	0x440



Register Name	Access Read/Write	Address
T_TRM_REG17	Read/Write	0x444
T_TRM_REG18	Read/Write	0x448
T_TRM_REG19	Read/Write	0x44C
T_TRM_REG20	Read/Write	0x450
T_TRM_REG21	Read/Write	0x454
T_TRM_REG22	Read/Write	0x458
T_TRM_REG23	Read/Write	0x45C
T_TRM_REG24	Read/Write	0x460
T_TRM_REG25	Read/Write	0x464
T_TRM_REG26	Read/Write	0x468
T_TRM_REG27	Read/Write	0x46C
T_TRM_REG28	Read/Write	0x470
T_TRM_REG29	Read/Write	0x474
T_TRM_REG30	Read/Write	0x478
T_TRM_REG31	Read/Write	0x47C
T_TRM_REG32	Read/Write	0x480
T_TRM_REG33	Read/Write	0x484
T_TRM_REG34	Read/Write	0x488
T_TRM_REG35	Read/Write	0x48C
T_TRM_REG36	Read/Write	0x490

7.11.2 DAC Register Definitions

7.11.2.1 ANA_CFG_INTF_CTRL0

Bit #	Type	Name	Comments	Default
4:0	RW	DAC_CLK_RATE	DAC clock divider. If pclk frequency is 200MHz, DAC clock frequency will be 6.25MHz	5'h1f
15:5	RO	RESERVED	RESERVED	11'h0
25:16	RW	DAC_STRB_HI	Number of DAC clock cycles , for which DAC strobe is asserted high.	10'h6f
31:26	RO	RESERVED	RESERVED	6'h0



7.11.2.2 ANA_CFG_INTF_CTRL1

Bit #	Type	Name	Comments	Default
9:0	RW	DAC_SETUP	Number of DAC clock cycles for DAC strobe setup	10'h6f
15:10	RO	RESERVED	RESERVED	6'h0
25:16	RW	DAC_HOLD	Number of DAC clock cycles for DAC strobe hold.	10'h6f
31:26	RO	RESERVED	RESERVED	6'h0

7.11.2.3 ANA_CFG_INTF_WR

Bit #	Type	Name	Comments	Default
15:0	RW	DAC_WDATA	16-bit DAC write data	16'h0
24:16	RW	DAC_ADDR	9-bit DAC address, the first 3 MSBs is for tile select, 6-bit LSBs for block address	9'h0
29:25	RO	RESERVED	RESERVED	5'h0
30	RW	DAC_RD_EN	DAC read enable	1'b0
31	RW	DAC_WR_EN	DAC write enable	1'b0

7.11.2.4 ANA_CFG_INTF_RD

Bit #	Type	Name	Comments	Default
15:0	RO	DAC_RDATA	16-bit DAC read data	16'h0
31:16	RO	RESERVED	RESERVED	16'h0

7.11.2.5 ANA_ERROR_STATUS

Bit #	Type	Name	Comments	Default
0	RW	DAC_DONE	When DAC transaction is done, it is asserted high, can be cleared by FW	1'b0
1	RW	ERROR_STATUS	When FW issues new transaction in case that DAC is busy, assert error. It can be cleared by FW	1'b1
31:2	RO	RESERVED	RESERVED	30'h0



7.11.3 Analog Miscellaneous Register Definitions

7.11.3.1 ANA_CFG_REG0

Bit #	Type	Name	Comments	Default
1:0	RW	MODE_SEL	Mode select bit 00: TM0, normal operation mode 01: TM1, analog block level test through serial interface 1x: TM2, analog BIST mode through serial interface	2'b00
7:2	RW	RESERVED	RESERVED	6'h0
9:8	RW	BOD_TH_SELECT	BOD threshold select	2'b00
10	RW	SEL_TRIM_REG	0 to select flash trim value and 1 to select APB trim value	1'b0
15:11	RO	RESERVED	RESERVED	5'h0
23:16	RW	CM_ANA_CTRL	Not a trim bit, reserved	8'h0
24	RW	MASTER_PD_DAC_E_N_DIG	When low disables all the PD/DAC in the analog block (Tile 0-3). Internal register state is not cleared. When this signal goes HIGH, previous state is restored. AND with EN_ALL_DAC_PD_2P5 pin.	1'b0
31:25	RO	RESERVED	RESERVED	7'h0

7.11.3.2 ANA_CFG_REG1

Bit #	Type	Name	Comments	Default
0	RW	LASER_CUR_CAL_EN	To enable calibration of laser current resistor	1'b0
11:1	RO	RESERVED	RESERVED	11'h0
19:12	RW	T_TILE_MUX_SELECT	Set 1 to observe ADC inputs at PD_DAC tile	8'h0
31:20	RO	RESERVED	RESERVED	12'h0

7.11.3.3 ANA_CFG_REG2

Bit #	Type	Name	Comments	Default
31:0	RW	ANA_CM_CONFIG	Analog CM configuration register	32'h0



7.11.3.4 ANA_CFG_REG3

Bit #	Type	Name	Comments	Default
31:0	RW	T_ANA_CONFIG_3_0	Tile configuration register for Tile 0~3. Bit [7:0] for Tile 0 Bit [15:8] for Tile 1 Bit [23:16] for Tile 2 Bit [31:24] for Tile 3	32'h0

7.11.3.5 ANA_CFG_REG4

Bit #	Type	Name	Comments	Default
31:0	RW	T_ANA_CONFIG_7_4	Tile configuration register for Tile 4~7. Bit [7:0] for Tile 4 Bit [15:8] for Tile 5 Bit [23:16] for Tile 6 Bit [31:24] for Tile 7	32'h0

7.11.3.6 ANA_STA_REG0

Bit #	Type	Name	Comments	Default
31:0	RO	CM_STATUS_READ	Cm status read register	32'h0

7.11.3.7 ANA_STA_REG1

Bit #	Type	Name	Comments	Default
31:0	RO	T_STATUS_READ_3_0	Tile status register. [7:0] for Tile 0 [15:8] for Tile 1 [23:16] for Tile 2 [31:24] for Tile 3	32'h0

7.11.3.8 ANA_STA_REG2

Bit #	Type	Name	Comments	Default
31:0	RO	T_STATUS_READ_4_7	Tile status register. [7:0] for Tile 4 [15:8] for Tile 5 [23:16] for Tile 6 [31:24] for Tile 7	32'h0



7.11.3.9 ANA_CFG_REG5

Bit #	Type	Name	Comments	Default
7:0	RW	CM_INT_TEMPDIODE_EN	Internal temp diode enable	8'h0
11:8	RW	CM_EXT_TEMPDIODE_EN	External temp diode enable	4'h0
13:12	RW	POR_FTH_SELECT	POR falling threshold select	2'h0
31:14	RO	RESERVED	RESERVED	18'h0

7.11.3.10 ANA_CFG_REG6

Bit #	Type	Name	Comments	Default
4:0	RO	RESERVED	RESERVED	5'h0
5	RW	CM_ATEST_BGR_EN	BGR sel enable for ATEST	1'b0
6	RW	CM_ATEST_V2I_EN	Bias sel enable for ATEST	1'b0
7	RW	CM_ATEST_PMON_EN	Process monitor select enable for ATEST	1'b0
8	RW	CM_ATEST_POR_BOD_EN	BOD select enable for ATEST	1'b0
17:9	RO	RESERVED	RESERVED	9'h0
18	RW	RSSI_INT_1K_SEL	RSSI internal 1K resistor select enable	1'b0
19	RW	RSSI_INT_6K_SEL	RSSI internal 6K resistor select enable	1'b0
20	RW	RSSI_CAL_EXTERNAL_SEL	RSSI external cal enable	1'b0
21	RW	RSSI_CAL_INTERNAL_SEL	RSSI internal cal enable	1'b0
24:22	RW	CM_ATEST_SPARE	ATEST spare signals	3'b0
25	RW	CM_ATEST_LDO_EN	ATEST ldo select enable	1'b0
26	RW	CM_ATEST_TEMPDIODE_EN	ATEST temp diode select enable	1'b0
31:27	RW	CM_ATEST	Reserved for ATEST signals	5'h0



7.11.3.11 ANA_OVERRIDE_CONTROL_REG

Bit #	Type	Name	Comments	Default
7:0	RW	OVRD_T_TILE_SELECT	Override values for t_tile_select	8'h0
8	RW	OVRD_EN_T_TILE_SELECT	Override enable for t_tile_select	1'b0
9	RW	OVRD_POR_B_DIG	Override value for por_b_dig	1'b1
10	RW	OVRD_EN_POR_B_DIG	Override enable for por_b_dig	1'b0
31:11	RO	RESERVED	RESERVED	21'h0

7.11.3.12 T_TRIM_REG1

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACREF_TRIM_0	LDAMP_IDACREF_TRIM for Tile 0	16'h0
31:16	RW	T_LDAMP_IDACREF_TRIM_1	LDAMP_IDACREF_TRIM for Tile 1	16'h0

7.11.3.13 T_TRIM_REG2

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACREF_TRIM_2	LDAMP_IDACREF_TRIM for Tile 2	16'h0
31:16	RW	T_LDAMP_IDACREF_TRIM_3	LDAMP_IDACREF_TRIM for Tile 3	16'h0

7.11.3.14 T_TRIM_REG3

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACREF_TRIM_4	LDAMP_IDACREF_TRIM for Tile 4	16'h0
31:16	RW	T_LDAMP_IDACREF_TRIM_5	LDAMP_IDACREF_TRIM for Tile 5	16'h0

7.11.3.15 T_TRIM_REG4

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACREF_TRIM_6	LDAMP_IDACREF_TRIM for Tile 6	16'h0
31:16	RW	T_LDAMP_IDACREF_TRIM_7	LDAMP_IDACREF_TRIM for Tile 7	16'h0



7.11.3.16 T_TRIM_REG5

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBD_IDACREF_TRIM_0	QBD_IDACREF_TRIM for Tile 0	16'h0
31:16	RW	T_QBD_IDACREF_TRIM_1	QBD_IDACREF_TRIM for Tile 1	16'h0

7.11.3.17 T_TRIM_REG6

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBD_IDACREF_TRIM_2	QBD_IDACREF_TRIM for Tile 2	16'h0
31:16	RW	T_QBD_IDACREF_TRIM_3	QBD_IDACREF_TRIM for Tile 3	16'h0

7.11.3.18 T_TRIM_REG7

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBD_IDACREF_TRIM_4	QBD_IDACREF_TRIM for Tile 4	16'h0
31:16	RW	T_QBD_IDACREF_TRIM_5	QBD_IDACREF_TRIM for Tile 5	16'h0

7.11.3.19 T_TRIM_REG8

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBD_IDACREF_TRIM_6	QBD_IDACREF_TRIM for Tile 6	16'h0
31:16	RW	T_QBD_IDACREF_TRIM_7	QBD_IDACREF_TRIM for Tile 7	16'h0

7.11.3.20 T_TRIM_REG9

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_0_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 0	32'h0



7.11.3.21 T_TRIM_REG10

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_0_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 0	32'h0

7.11.3.22 T_TRIM_REG11

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_1_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 1	32'h0

7.11.3.23 T_TRIM_REG12

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_1_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 1	32'h0

7.11.3.24 T_TRIM_REG13

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_2_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 2	32'h0

7.11.3.25 T_TRIM_REG14

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_2_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 2	32'h0

7.11.3.26 T_TRIM_REG15

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_3_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 3	32'h0

7.11.3.27 T_TRIM_REG16

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_ TRIM_3_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 3	32'h0



7.11.3.28 T_TRIM_REG17

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_4_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 4	32'h0

7.11.3.29 T_TRIM_REG18

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_T_RIM_4_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 4	32'h0

7.11.3.30 T_TRIM_REG19

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_5_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 5	32'h0

7.11.3.31 T_TRIM_REG20

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_5_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 5	32'h0

7.11.3.32 T_TRIM_REG21

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_6_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 6	32'h0

7.11.3.33 T_TRIM_REG22

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_6_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 6	32'h0



7.11.3.34 T_TRIM_REG23

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_7_31_0	32-bit LSBs T_RHEAT_IDACLSB_TRIM for Tile 7	32'h0

7.11.3.35 T_TRIM_REG24

Bit #	Type	Name	Comments	Default
31:0	RW	T_RHEAT_IDACLSB_TRIM_7_63_32	32-bit MSBs T_RHEAT_IDACLSB_TRIM for Tile 7	32'h0

7.11.3.36 T_TRIM_REG25

Bit #	Type	Name	Comments	Default
7:0	RW	T_RHEAT_IDACREF_TIM_0	8-bit rheat_idaclsb_trim for Tile 0	8'h0
15:8	RW	T_RHEAT_IDACREF_TIM_1	8-bit rheat_idaclsb_trim for Tile 1	8'h0
23:16	RW	T_RHEAT_IDACREF_TIM_2	8-bit rheat_idaclsb_trim for Tile 2	8'h0
31:24	RW	T_RHEAT_IDACREF_TIM_3	8-bit rheat_idaclsb_trim for Tile 3	8'h0

7.11.3.37 T_TRIM_REG26

Bit #	Type	Name	Comments	Default
7:0	RW	T_RHEAT_IDACREF_TIM_4	8-bit rheat_idaclsb_trim for Tile 4	8'h0
15:8	RW	T_RHEAT_IDACREF_TIM_5	8-bit rheat_idaclsb_trim for Tile 5	8'h0
23:16	RW	T_RHEAT_IDACREF_TIM_6	8-bit rheat_idaclsb_trim for Tile 6	8'h0
31:24	RW	T_RHEAT_IDACREF_TIM_7	8-bit rheat_idaclsb_trim for Tile 7	8'h0



7.11.3.38 Miscellaneous Trim Register 2

Bit #	Type	Name	Comments	Default
5:0	RO	RESERVED	RESERVED	6'h0
13:6	RW	ADC_LDO_TRIM	0.9V LDO trim	8'h0
31:7	RO	RESERVED	RESERVED	25'h0

7.11.3.39 T_TRIM_REG27

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACMSB_TRIM_0	ldamp_idacmsb_trim for Tile 0	16'h0
31:16	RW	T_LDAMP_IDACMSB_TRIM_1	ldamp_idacmsb_trim for Tile 1	16'h0

7.11.3.40 T_TRIM_REG28

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACMSB_TRIM_2	ldamp_idacmsb_trim for Tile 2	16'h0
31:16	RW	T_LDAMP_IDACMSB_TRIM_3	ldamp_idacmsb_trim for Tile 3	16'h0

7.11.3.41 T_TRIM_REG29

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACMSB_TRIM_4	ldamp_idacmsb_trim for Tile 4	16'h0
31:16	RW	T_LDAMP_IDACMSB_TRIM_5	ldamp_idacmsb_trim for Tile 5	16'h0

7.11.3.42 T_TRIM_REG30

Bit #	Type	Name	Comments	Default
15:0	RW	T_LDAMP_IDACMSB_TRIM_6	ldamp_idacmsb_trim for Tile 6	16'h0
31:16	RW	T_LDAMP_IDACMSB_TRIM_7	ldamp_idacmsb_trim for Tile 7	16'h0



7.11.3.43 T_TRIM_REG31

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBDAMP_IDACMS_B_TRIM_0	Idamp_idacmsb_trim for Tile 0	16'h0
31:16	RW	T_QBDAMP_IDACMS_B_TRIM_1	Idamp_idacmsb_trim for Tile 1	16'h0

7.11.3.44 T_TRIM_REG32

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBDAMP_IDACMS_B_TRIM_2	Idamp_idacmsb_trim for Tile 2	16'h0
31:16	RW	T_QBDAMP_IDACMS_B_TRIM_3	Idamp_idacmsb_trim for Tile 3	16'h0

7.11.3.45 T_TRIM_REG33

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBDAMP_IDACM_SB_TRIM_4	Idamp_idacmsb_trim for Tile 4	16'h0
31:16	RW	T_QBDAMP_IDACM_SB_TRIM_5	Idamp_idacmsb_trim for Tile 5	16'h0

7.11.3.46 T_TRIM_REG34

Bit #	Type	Name	Comments	Default
15:0	RW	T_QBDAMP_IDACMS_B_TRIM_6	Idamp_idacmsb_trim for Tile 6	16'h0
31:16	RW	T_QBDAMP_IDACMS_B_TRIM_7	Idamp_idacmsb_trim for Tile 7	16'h0



7.11.4 ADC controller register definition

BASE Address : APB_ADC_CTRL_BASE (0x98_2C00)

7.11.4.1 ADC controller's config register (EXT_ADC_CTRL_CFG 0x00)

ADC controller's config register (0x00)				
Bit #	Type	Name	Comments	Default
0	RW	adc_En	Config bit to bring ADC controller to either Active or Idle mode of operation	1'b0
1	RW	adc_mode	Config bit to run ADC controller in either of two modes. 0→FIFO or in 1→AUTO mode.	1'b0
2	RW	low_linearity	If a linearity lower than 7 bits is acceptable then there is no need to run the SC calibration	1'b0
3	RW	load_cal_coeff	Skip Calibration and load cal coefficients directly	1'b0
4	RW	adc_clk_en	ADC clock enable signal	1'b0
13:5	RW	nof_sampling_cycle_s	minimum sampling_time * fclk (40MHz) clock.	9'd128
17:14	RW	adc_ctrl_int_mask	ADC controller's interrupt mask bits	4'b1111
18	RW	adc_ext_ref_sel	ADC external reference select bit (1 → Select external reference through ADC_REFP pin, 0 → internal reference short ADC_REFP with VSUP_EXT_ADC)	1'b0
19	RW	adc_ldo_bypass_en	ADC avddhv analog supply LDO bypass enable (1 → LDO bypass, apply supply through VSUP_ADC_EXT)	1'b0
31:20	R	RESERVED	Reserved	12'd0



7.11.4.2 ADC IP digital data path control register (ADC_IP_DATA_PATH_CTRL_CFG 0x04)

ADC IP digital data path control register (0x04)				
Bit #	Type	Name	Comments	Default
0	RW	resetz	Reset of the complete block	1'b1
1	RW	resetrz	Reset of the Retention Memory block	1'b1
2	RW	restart	Stops the current conversion and starts a new sampling phase.	1'b0
4:3	RW	selres	Select the ADC resolution mode. <ul style="list-style-type: none"> • 2'b00 → 8-bit mode • 2'b01 → 10-bit mode • 2'b10 → 12-bit mode • 2'b11 → 14-bit mode 	2'b11
5	RW	startscal	Triggers the switched capacitor and offset calibration cycle	1'b0
6	RW	startvscal	Triggers the offset calibration cycle.	1'b0
7	RW	seldiff	Selects the ADC input mode. 1'b0 : single ended, 1'b1 : differential	1'b0
8	RW	soc	Signals start-of-conversion.	1'b0
9	RW	rearm	Rearms the sampling switches	1'b0
14:10	RW	sel	Selects the analog input signal. 5'b00000 : vinp/n0 selected ... 5'b10011 : vinp/n19 selected	5'b00000
31:15	R	RESERVED	Reserved	17'd0



7.11.4.3 ADC IP LDO control config register (ADC_IP_LDO_CTRL_CFG 0x08)

ADC IP LDO control config register (0x08)				
Bit #	Type	Name	Comments	Default
0	RW	enldo	Enables the internal LDO voltage regulator	1'b1
1	RW	selrefldo	Selects the LDO reference voltage. 1'b1 : vrefldo, 1'b0 : dvdd	1'b1
2	RW	selrangeldo	Defines the range for the LDO reference – either dvdd or vrefldo.	1'b0
3	RW	enadc	Enables the ADC. 1'b1 : normal operation, 1'b0 : standby or power down/deep power down modes, depending on enldo and dislvl	1'b1
9:4	RW	adc_vrefldo_ctrl	ADC reference LDO ctrl code (Description)	6'd0
31:10	R	RESERVED	Reserved	22'd0

7.11.4.4 ADC conversion status register (ADC_OUT_RDY_STAT 0x0C)

ADC conversion status register (0x0C)				
Bit #	Type	Name	Comments	Default
13:0	R	adc_result	ADC IP output b[13:0]	14'd0
14	R	eoc	Signals end-of-conversion. When active indicates that the conversion has terminated and the output data is valid.	1'b0
15	R	pg	Indicates that the LDO output voltage is settled - Power good.	1'b0
16	R	adcrdy	Indicates that the ADC is ready to convert	1'b0
31:17	R	RESERVED	Reserved	15'd0

Note 1 : Details are present in ADC IP data sheet.



7.11.4.5 ADC request's status registers (ADC_CTRL_FIFO_CNT_nERROR_STAT 0x10)

ADC request's status register (0x10)				
Bit #	Type	Name	Comments	Default
7:0	R	pend_adc_req_count	Number of pending adc requests waiting in the queue to be served	8'd0
15:8	R	adc_out_yet2be_read	Number of adc out results yet to be read by FW.	8'd0
16	W1C	apb_adc_req_rd_error	adc req can not be read when controller is reading. This bit will be cleared upon writing 1'b1 to it.	1'b0
17	W1C	apb_adc_req_wr_error	adc req can not be written when fifo is full or when controller is reading. This bit will be cleared upon writing 1'b1 to it.	1'b0
18	W1C	apb_adc_out_rd_error	adc_out data can not be read when fifo is empty. This bit will be cleared upon writing 1'b1 to it.	1'b0
19	W1C	apb_adc_out_wr_error	adc out can not be written when ADC controller is in active mode of operation. This bit will be cleared upon writing 1'b1 to it.	1'b0
23:20	R	adc_ctrl_fsm_state	ADC controller's FSM state.	4'd0
31:24	R	RESERVED	Reserved	8'd0



7.11.4.6 ADC sig bufer registers (ADC_SIG_BUFS_CFG_0....127 0x14....0x210)

ADC Request register (0x14....0x210)				
Bit #	Type	Name	Comments	Default
7:0	RW	analog_signal_sel	analog_signal_sel[7:0]	8'd0
12:8	RW	adc_master_mux_sel	adc_master_mux_sel[4:0]	5'd0
15:13	RW	adc_init_exclude_sample	adc_init_exclude_sample[2:0]	3'd0
18:16	RW	adc_avg_depth	adc_avg_depth[2:0]	3'd0
25:19	RW	next_sig_pointer	next_sig_pointer[6:0]	7'd0
30:26	RW	repeat_ntimes_meas	repeat_ntimes_meas[4:0]	5'd0
31	RW	invalid_signal	invalid_signal	1'b0

7.11.4.7 ADC out buffer registers (ADC_OUT_BUF_STAT_0....127 0x214....0x410)

ADC Out register (0x214....0x410)				
Bit #	Type	Name	Comments	Default
13:0	R	sign_adc_out	sign_adc_out[13:0]	14'd0
14	R	conv_done	conv_done	1'b0
15	R	RESERVED	Reserved	1'b0
31:16	R	RESERVED_2	Reserved	16'd0



**7.11.4.8 Decoded analog signal's mux sel override register
 (ADC_DECODED_AFE_OVRDVAL 0x414)**

Decoded analog signal's mux sel override register (0x414)				
Bit #	Type	Name	Comments	Default
7:0	RW	adc_t_tile_mux_en	Decoded master mux sel signal	8'd0
15:8	RW	adc_tile_mux_ctrl	Analog signal's sel signal for each tile 0-7.	8'd0
17:16	RW	adc_cm_mux_en	Decoded cm mux sel signal	2'b00
25:18	RW	adc_cm_mux_ctrl	Analog signal's sel signal for each common block	8'd0
26	RW	adc_ext_sig_muxsel_en	Decoded external signals sel bit	1'b0
30:27	RW	adc_ext_sig_muxsel	Decoded external signal's index from master mux sel signal[3:0].	4'b0000
31	R	RESERVED	Reserved	1'b0



7.11.4.9 ADC controller's override enable register (ADC_DECODED_AFE_OVRDEN 0x418)

ADC controller's Override enable register (0x418)				
Bit #	Type	Name	Comments	Default
0	RW	ovrd_en_adc_t_tile_mux_en	Decoded master mux sel signal	1'b0
1	RW	ovrd_en_adc_tile_mux_ctrl	Analog signal's sel signal for each tile 0-7.	1'b0
2	RW	ovrd_en_adc_cm_mux_en	Decoded cm mux sel signal	1'b0
3	RW	ovrd_en_adc_cm_mux_ctrl	Analog signal's sel signal for each common block	1'b0
4	RW	ovrd_en_adc_ext_sig_muxsel_en	Decoded external signals sel bit	1'b0
5	RW	ovrd_en_adc_ext_sig_muxsel	Decoded external signal's index from master mux sel signal[4:0].	1'b0
31:6	R	RESERVED	Reserved	26'd0



7.12 System controller registers

7.12.1 List of registers and offset details

BASE Address : APB_SYSTEM_BASE

Register Name	Access Read/Write	Address
PMIC ID register (SYS_PMIC_ID)	RO	0x00
System mode register (SYS_MODE_REG)	RO	0x04
System gpio strap register (SYS_GPIO_STRAP_REG)	RW	0x08
SYS_GPIO_PULL_SEL	RW	0X0C
System gpio HW mode debug select (SYS_GPIO_HW_DEBUG_SEL)	RW	0x10
System gpio pullup/down enable (SYS_GPIO_PULL_EN)	RW	0x14
System control register (SYS_CNTRL_REG0)	RW	0x18
System GPIO input enables (SYS_GPIO_INPUT_EN)	RW	0X1C
System interrupt status register (SYS_INT_STA)	RW	0x20
System interrupt mask register (SYS_INT_MASK)	RW	0x24
System status register (SYS_STA0)	RO(Special write)	0x28
System status register (SYS_STA1)	RO	0x2C
System clock disable register (SYS_CLK_DIS)	RW	0x30
System soft reset enable register (SYS_SOFT_RESET_EN)	RW	0x34
System oscillator clock rate (SYS_OSC_CLK_RATE)	RW	0X38
System CHIP mode register (SYS_CHIP_MODE_REG)	RO	0X3C
Glitch control for I3C (SYS_I3C_GLITCH_CTRL_REG)	RW	0X40
Debug port for ANALOG top (SYS_ANA_TOP_DEBUG_REG)	RO	0X44
UART Debug port (SYS_UART_DEBUG_REG)	RO	0X48
I3C Master Debug port (SYS_I3C_MAS_FIRST_DEBUG_REG)	RO	0X4C
I3C Master Debug port (SYS_I3C_MAS_SECOND_DEBUG_REG)	RO	0X50
I3C Slave Debug port (SYS_I3C_SLV_FIRST_DEBUG_REG)	RO	0X54
I3C Slave Debug port (SYS_I3C_SLV_SECOND_DEBUG_REG)	RO	0X58
I2C pad control register (SYS_PI2C33_50_T_DR_MODE)	RW	0X5C



Register Name	Access Read/Write	Address
SPI pad control register (SYS_SPI_PAD)	RW	0X60
Miscellaneous pad control (SYS_MISC_PAD_CTRL_REG)	RW	0X64
I2C glicth filter (SYS_I2C_GLITCH_FILTER_REG)	RW	0X68

7.12.2 Register definition

7.12.2.1 PMIC ID register (SYS_PMIC_ID)

Size: 32 bits

Offset: 0x0000

Bit #	Type	Name	Comments	Default
3:0	RO	PMIC_ID_REV	Indicates the revision of the chip	0
7:4	RO	PMIC_ID_VER	Indicates the version of the chip	8
31:8	RO	PMIC_ID_DEV	Indicates the device ID	0

7.12.2.2 System mode register (SYS_MODE_REG)

Size: 32 bits

Offset: 0x0004

Bit #	Type	Name	Comments	Default
5:0	RO	PMIC_OSC_TRIM	Indicates the trim value of the oscillator, which is stored in the Flash	0
9:6	RO	PMIC_BG_TRIM	Indicates the trim value of the bandgap regulator, which is stored in the Flash	0
13:10	RO	PMIC_V2I_TRIM	Indicates the trim value for V2I, which is stored in the Flash	0
29:14	RO	PMIC_LDO_TRIM	Indicates the trim value for LDO, which is stored in the Flash	0
31:30	RO	PMIC_POR_DELAY_TRIM	Indicates the trim value for POR DELAY, which is stored in the Flash	0



7.12.2.3 System strap register (SYS_GPIO_STRAP_REG)

Size: 32 bits

Offset: 0x0008

Bit #		Type	Name	Comments	Default
0		W1C	PMIC_GPIO0_STRAP	This indicates if the OCD halt is asserted at power on. After digital reset is removed this value can be changed.	0
1		W1C	PMIC_GPIO1_STRAP	This indicates at power on Debug feature is required or not. After dig reset is remove if cleared only some of the GPIO can be used as HW/FW control register.	0
31:2		W1C	PMIC_GPIOx_STRAP	These strap value are not used by hardware. Firmware can use it.	0

7.12.2.4 System GPIO pull up/down register (SYS_GPIO_PULL_SEL)

Size: 32 bits

Offset: 0x000C

Bit #	Type	Name	Comments	Default
31:0	RW	PMIC_GPIO_PU_PD_N_SEL_REG	1'b1 for pull-up and 1'b0 for pull-down, work together with SYS_GPIO_PULL_EN	32'h000C00F0

7.12.2.5 System gpio HW mode debug select (SYS_GPIO_HW_DEBUG_SEL)

Size: 32 bits

Offset: 0x0010

Bit #	Type	Name	Comments	Default
[1:0]	RW	SYS_GPIO_HW_SEL	When the GPIO is enabled for hardware mode, this controls the which internal signals will be output to the GPIO pins. Note : To observe the output PMIC_GPIO0_STRAP=0 (cleared) and gpio_swporta_ctl=1 (HW mode)	2'b00
31:2	R	Reserved		0

SYS_GPIO_HW_SEL:

2'b00: observe adc_data[6:0]

2'b01: observe adc_data[13:7]



Note: Debug observation details

External pin	HW mode (gpio_swporta_ctl=1) and SYS_GPIO_HW_SEL=00		HW mode (gpio_swporta_ctl=1) and SYS_GPIO_HW_SEL=01		HW mode (gpio_swporta_ctl=1) and SYS_GPIO_HW_SEL=10/11 (Not used)	
	Dir	Pin info	Dir	Pin info	Dir	Pin info
GPIO[0]	-	-	-	-	-	-
	out	DAC write strobe	out	DAC write strobe	out	
GPIO[1]	-	-	-	-	-	
	out	ADC EOC	out	ADC EOC	out	
GPIO[2]	-	-	-	-	-	
	out	Divided osc_clk	out	Divided osc_clk	out	-
GPIO[3]	-	-	-	-	-	
	out	Flash_sel_main_mem	out	Flash_sel_main_me m	out	
GPIO[4]	-	-	-	-	-	
	out	WDT reset	out	WDT reset	out	
GPIO[5]	-	-	-	-	-	
	out	Digi reset	out	Digi reset	out	
GPIO[6]	-	-	-	-	-	
	out	Brown out	out	Brown out	out	
GPIO[7]	-	-	-	-	-	
	out	POR	out	POR	out	
GPIO[8]	-	-	-	-	-	
	out	ADC STROBE	out	ADC STROBE	out	
GPIO[9]	-	-	-	-	-	
	out	DAC read strobe	-	DAC read strobe	-	
GPIO[10]	-	-	-	-		
	out	ADC_CLK		ADC_CLK		
GPIO[11]	-	-	-	-	-	
	out	ADC_DATA[0]	Out	ADC_DATA[7]	out	
GPIO[12]	-	-	-	-	-	
	out	ADC_DATA[1]	out	ADC_DATA[8]	out	
GPIO[13]	-	-	-	-	-	
	out	ADC_DATA[2]	out	ADC_DATA[9]	out	
GPIO[14]	-	-	-	-	-	
	out	ADC_DATA[3]	out	ADC_DATA[10]	out	
GPIO[15]	-	-	-	-	-	
	out	ADC_DATA[4]	out	ADC_DATA[11]	out	
GPIO[16]	-	-	-	-	-	
	out	ADC_DATA[5]	out	ADC_DATA[12]	out	
GPIO[17]	-	-	-	-	-	
	out	ADC_DATA[6]	out	ADC_DATA[13]	out	



7.12.2.6 System gpio pullup/down enable (SYS_GPIO_PULL_EN)

Size: 32 bits

Offset: 0x0014

Bit #	Type	Name	Comments	Default
[31:0]	RW	SYS_GPIO_PULL_EN	When set the internal on-chip pull up/down feature of the GPIO is enabled. When zero the pull up/down is disabled.	32'h000F00FF

7.12.2.7 System control register (SYS_CNTRL_REG0)

Size: 32 bits

Offset: 0x0018

Bit #	Type	Name	Comments	Default
0	RW	SYS_FLASH_V_OK_EN	When this bit is set the flash voltage ok signal can be written by the FW	1'b0
1	RW	SYS_BOD_INT_TYPE	Indicates if the interrupt to the micro controller is level or pulse. 1- Level interrupt 0 - Pulse interrupt	1'b0
3:2	R	Reserved		
5:4	RW	SYS_BOD_GEN_TYPE	Indicates when the interrupt needs to be generated for brownout detection. 2'b00 : Interrupt generated for both assertion and de-assertion . 2'b01 : Interrupt generated for only de-assertion 2'b11 : Interrupt generated for only assertion	2'b00
31:6	R	Reserved		0

7.12.2.8 System gpio Input enable (SYS_GPIO_IE)

Size: 32 bits

Offset: 0x001C

Bit #	Type	Name	Comments	Default
[31:0]	RW	SYS_GPIO_IE	GPIO input enables	32'hfffffff



7.12.2.9 System interrupt status register (SYS_INT_STA)

Size: 32 bits

Offset: 0x0020

Bit #	Type	Name	Comments	Default
0	W1C	SYS_BOD_INT_STA	Indicates that the brownout reset occurred.	1'b0
31:1	R	Reserved		

7.12.2.10 System interrupt unmask register (SYS_INT_MASK)

Size: 32 bits

Offset: 0x0024

Bit #	Type	Name	Comments	Default
0	RW	SYS_BOD_INT_UNMASK	1 – The interrupt is un masked. 0 – The interrupt is masked	1'b0
31:2	R	Reserved		

7.12.2.11 System status register (SYS_STA0)

Size: 32 bits

Offset: 0x0028

Bit #	Type	Name	Comments	Default
0	RW	SYS_FLASH_V_OK_STA	1 – Indicates the flash voltage is ok. Set before the digital power on reset is removed. Write 0 : If SYS_FLASH_V_OK_EN is enabled the flash ok is cleared. Write 1 : If SYS_FLASH_V_OK_EN is enabled the flash ok is set.	1'b1
31:1	R	Reserved		0

7.12.2.12 System status register (SYS_STA1)

Size: 32 bits

Offset: 0x002C

Bit #	Type	Name	Comments	Default
0	R	SYS_BOD_B_STA	0 – Indicates the brownout condition occurred. 1 – Indicates the brownout did not occur	1' b1
31:1	R	Reserved		0



7.12.2.13 System clock disable register (SYS_CLK_DIS)

Size: 32 bits

Offset: 0x0030

Bit #	Type	Name	Comments	Default
0	RW	SYS_FLASH_CLK_DIS	The flash controller clock can be disabled. This would result in the removal of clock to flash controller 1 – disable the clock 0 – enable the clock	1'b 0
1	RW	SYS_ANA_CNTRL_CLK_DIS	The I2C and GPIO block clock can be disabled. 1 – disable the clock 0 – enable the clock	1'b 0
6:2	RW	SYS_I2C_MAS_CLK_DIS	I2C master APB clock disable, Bit[2] for I2C_MAS[0] and BIT[6] for I2C_MAS[4] 1–disable the clock 0 –enable the clock	5'h 00
9:7	RW	SYS_I2C_SLV_CLK_DIS	I2C slave APB clock disable, Bit[7] for I2C_SLV[0], BIT[8] for I2C_SLV[1] and I2C_DBG, and BIT[9] for I2C_SLV[2] 1 – disable the clock 0 – enable the clock	3'h 0
10	RW	SYS_I3C_MAS_CLK_DIS	I3C master APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
11	RW	SYS_I3C_SLV_CLK_DIS	I3C slave APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
12	RW	SYS_GPIO_CLK_DIS	GPIO APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
13	RW	SYS_UART_CLK_DIS	UART APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
14	RW	SYS_SPI_CLK_DIS	SPI APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
15	RW	SYS_MDIO_CLK_DIS	MDIO APB clock disable 1 – disable the clock 0 – enable the clock	1'b 0
31:16	R	Reserved		

7.12.2.14 System soft reset enable register (SYS_SOFT_RESET_EN)

Size: 32 bits

Offset: 0x0034

Bit #	Type	Name	Comments	Default
0	RW	SYS_FLASH_RESET	The flash controller is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
1	RW	SYS_ANA_CNTRL_RESET	The analog controller is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
2	RW	SYS_EXT_GPIO_RESET	The GPIO block is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
3	RW	SYS_ADC_CNTRL_RESET	The ADC controller block is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
4	RW	SYS_EXT_SPI_RESET	The SPI block is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
9:5	RW	SYS_EXT_I2C_M_RESET[4:0]	The I2C master are under reset. It's a vector signal , connected to each master. 1 – soft reset is enabled 0 – Not under soft reset	0
12:10	RW	SYS_EXT_I2C_S_RESET[2:0]	The I2C slave are under reset. It's a vector signal, connected to each I2C slaves. 1 – soft reset is enabled 0 – Not under soft reset	0
13	RW	SYS_EXT_I3C_M_RESET	The I3C master controller is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
14	RW	SYS_EXT_I3C_S_RESET	The I3C slave controller is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
15	RW	MDIO_RESET	The MDIO block is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
16	RW	SYS_EXT_UART_RESET	The UART block is under reset. 1 – soft reset is enabled 0 – Not under soft reset	0
31:17	RO	Reserved		0



7.12.2.15 System OSC clock rate (SYS_OSC_CLK_RATE)

Size: 32 bits

Offset: 0x0038

Bit #	Type	Name	Comments	Default
1:0	RW	SYS_OSC_CLK_RATE	OSC clock rate 0 - the frequency of the observed osc clock is the same as osc_clk 1 - the frequency of the observed osc clock is 1/2 of osc_clk 2 - the frequency of the observed osc clock is 1/4 of osc_clk 3 - the frequency of the observed osc clock is 1/8 of osc_clk	2'b 11
9:2	RW	ADC_CLK_RATE	ADC Clock rate	8'h 05
31:1	RO	Reserved		0

7.12.2.16 System chip mode register (SYS_CHIP_MODE_REG)

Size: 32 bits

Offset: 0x003C

Bit #	Type	Name	Comments	Default
2:0	RO	PMIC_CHIP_MODE	Indicates the chip mode of operation	0
31:3	RO	Reserved		0

7.12.2.17 Glitch filter control for DW I3C (SYS_I3C_GLITCH_CTRL_REG)

Size: 32 bits

Offset: 0x0040



Bit #	Type	Name	Comments	Default
0	RW	slv_glt_flt_disable	control to bypass the external Glitch filter for instance 'i_DW_apb_i3c_slv'	0
6:1	RW	slv_glt_flt_width	Filter width parameter for instance 'i_DW_apb_i3c_slv'	6'h0A
7	RW	slv_force_i2c	Force I2C mode for instance 'i_DW_apb_i3c_slv'	0
8	RO	slv_wakeup_sts	Address match status for instance 'i_DW_apb_i3c_slv'	0
9	RW	mstr_force_i2c	Force I2C mode for instance 'i_DW_apb_i3c_mas'	0
10	RO	mstr_wakeup_sts	Address match status for instance 'i_DW_apb_i3c_mas'	0
31:11	RO	Reserved	RESERVED	0

7.12.2.18 Debug port for Analog top (SYS_ANA_TOP_DEBUG_REG)

Size: 32 bits

Offset: 0x0044

Bit #	Type	Name	Comments	Default
7:0	RO	adc_t_tile_mux_en_o	status for ANA TOP debug port	8'h01
15:8	RO	adc_tile_mux_ctrl_o		0
17:16	RO	adc_cm_mux_en_o		0
25:18	RO	adc_cm_mux_ctrl_o		0
26	RO	adc_ext_sig_muxsel_en_o		0
30:27	RO	adc_ext_sig_muxsel_o		4'h6
31	RO	POR_B_DIG		1'b1

7.12.2.19 Debug port for UART (SYS_UART_DEBUG_REG)

Size: 32 bits

Offset: 0x0048

Bit #	Type	Name	Comments	Default
31:0	RO	debug_uart	status for debug UART port	0



7.12.2.20 Debug port for I3C master (SYS_I3C_MAS_FIRST_DEBUG_REG)

Size: 32 bits

Offset: 0x004C

Bit #	Type	Name	Comments	Default
31:0	RO	debug_i3c_mas[31:0]	status for debug I3C master port	32'h8000AAAB

7.12.2.21 Debug port for I3C master (SYS_I3C_MAS_SECOND_DEBUG_REG)

Size: 32 bits

Offset: 0x0050

Bit #	Type	Name	Comments	Default
15:0	RO	debug_i3c_mas[47:32]	status for debug I3C master port	0

7.12.2.22 Debug port for I3C slave (SYS_I3C_SLV_FIRST_DEBUG_REG)

Size: 32 bits

Offset: 0x0054

Bit #	Type	Name	Comments	Default
31:0	RO	debug_i3c_slv[31:0]	status for debug I3C slave port	0

7.12.2.23 Debug port for I3C slave (SYS_I3C_SLV_SECOND_DEBUG_REG)

Size: 32 bits

Offset: 0x0058

Bit #	Type	Name	Comments	Default
15:0	RO	debug_i3c_slv[47:32]	status for debug I3C slave port	0

7.12.2.24 I2C pad control (SYS_PI2C_33_50_T_DR_MODE_REG)

Size: 32 bits

Offset: 0x005C

Bit #	Type	Name	Comments	Default
15:0	RW	pi2c_33_50_t_dr_mode[15:0]	PAD control register for I2C	0



PI2C_33_50_T_DR_MODE[15:0]:

- bit [4:0] PAD mode for i_m_sck_pad_0 ~ i_m_sck_pad_4
- bit [9:5] PAD mode for i_m_sda_pad_0 ~ i_m_sck_pad_4
- bit [10] PAD mode for i_s_sck_pad
- bit [11] PAD mode for i_s_sda_pad
- bit [12] PAD mode for i_m_sck_i3c_pad
- bit [13] PAD mode for i_m_sda_i3c_pad
- bit [14] PAD mode for i_s_sck_i3c_pad
- bit [15] PAD mode for i_s_sda_i3c_pad

7.12.2.25 SPI pad control (SYS_SPI_PAD_CTRL_REG)

Size: 32 bits

Offset: 0x0060

Bit #	Type	Name	Comments	Default
20:0	RW	spi_pad_ctrl_reg[20:0]	PAD control register for SPI	0
31:21	RO	RESERVED		0

PI2C_33_50_T_DR_MODE[15:0]:

- [0]: pu_pdn_ctrl for SCLK_SPI*
- [1]: pu_pdn_ctrl for MOSI_SPI
- [2]: pu_pdn_ctrl for MISO_SPI
- [3]: pu_pdn_ctrl for SSO_SPI
- [4]: pu_pdn_ctrl for SSO_SPI
- [5]: pu_pdn_ctrl for SSO_SPI
- [6]: pu_pdn_ctrl for SSO_SPI
- [7]: pu_pdn_sel for SCLK_SPI
- [8]: pu_pdn_sel for MOSI_SPI
- [9]: pu_pdn_sel for MISO_SPI
- [10]: pu_pdn_sel for SSO_SPI
- [11]: pu_pdn_sel for SSO_SPI
- [12]: pu_pdn_sel for SSO_SPI
- [13]: pu_pdn_sel for SSO_SPI
- [14]: ie for SCLK_SPI
- [15]: ie for MOSI_SPI
- [16]: ie for MISO_SPI
- [17]: ie for SSO_SPI
- [18]: ie for SSO_SPI
- [19]: ie for SSO_SPI
- [20]: ie for SSO_SPI

*Note: When SPI master is idle and spi_oe is deasserted, SPI PADs are set as HiZ by the default value, pu_pdn_ctrl='0



7.12.2.26 Miscellaneous pad control (SYS_MISC_PAD_CTRL_REG)

Size: 32 bits

Offset: 0x0064

Bit #	Type	Name	Comments	Default
30:0	RW	misc_pad_ctrl_reg[30:0]	control register for PAD	31'hC0000000
31	RO	RESERVED		0

PI2C_33_50_T_DR_MODE[15:0]:

- [0]: uart_rx_pu_pdn_ctrl
- [1]: uart_rx_pu_pdn_sel
- [2]: uart_rx_oe
- [3]: uart_rx_ie
- [4]: uart_tx_pu_pdn_ctrl
- [5]: uart_tx_pu_pdn_sel
- [6]: uart_tx_oe
- [7]: uart_tx_ie
- [8]: mdio_clk_pu_pdn_ctrl
- [9]: mdio_clk_pu_pdn_sel
- [10]: mdio_clk_oe
- [11]: mdio_clk_ie
- [12]: mdio_data_pu_pdn_ctrl
- [13]: mdio_data_pu_pdn_sel
- [14]: mdio_data_ie
- [15]: i3c_slv_sda_ie
- [16]: i3c_slv_sck_ie
- [17]: i3_mas_sda_ie
- [18]: i3_mas_sck_ie
- [23:19]: i2c_mas_sck_ie[4:0]
- [28:24]: i2c_mas_sda_ie[4:0]
- [29]: i2c_slv_sck_ie
- [30]: i2c_slv_sda_ie

7.12.2.27 I2C glitch filter register (SYS_I2C_GLITCH_FILTER_REG)

Size: 32 bits

Offset: 0x0068



Bit #	Type	Name	Comments	Default
4:0	RW	i2cm_sda_gf_disable	Control to enable or disable the glitch filter on I2C master SDA lines [0] - External Glitch filter enabled [1] - External Glitch filter disabled	0
9:5	RW	i2cm_scl_gf_disable	Control to enable or disable the glitch filter on I2C master SCL lines [0] - External Glitch filter enabled [1] - External Glitch filter disabled	0
13:10	RW	i2cs_sda_gf_disable	Control to enable or disable the glitch filter on I2C slave SDA lines [0] - External Glitch filter enabled [1] - External Glitch filter disabled	4' h 8
17:14	RW	i2cs_scl_gf_disable	Control to enable or disable the glitch filter on I2C slave SCL lines [0] - External Glitch filter enabled [1] - External Glitch filter disabled	4' h 8
23:18	RW	i2c_gf_width	I2C external digital glitch filter width	6' 0 A
31:24	RO	RESERVED		



8 Version History

Table 27 : Version History

Version	Date	Comment
0.1	15 th July, 2019	Initial version
0.2	25 th August, 2019	Updated all analog/digital specs and reformatted for initial release
0.21	29 th August, 2019	ESD for external supply monitoring pin are excluded, resolution of LD, QBD and FS range update for all DACs
0.22	April 2, 2021	Added FCCSP information
0.3	September 1, 2022	Formatted into initial customer release
0.4	June 28, 2023	Added register description

9 Part Number Ordering Information

Table 28: Part Numbers and Descriptions

Part Number	Description
SPTEMZZZFB1DF	Intel® Silicon Photonics Power Management and Control IC with Expanded Memory, Version DF