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Computer Architecture Lab (Week 3)

Decimal Number

- ❑ Converting decimal number to binary number and hexadecimal numbe
- ❑ 57
- ❑ 143
- ❑ 76
- ❑ 223
- ❑ 90

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Hexadecimal Number

- ❑ Converting hexadecimal number to binary number and decimal numbe
- ❑ 57H
- ❑ 143H
- ❑ 76H
- ❑ 223H
- ❑ 90H

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Binary Number

- Converting binary number to decimal number and hexadecimal numbe
- 11111100
- 00111100
- 1111000000001111
- 10101100
- 0011001100001111

Opcode	Operand	Description
RAR	None	Rotate accumulator right through carry

- Each binary bit of the accumulator is rotated right by one position through the Carry flag.
- Bit Do is placed in the Carry flag, and the Carry flag is placed in the most significant position D7.
- CY is modified according to bit Do.
- S, Z, P, AC are not affected.
- **Example:** RAR.

Opcode	Operand	Description
RAL	None	Rotate accumulator left through carry

- Each binary bit of the accumulator is rotated left by one position through the Carry flag.
- Bit D7 is placed in the Carry flag, and the Carry flag is placed in the least significant position Do.
- CY is modified according to bit D7.
- S, Z, P, AC are not affected.
- **Example:** RAL.

Opcode	Operand	Description
RLC	None	Rotate accumulator left

- Each binary bit of the accumulator is rotated left by one position.
- Bit D7 is placed in the position of Do as well as in the Carry flag.
- CY is modified according to bit D7.
- S, Z, P, AC are not affected.
- **Example:** RLC.

Opcode	Operand	Description
RRC	None	Rotate accumulator right

- Each binary bit of the accumulator is rotated right by one position.
- Bit Do is placed in the position of D7 as well as in the Carry flag.
- CY is modified according to bit Do.
- S, Z, P, AC are not affected.
- **Example:** RRC.

Arithmetic Instructions

Opcode	Operand	Description
INR	R M	Increment register or memory by 1

- The contents of register or memory location are incremented by 1.
- The result is stored in the same place.
- If the operand is a memory location, its address is specified by the contents of H-L pair.
- **Example:** INR B or INR M

Arithmetic Instructions

Opcode	Operand	Description
INX	R	Increment register pair by 1

- The contents of register pair are incremented by 1.
- The result is stored in the same place.
- **Example:** INX H

Jump Conditionally

Opcode	Description	Status Flags
JC	Jump if Carry	CY = 1
JNC	Jump if No Carry	CY = 0
JP	Jump if Positive	S = 0
JM	Jump if Minus	S = 1
JZ	Jump if Zero	Z = 1
JNZ	Jump if No Zero	Z = 0
JPE	Jump if Parity Even	P = 1
JPO	Jump if Parity Odd	P = 0

Data Transfer Instructions

Opcode	Operand	Description
PUSH	Reg. pair	Push register pair onto stack

- The contents of register pair are copied onto stack.
- SP is decremented and the contents of high-order registers (B, D, H, A) are copied into stack.
- SP is again decremented and the contents of low-order registers (C, E, L, Flags) are copied into stack.
- **Example:** PUSH B

Data Transfer Instructions

Opcode	Operand	Description
POP	Reg. pair	Pop stack to register pair

- The contents of top of stack are copied into register pair.
- The contents of location pointed out by SP are copied to the low-order register (C, E, L, Flags).
- SP is incremented and the contents of location are copied to the high-order register (B, D, H, A).
- **Example:** POP H

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Flage Register in 8085 Microprocessor

❑ What is Flage in register in 8085 microprocessor?

❖ Flag register includes five flip-flops, which are set or reset after an operation according to the data conditions of the result in the accumulator and other r

❖ The flags register can have a total of eight flags. Thus, a flag can be represen 1 bit of information. But only five flags are implemented in 8085.

D7	D6	D5	D4	D3	D2	D1	D0
S	Z	X	AC	X	P	X	CY

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Flage Register in 8085 Microprocessor

❑ Z (Zero) Flag :

- ❖ This flag indicates whether the result of mathematical or logical operation is zero or not.
- ❖ If the result of the current operation is zero, then this flag will be set, otherwise reset

❑ CY (Carry) Flag :

- ❖ This flag indicates, whether, during an addition or subtraction operation, carry or borrow is generated or not, if generated then this flag bit will be set.

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Flage Register in 8085 Microprocessor

❑ **AC (Auxiliary Carry) Flag:**.

❖ It shows carry propagation from D3 position to D4 position.

❖ AF (Auxiliary carry Flag): It holds the carry (half carry) after addition or borrows after subtraction between bit positions 3 and 4 of the result in a **BCD** operation.

❖ If carry or borrow generated to D3 and to D4, then AC flag is set otherwise reset.

❑ **PF (Parity Flag):**

❖ It is the count of ones in a number expressed as even or odd.

❖ It is logic 0 for even parity (i.e. even number of 1s) and logic 1 for odd parity (i.e. odd number of 1s).

❖ For example, if a number contains three binary passone bits, it has odd parity and if a number contains no one bits, it has even parity.

Flage Register in 8085 Microprocessor

❑ **SF (Sign Flag):**.

❖ It holds the arithmetic sign of the result after arithmetic or logic instruction e

❖ If S = 1, the sign bit (leftmost bit of a number) is set or negative and if S= 0, th

bit is cleared or positive.

TP01: Right shift 4 bits of 8-bits data (shift ri
carry

- **Statement**: Do 4 bits shifting of 8-bits data in memory location 2000H and st
  shifting data to memory location 2001H.
- **Sample Problem**: (2000H) = 5B = 0101 1011 (CY = 0)
- **Result**: (2001H) = 65 = 0110 0101 (CY = 1)

LDA 2000

CMC

RAR

RAR

RAR

RAR

STA 2001

HLT

TP02: Right shift 8 bits of 16-bits data (shif right without carry)

- **Statement**: Do 8 bits shifting of 16-bits data in memory location 2000H an 2001H then store shifting data to memory location 2002H and 2003H.
- **Sample Problem**: (2001H & 2000H) = 04 05 = 0000 0100 0000 0101
- Result: (2003H & 2002H) = 05 04 = 0000 0101 0000 0100

```
LHLD 2000
XCHG
MOV L, D
MOV H, E
SHLD 2002
HLT
```

TP03: Left shift 4 bits of 8-bits data (shift with carry)

- **Statement**: Do 4 bits shifting of 8-bits data in memory location 2000H and store shifting data to memory location 2001H.
- **Sample Problem**: (2000H) = 16 = 0001 0110, CY = 0
- **Result**: (2001H) = 60 = 0110 0000, CY = 1

LDA 2000
RLC
RLC
RLC
RLC
STA 2001
HLT

TP04: Left shift 8 bits of 16-bits data (shi left without carry)

- Statement: Do 8 bits shifting of 16-bits data in memory location 2000H and 2001H then store shifting data to memory location 2002H and 2003H.
- Sample Problem: (2001H & 2000H) = 04 05 = 0000 0100 0000 0101
- Result: (2003H & 2002H) = 05 04 = 0000 0101 0000 0100

```
LHLD 2000
XCHG
MOV L, D
MOV H, E
SHLD 2002
HLT
```

TP05: Alter the content of flags register 8085

- Statement: Modify the content of all flags in 8085
- Sample Problem:

S	Z	X	AC	X	P	X	CY
1	0	1	1	0	1	0	0

- Result:

S	Z	X	AC	X	P	X	CY
0	1	0	0	1	0	1	1

TP06: Calculate the sum of series of 8 bits numbers (no carry)

- Statement: Calculate the sum of series of 8-bits data from memory location 2000H to 2003H using branching instruction to loop. Memory location 2010H will be store the amount of series number to sum. Then store the sum data to address 2005H.
- Sample Problem: 2000H = 05, 2001H = 04H
  2002H = 50, 2003H = 10H
- Result: (2005) = 69H

```
LDA 2010
MOV C, A
MVI A, 00
LXI H, 2000
Loop: MOV B, M
ADC B
INX H
DCR C
JNZ LOOP
STA 2005
HLT
```

TP07: Calculate the sum of series of 8 bits numbers (with carry)

- Statement: Calculate the sum of series of 8-bits data from memory location 2000H to 2003H using branching instruction to loop. Memory location 2010H will be store the amount of series number to sum. Then store the sum data to address 2005H.
- Sample Problem: 2000H = 5A, 2001H = 10H
  2002H = 74, 2003H = 85H
- Result: (2005) = 63H, (2006) = 01H

```
LDA 2010
MOV B, A
MVI A, 00
MVI C, 00
LXI H, 2000
LOOP: ADD M
JNC SKIP
INR C
SKIP: INX H
DCR B
JNZ LOOP
STA 2005
MOV A, C
STA 2006
HLT
```

TP08: Calculate the sum of 1+2+...+n

- Statement: Calculate the sum from 1 to n number in memory location 2000H. Then store to address 2001H.
- Sample Problem: (2000H) = 04H
- Result: (2001H) = 01 + 02 + 03 + 04 = 0A

```
LDA 2000
MOV C, A
MVI A, 00
MVI B, 01
LOOP: ADD B
INR B
DCR C
JNZ LOOP
STA 2001
HLT
```

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Thanks