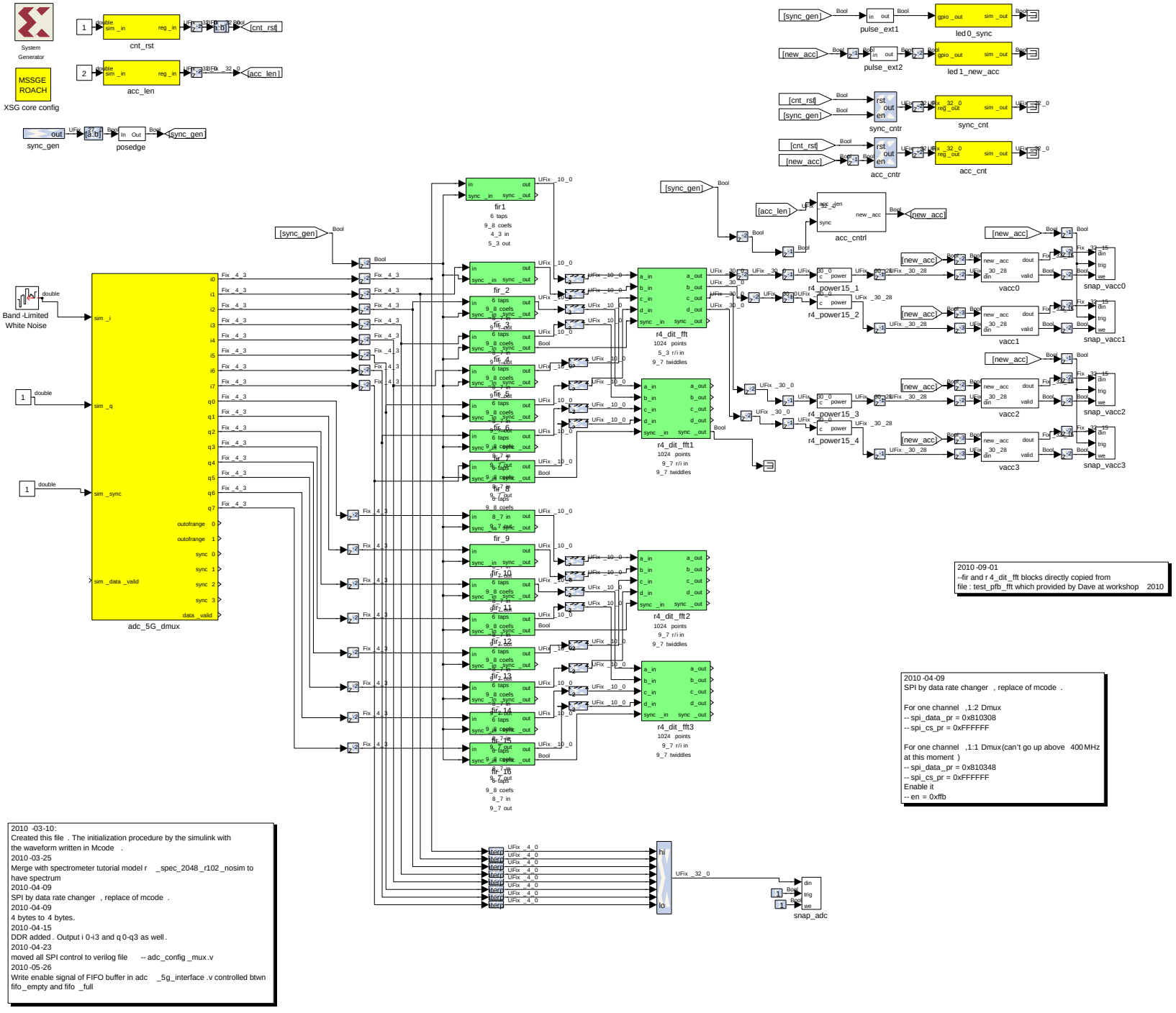
System Generator
MSSGE ROACH
XSG core config
cnt_rst
acc_len
sync_gen
posedge
[cnt_rst]
[acc_len]
[sync_gen]
pulse_ext1
pulse_ext2
led 0_sync
led 1_new_acc
[new_acc]
sync_cntr
sync_cnt
acc_cntr
acc_cnt
acc_cntrl
Band -Limited White Noise
adc_5G_dmux
fir1
fir_2
fir_3
fir_4
fir_5
fir_6
fir_7
fir_8
fir_9
fir_10
fir_11
fir_12
fir_13
fir_14
fir_15
fir_16
6 taps
9_8 coefs
4_3 in
5_3 out
8_7 in
9_7 out
r4_dit_fft
1024 points
5_3 r/i in
9_7 twiddles
r4_dit_fft1
r4_dit_fft2
r4_dit_fft3
r4_power15_1
r4_power15_2
r4_power15_3
r4_power15_4
vacc0
vacc1
vacc2
vacc3
snap_vacc0
snap_vacc1
snap_vacc2
snap_vacc3
snap_adc
2010 -09-01
--fir and r 4_dit _fft blocks directly copied from
file : test_pfb_fft which provided by Dave at workshop 2010
2010 -04-09
SPI by data rate changer , replace of mcode .
For one channel ,1:2 Dmux
-- spi_data _pr = 0x810308
-- spi_cs_pr = 0xFFFFFF
For one channel ,1:1 Dmux(can't go up above 400MHz
at this moment)
-- spi_data _pr = 0x810348
-- spi_cs_pr = 0xFFFFFF
Enable it
-- en = 0xffb
2010 -03-10:
Created this file . The initialization procedure by the simulink with
the waveform written in Mcode .
2010 -03-25
Merge with spectrometer tutorial model r _spec_2048 _r102 _nosim to
have spectrum
2010 -04-09
SPI by data rate changer , replace of mcode .
2010 -04-09
4 bytes to 4 bytes.
2010 -04-15
DDR added . Output i 0-i3 and q 0-q3 as well .
2010 -04-23
moved all SPI control to verilog file -- adc_config _mux .v
2010 -05-26
Write enable signal of FIFO buffer in adc _5g_interface .v controlled btwn
fifo _empty and fifo _full