HOMEWORK MUX

Revision 0

*Note: Late HW is **not** accepted! Put your **"last name, first name," the course number (3701), and the HW number** in the **top right hand corner** of the first page of **all** HW assignments. Also for **all** homework, use file name **HWx.pdf**. Do **NOT** put your social security number or your UF ID number on your HW.*

Design three circuits, each to implement the equation,

$$F_0 = \overline{W}\,X\,(Y + Z) + X\,\overline{Y}\,\overline{Z}\,.$$

For each of the circuits, you will use a 4-input MUX, along with a few SSI gates. When you build the circuits, first in Quartus and then on your bread board, you will use a 74'153 dual-MUX device inside Quartus, i.e., **not** with a 74'153 chip on your breadboard. First, you will design a circuit to implement this equation without using the MUX enable and then you will design a second circuit to implement the equation **using** the MUX enable.

When you use Quartus to design with a 74'153 MUX (available under `others|maxplus2|74153`, and shown in Figure 1), you will find that the select lines are labeled A and B. Which select inputs correspond to A and B for you MUX? Verify the functioning of a 74'153 MUX (and if A B =S_1 S_0 or A B = S_0 S_1) by creating a new Quartus circuit (in a new project and file, **Lab2_MUX_TEST**) using only this chip, inputs, and outputs. Simulate this design using enough different input combinations to prove that the 74'153 works as you suspect it should. Note: For every "new" part you use (like the 74'153), if you are not sure of a pins function, you should **verify its operation before** using it in a circuit. Include this design and simulation in your homework submission.

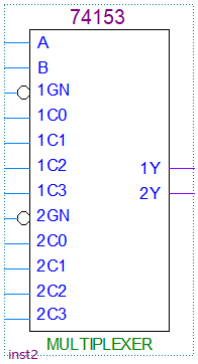

Figure 1: 74'153 in Quartus.

- Create a truth table for the above equation.
- Derive **both** MSOP **and** MPOS logic expressions for the equation. (You may use K-maps, if desired.)
- Design a circuit (**EQU.bdf** in project **EQU**) to implement this equation with a single 74'153 chip (in Quartus) and (only if necessary) the gates available on 74'00, 74'02, and/or 74'04 ICs. But do **not** use the MUX enable in this design. *Label all gates and show device pin numbers.* Your design must (non-trivially) use a 74'153. Use the MUX select lines as follows: S_1 = W(H) and S_0 = Y(H). Note that the 74'153 (see Figure 4) includes two 4-input MUX's.
- Make a voltage table from the truth table and the activation-levels that you chose above.
- Simulate your design using Quartus to verify that your design works (by comparing it to the voltage table).
- Design another circuit in the same **EQU.bdf** that implements the same equation (below), but calls the output F_1 (instead of F_0) and this time **uses** the MUX enable.

$$F_1 = \overline{W}\,X\,(Y + Z) + X\,\overline{Y}\,\overline{Z}$$

- Add the new F_1 output to your previous Quartus simulation to verify that your design for F_1 works. .
- Design a new circuit to implement the same equation (with output F_2), but this time chose S_1 = W(H) and S_0 = Y(**L**).

$$F_2 = \overline{W}\,X\,(Y + Z) + X\,\overline{Y}\,\overline{Z}$$

- Demonstrate (to yourself) that your MUX F_1 and F_2 designs operate correctly.