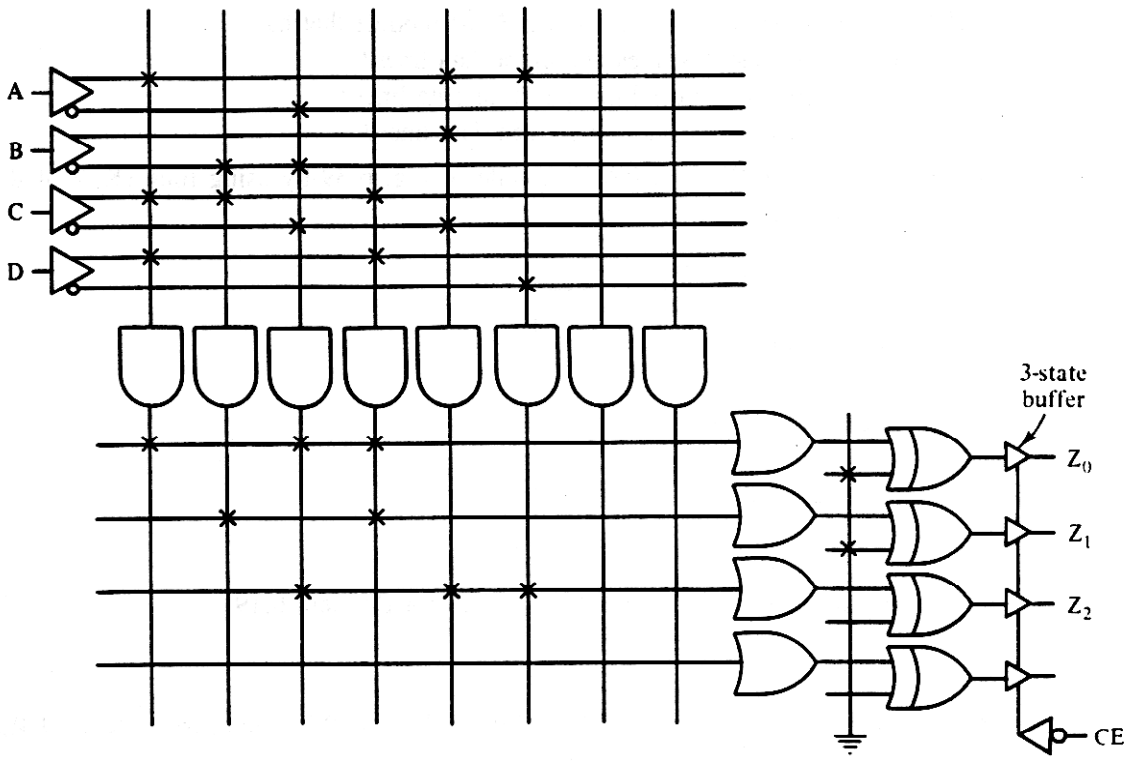

Figure 6.38 Programmed PLA for Problem 6.12.

6.13. What is the main difference between a PLA and a PAL?

6.14. Using the same PAL16L8, realize the following logic equations and have the realizations based on the following assignments:

Inputs: X_1.H is assigned to pin 2, X_2.H is assigned to pin 3, S_1.H is assigned to pin 17, and S_2.H is assigned to pin 16.

Outputs: Z_1.L is assigned to pin 19, Z_2.L is assigned to pin 18, Z_3.L is assigned to pin 12, and Z_4.H is assigned to pin 13.

All the other pins are not to be used unless specified otherwise.

(a) $Z_1 = S_2 \cdot X_1$ (*Hint:* Pin 16 needs to be programmed as an input.)

(b) $Z_2 = S_1 + S_1 \cdot \overline{X_2}$

(c) $Z_3 = X_2 \cdot (S_2 + S_1 \cdot \overline{X_1})$ (*Hint:* You can use pin 11 also if necessary.)

(d) $Z_4 = X_1 + X_2$ (*Hint:* Since Z_4 is active-high, you may need to use DeMorgan's laws.)

6.15. Using a PAL16L8, realize a BCD-to-7-segment decoder similar to the one shown in Fig. 6.28. However, the outputs a, b, c, d, e, f, and g are to be active-low.

6.16. Using a PAL16R4, realize a 4-bit decade counter with a synchronous CLEAR input. Compare your realization with the one obtained in Problem 5.26.

6.17. Draw block diagrams corresponding to the following static RAM module specifications. Specify the number of address lines and data lines.

(a) 64 × 4 bits **(b)** 4096 × 8 bits **(c)** 64K × 8 bits

6.18. What is the capacity of a static RAM module that has
(a) Seven address lines and eight data lines?
(b) Fourteen address lines and four data lines?
(c) Ten address lines and sixteen data lines?

6.19. Realize the 2K × 8 RAM module of Fig. 6.39 by using four 1K × 4 RAMs, as shown in Fig. 6.23, and an inverter.

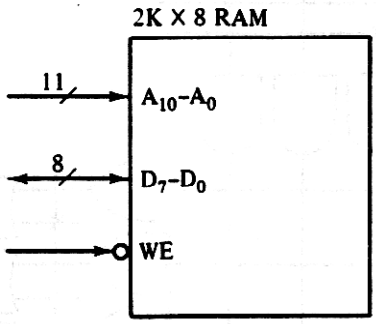

Figure 6.39 2K × 8 RAM module for Problem 6.19.

6.20. Realize the 4K × 4 RAM module of Fig. 6.40 by using four 1K × 4 RAMs, as shown in Fig. 6.23, and a 4-to-2 decoder.

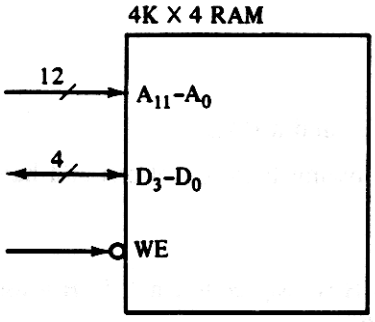

Figure 6.40 4K × 4 RAM module for Problem 6.20.

6.21. Realize the 2K × 4 RAM module with chip-select input of Fig. 6.41 by using 1K × 4 RAMs, as shown in Fig. 6.23, and any additional logic that is necessary.

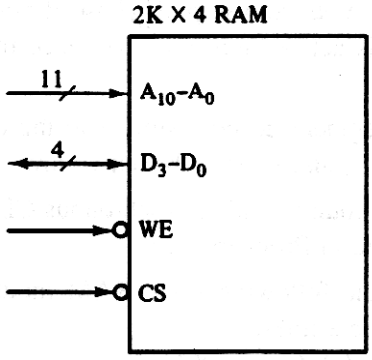

Figure 6.41 2K × 4 RAM module for Problem 6.21.

6.22. Realize the memory module of Fig. 6.42 by using a 1K × 4 RAM, as shown in Fig. 6.23, and any additional logic that is necessary. Note that the bidirectional data lines of the 1K × 4 RAM become two sets of data lines, DIN and DOUT. (*Hint:* Use three-state buffers.)

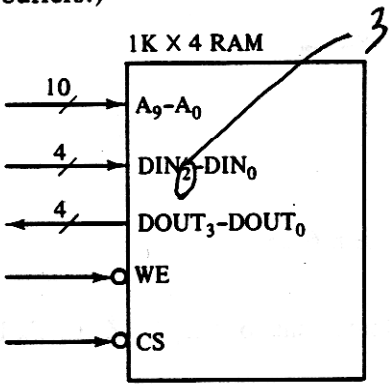

Figure 6.42 Memory module for Problem 6.22.

6.23. The static RAM chip shown in Fig. 6.26(a) has the following timing parameter values:

$$t_{RC} = 100 \text{ ns minimum}$$
$$t_A(AD) = 100 \text{ ns minimum}$$
$$t_A(CE) = 75 \text{ ns minimum}$$

At $t = 0$ s, a valid address is applied and the WE signal is set to false (H).

(a) If the chip-enable signal (CE) is applied at $t = 10$ ns, then when is the time t at which the data first becomes valid?

(b) If the chip-enable signal (CE) is applied at $t = 50$ ns, then when is the time t at which the data first becomes valid?

6.24. The static RAM chip shown in Fig. 6.26(a) has the following timing parameters:

$$t_{WC} = 100 \text{ ns minimum}$$
$$t_{SU}(CE) = 70 \text{ ns minimum}$$
$$t_W(WE) = 100 \text{ ns minimum}$$
$$t_{SU}(DA) = 70 \text{ ns minimum}$$

At $t = 0$ s, a valid address is applied and the WE signal is set to true (L).

(a) If CE and the data are applied at $t = 0$ s, then the WE signal must remain true (L) until a time t_x to ensure a valid write operation. What is this time t_x?

(b) If CE is applied at $t = 50$ ns and the data is applied at $t = 0$ s, then what is this time t_x?

(c) If CE is applied at $t = 0$ s and the data is applied at $t = 50$ ns, then what is this time t_x?

6.25. Discuss the similarities and differences among ROMs, PROMs, and EPROMs.

6.26. The hardware multiplier of Fig. 6.43 can multiply two 4-bit numbers (MCAND and MPLIER) and produce an 8-bit product (PRODUCT).

(a) Derive the truth table for this circuit. Use don't cares when convenient.

(b) If a ROM is used to realize this circuit, what must be the ROM capacity?

(c) Draw a block diagram of the ROM realization, specifying all connections to the address and data lines.

(d) What are the contents of the ROM? Explain in words.

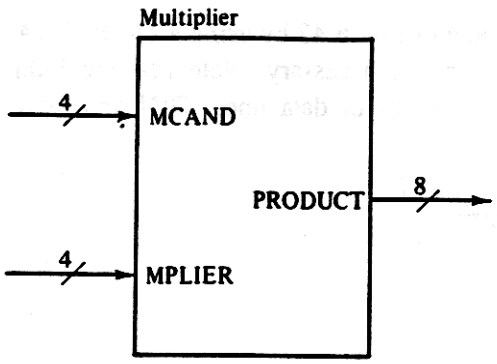

Figure 6.43 Multiplier for Problem 6.26.

6.27. Use a ROM to realize the four logic functions $Z_1.L$, $Z_2.L$, $Z_3.L$, and $Z_4.H$ specified in Problem 6.14 as follows:
(a) Draw a block diagram design of the ROM realization, specifying all connections to the address and data lines.
(b) Specify in hexadecimal the contents of the ROM.
(c) Explain what an active-low output does to the corresponding contents of the ROM.

6.28. Consider a PLA with 12 inputs (actually 12 inputs and 12 complements), 8 outputs, and 64 AND gates. Can it be used to realize the following combinational circuits?
(a) A circuit with eight inputs and six outputs.
(b) A circuit with six inputs and eight outputs.
In each case answer yes, no, or maybe, and explain your answer.

6.29. Can you implement the logic equations of the following combinational circuits with a 128 × 8 ROM?
(a) A circuit with eight inputs and six outputs.
(b) A circuit with six inputs and eight outputs.
In each case answer yes, no, or maybe, and explain your answer.

6.30. Construct the memory module of Fig. 6.44 that provides 6K × 8 bits of EPROM and 2K × 8 bits of RAM. [*Hint:* Use three 2716 EPROMs and two 1K × 8 RAM modules (see Fig. 6.24), a 2-to-4 decoder, and any additional logic that is necessary.]

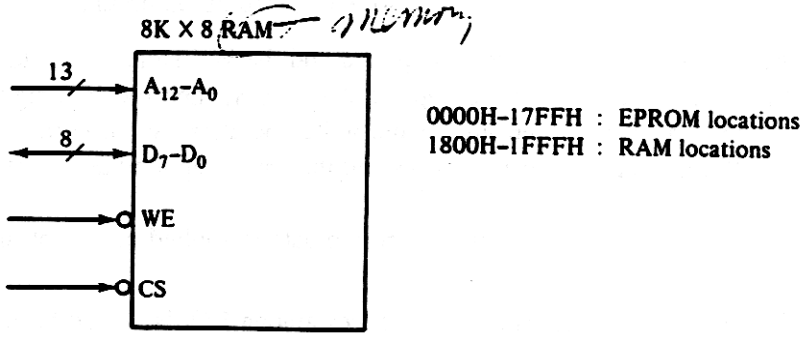

Figure 6.44 Memory module for Problem 6.30.

6.31. Discuss the advantages and disadvantages of using static RAMs versus dynamic RAMs in a digital circuit.

6.32. Consider the dynamic RAM of Fig. 6.45 that functions similarly to the one shown in Fig. 6.30(b).
(a) What is the capacity of this DRAM?